

## FEATURES:

- 0.5 MICRON CMOS Technology
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Low switching noise

## APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

## DESCRIPTION:

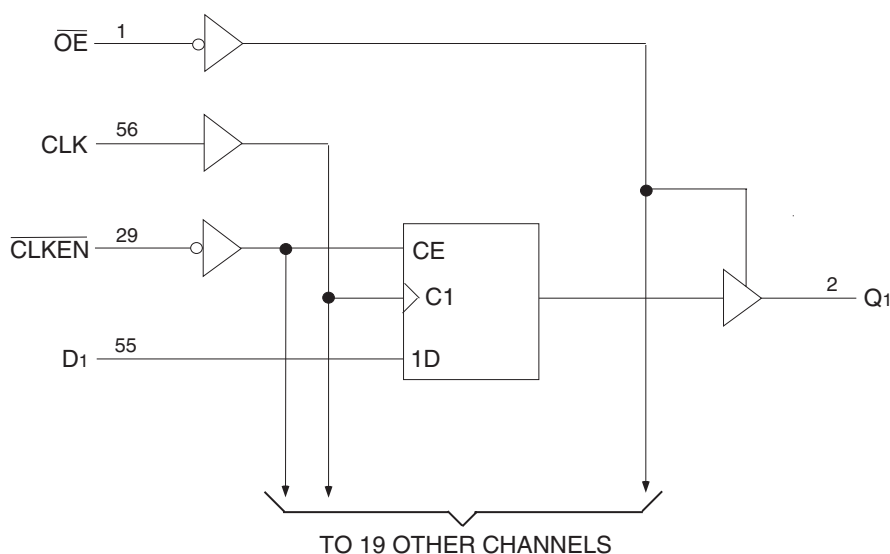
This 20-bit flip-flop is built using advanced dual metal CMOS technology. The 20 flip-flops of the ALVCH16721 are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable ( $\overline{CLKEN}$ ) input is low. If  $\overline{CLKEN}$  is high, no data is stored.

A buffered output-enable ( $\overline{OE}$ ) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

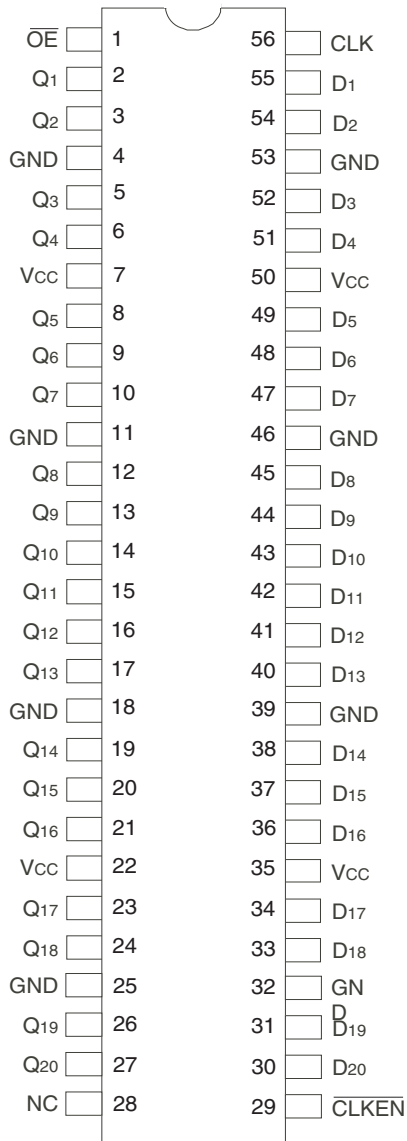
The ALVCH16721 has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16721 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
D <sub>x</sub>	Data Inputs <sup>(1)</sup>
Q <sub>x</sub>	3-State Outputs
CLK	Clock Input
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
NC	No Internal Connection

### NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE (EACH FLIP-FLOP)<sup>(1)</sup>

Inputs				Output
$\overline{OE}$	$\overline{CLKEN}$	CLK	D <sub>x</sub>	Q <sub>x</sub>
L	H	X	X	Q <sub>0</sub> <sup>(2)</sup>
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q <sub>0</sub> <sup>(2)</sup>
H	X	X	X	Z

### NOTES:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance  
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		2	—	—	
$V_{IL}$	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to $2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to $3.6\text{V}$		—	—	0.8	
$I_{IH}$	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	$\pm 10$	$\mu\text{A}$
$I_{OZL}$			$V_O = \text{GND}$	—	—	$\pm 10$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$ , $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	0.1	40	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ , other inputs at $V_{CC}$ or $\text{GND}$		—	—	750	$\mu\text{A}$

### NOTE:

1. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 3\text{V}$	$V_I = 2\text{V}$	-75	—	—	$\mu\text{A}$
			$V_I = 0.8\text{V}$	75	—	—	
$I_{BHH}$ $I_{BHL}$	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	$\mu\text{A}$
			$V_I = 0.7\text{V}$	45	—	—	
$I_{BHHO}$ $I_{BHLO}$	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to $3.6\text{V}$	—	—	$\pm 500$	$\mu\text{A}$

### NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range.  
TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	55	59	pF
CPD	Power Dissipation Capacitance Outputs disabled		46	49	

## SWITCHING CHARACTERISTICS<sup>(1)</sup>

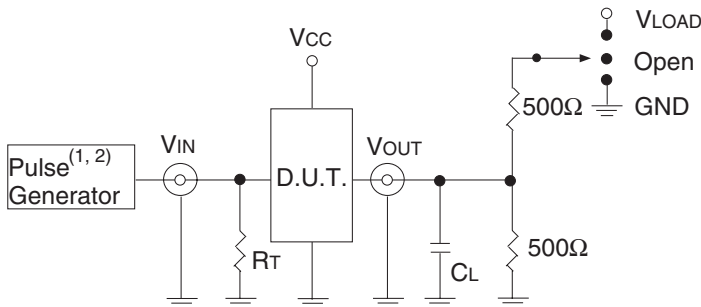
Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tMAX		150	—	150	—	150	—	MHz
tPLH	Propagation Delay	1	5.6	1	5.1	1	4.3	ns
tPHL	CLK to Qx							
tPZH	Output Enable Time	1	6.1	1	5.8	1	4.8	ns
tPZL	OE to Qx							
tPHZ	Output Disable Time	1	5.5	1	4.7	1	4.4	ns
tPLZ	OE to Qx							
tsu	Set-up Time, data before CLK↑	4	—	3.6	—	3.1	—	ns
tsu	Set-up Time, CLKEN before CLK↑	3.4	—	3.1	—	2.7	—	ns
tH	Hold Time, data after CLK↑	0	—	0	—	0	—	ns
tH	Hold Time, CLKEN after CLK↑	0	—	0	—	0	—	ns
tw	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tSK(O)	Output Skew <sup>(2)</sup>	—	—	—	—	—	500	ps

**NOTES:**  
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.  
2. Skew between any two outputs of the same package and switching in the same direction.

## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> = 3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> = 2.7V	V <sub>CC</sub> <sup>(2)</sup> = 2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

#### DEFINITIONS:

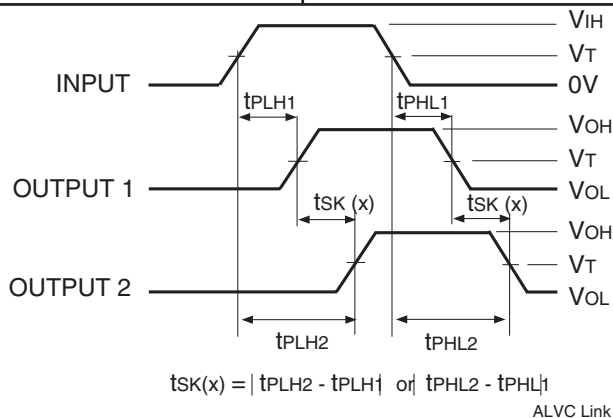
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2ns; t<sub>r</sub> ≤ 2ns.

### SWITCH POSITION

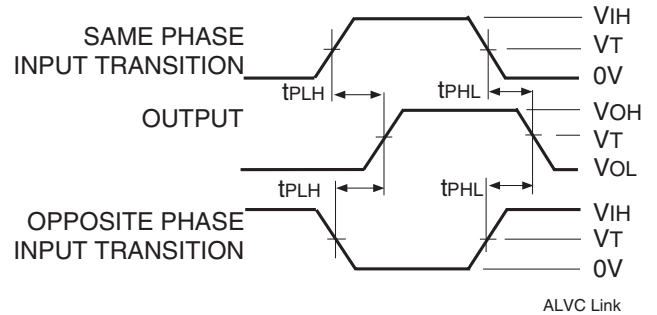
Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open



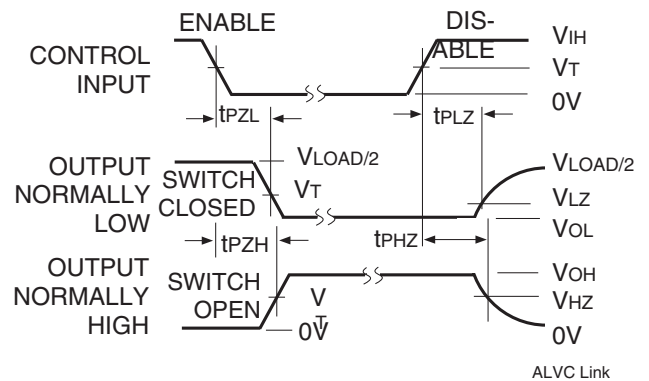
Output Skew - t<sub>SK</sub>(x)

#### NOTES:

1. For t<sub>SK</sub>(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.



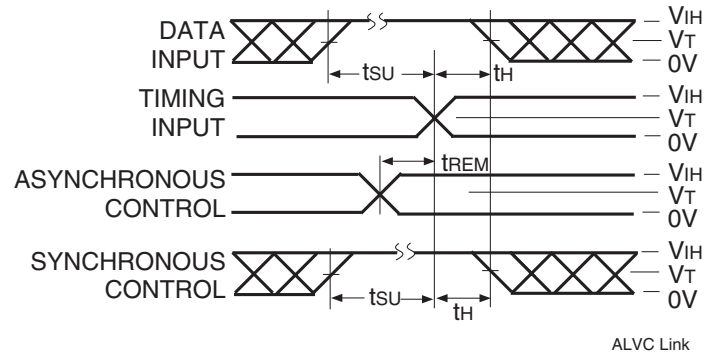
Propagation Delay



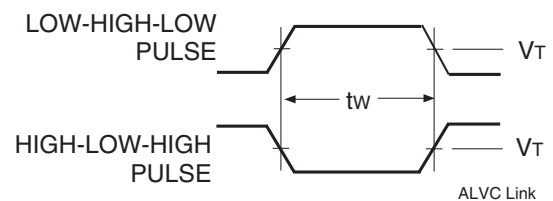
Enable and Disable Times

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION

<u>XX</u>	<u>ALVC</u>	<u>X</u>	<u>XXX</u>	<u>XXX</u>	<u>XX</u>	
Temp. Range		Bus-Hold	Family	Device Type	Package	
					PAG	Thin Shrink Small Outline Package - Green
					721	20-Bit Flip-Flop with 3-State Outputs
					16	Double-Density, ±24mA
					H	Bus-Hold
					74	−40°C to +85°C

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.