

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

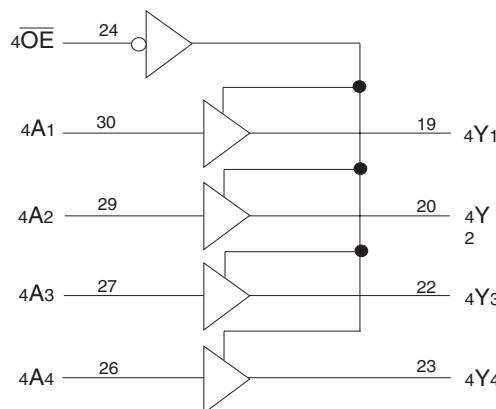
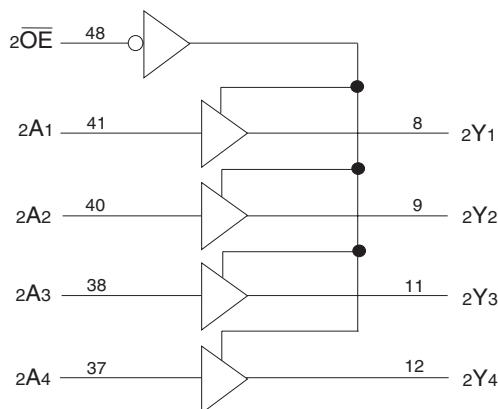
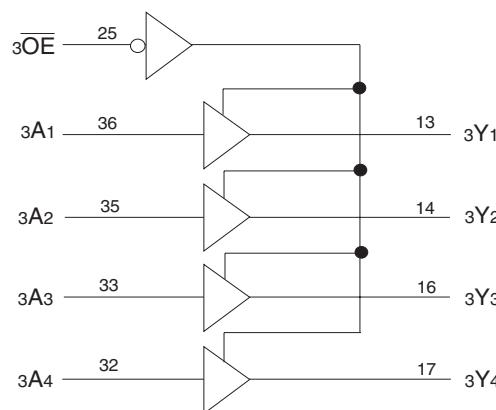
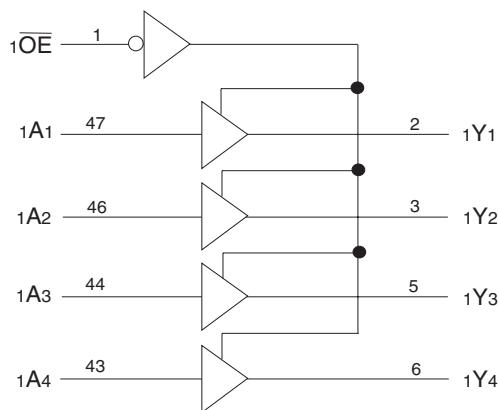
DESCRIPTION:

This 16-bit buffer/driver is built using advanced dual metal CMOS technology. The ALVC162244 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

The ALVC162244 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

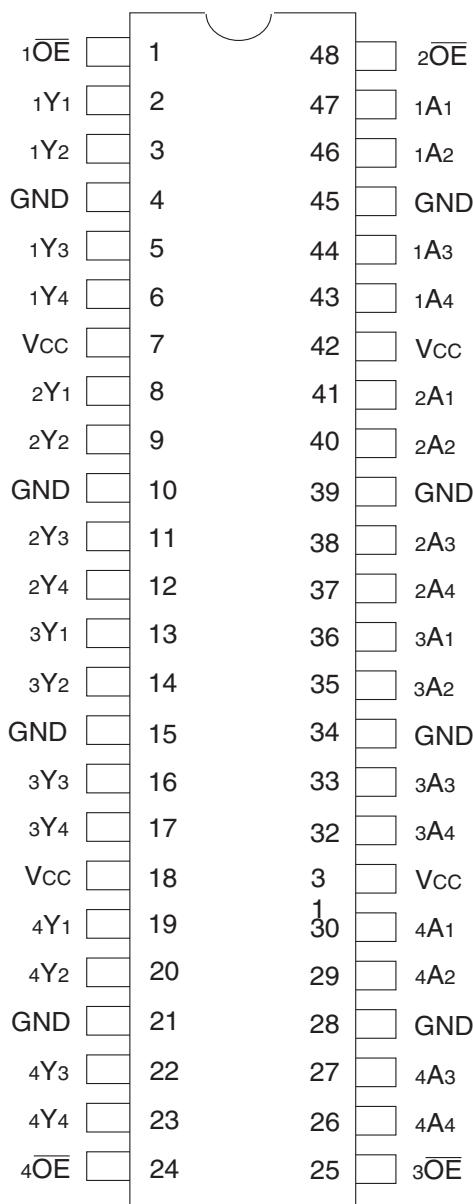
FUNCTIONAL BLOCK DIAGRAM

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INDUSTRIAL TEMPERATURE RANGE

JUNE 2009

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
Ik	Continuous Clamp Current, Vi < 0 or Vi > Vcc	±50	mA
Ik	Continuous Clamp Current, Vo < 0	-50	mA
Icc	Continuous Current through each Vcc or GND	±100	mA
Iss			

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
COUT	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
x̄OE	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

FUNCTION TABLE (EACH 4-BIT BUFFER)⁽¹⁾

Inputs		Outputs
x̄OE	xAx	xYx
L	H	H
L	L	L
H	X	Z

NOTE:

1. H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH	Input HIGH Current	VCC = 3.6V	VI = VCC	—	—	± 5	μA
IIL	Input LOW Current	VCC = 3.6V	VI = GND	—	—	± 5	μA
IOZH	High Impedance Output Current (3-State Output pins)	VCC = 3.6V		—	—	± 10	μA
				—	—	± 10	
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V VIN = GND or VCC		—	0.1	40	μA
				—	—	750	μA
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	750	μA

NOTE:

1. Typical values are at $VCC = 3.3V$, $+25^\circ\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	I _{OH} = -0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	I _{OH} = -4mA	1.9	—	
			I _{OH} = -6mA	1.7	—	
		VCC = 2.7V	I _{OH} = -4mA	2.2	—	
			I _{OH} = -8mA	2	—	
		VCC = 3V	I _{OH} = -6mA	2.4	—	
			I _{OH} = -12mA	2	—	
		VCC = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
			I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
			I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		VCC = 3V	I _{OL} = 6mA	—	0.55	
			I _{OL} = 12mA	—	0.8	

NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	16	19	pF
CPD	Power Dissipation Capacitance Outputs disabled		4	5	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay xAx to xYx	1	4.9	—	4.7	1	4.2	ns
t _{PHL}	Output Enable Time x _{OE} to xYx	1	6.8	—	6.7	1	5.6	ns
t _{PZH}	Output Disable Time x _{OE} to xYx	1	6.3	—	5.7	1	5.5	ns
t _{PLZ}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

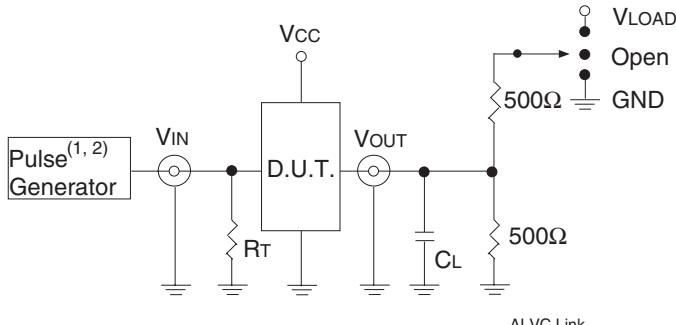
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

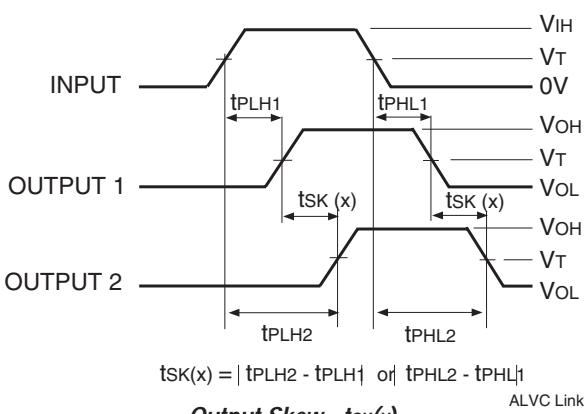
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2\text{ns}$; $t_r \leq 2\text{ns}$.

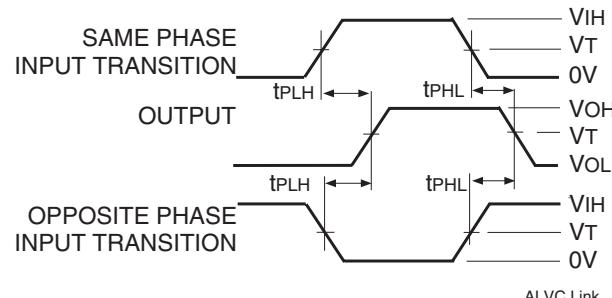
SWITCH POSITION

Test	Switch
Open Drain	
Disable Low	V_{LOAD}
Enable Low	
Disable High	GND
Enable High	
All Other Tests	Open

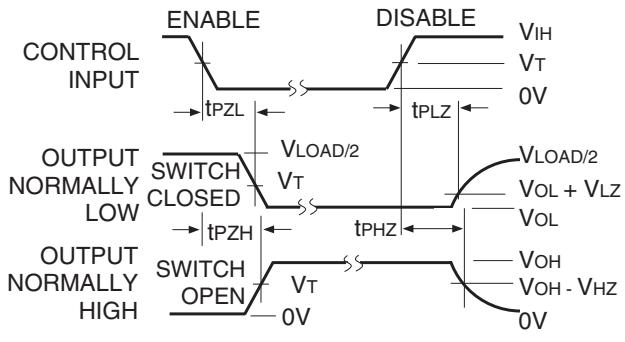


NOTES:

1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.



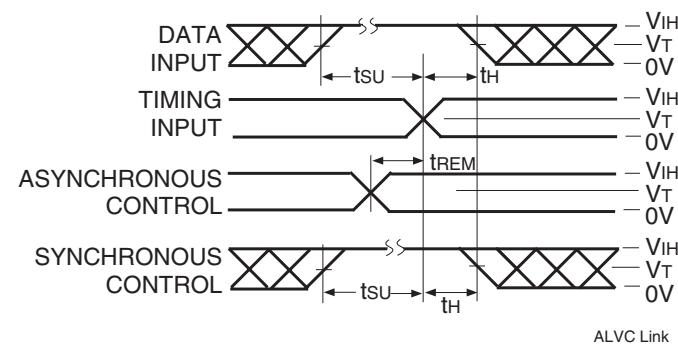
Propagation Delay



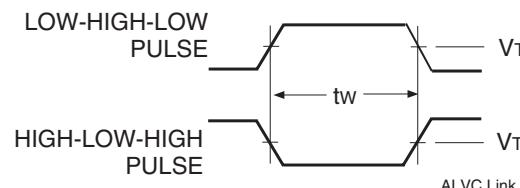
Enable and Disable Times

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

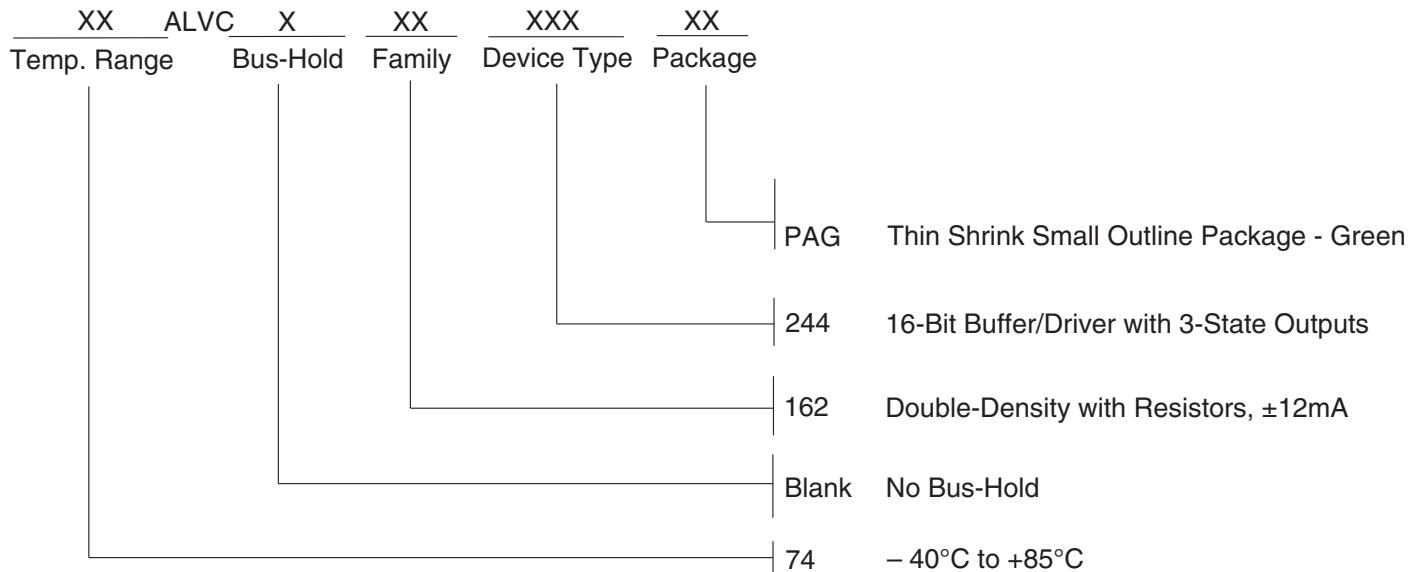


Set-up, Hold, and Release Times



Pulse Width

ORDERING INFORMATION



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