

FEATURES:

- Two independent FIFO memories for fully bidirectional data transfers
- 256 x 18 x 2 organization (IDT72605)
- 512 x 18 x 2 organization (IDT72615)
- Synchronous interface for fast (20ns) read and write cycle times
- Each data port has an independent clock and read/write control
- Output enable is provided on each port as a three-state control of the data bus
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Programmable flag offset can be set to any depth in the FIFO
- The synchronous BiFIFO is packaged in a 64-pin TQFP (Thin Quad Flatpack) and 68-pin PLCC
- Industrial temperature range (-40°C to +85°C)
- Green parts available, see ordering information

DESCRIPTION:

The IDT72605 and IDT72615 are very high-speed, low-power bidirectional First-In, First-Out (FIFO) memories, with synchronous interface for fast read and write cycle times. The SyncBiFIFO™ is a data buffer that can store or retrieve information from two sources simultaneously. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction.

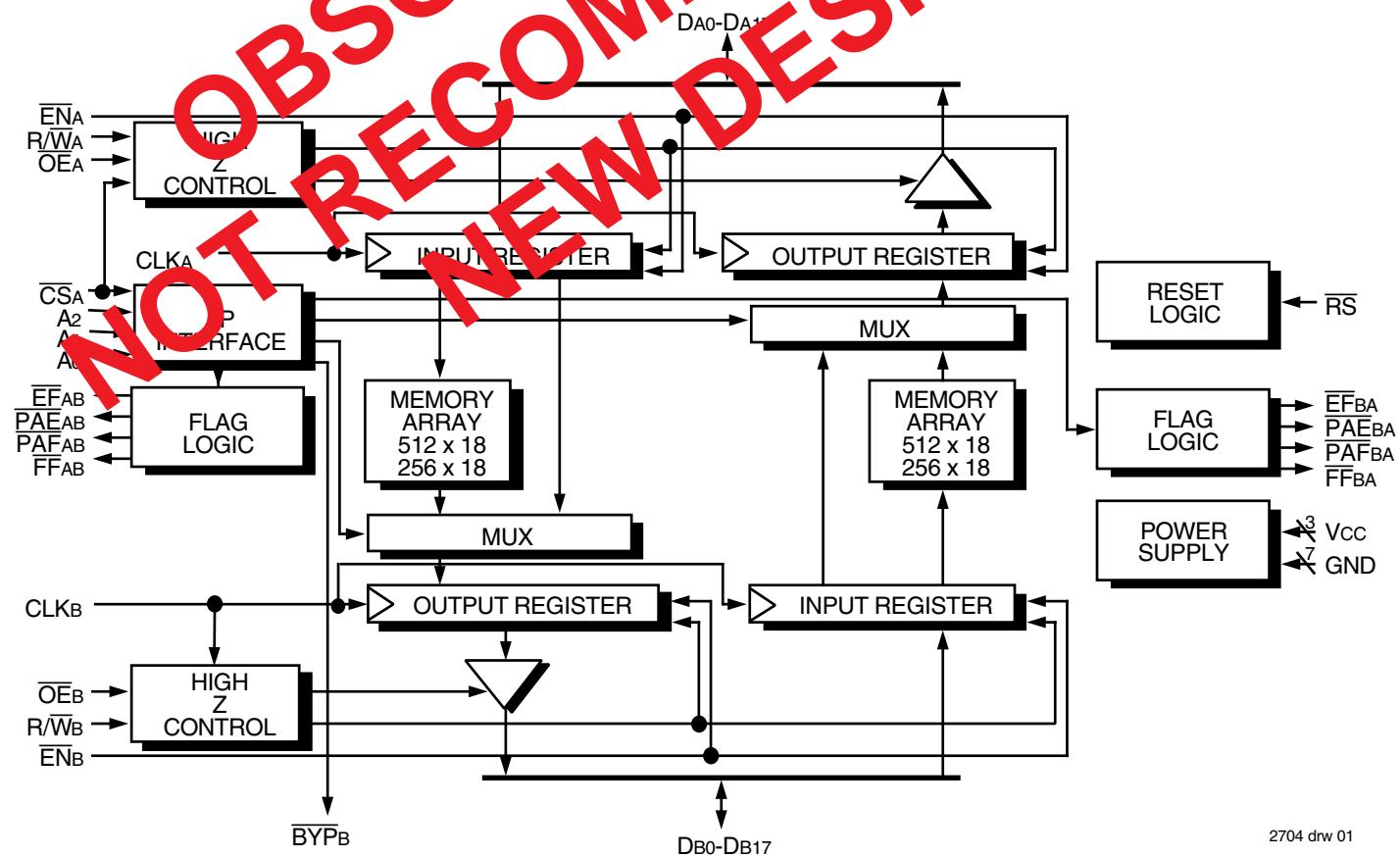
The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Each port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state.

Bypass control allows data to be directly transferred from input to output register in either direction.

The SyncBiFIFO has eight flags. The flag pins are Full, Empty, Almost-Full, and Almost-Empty for both FIFO memories. The offset depths of the Almost-Full and Almost-Empty flags can be programmed to any location.

The SyncBiFIFO is fabricated using IDT's high-speed, submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM

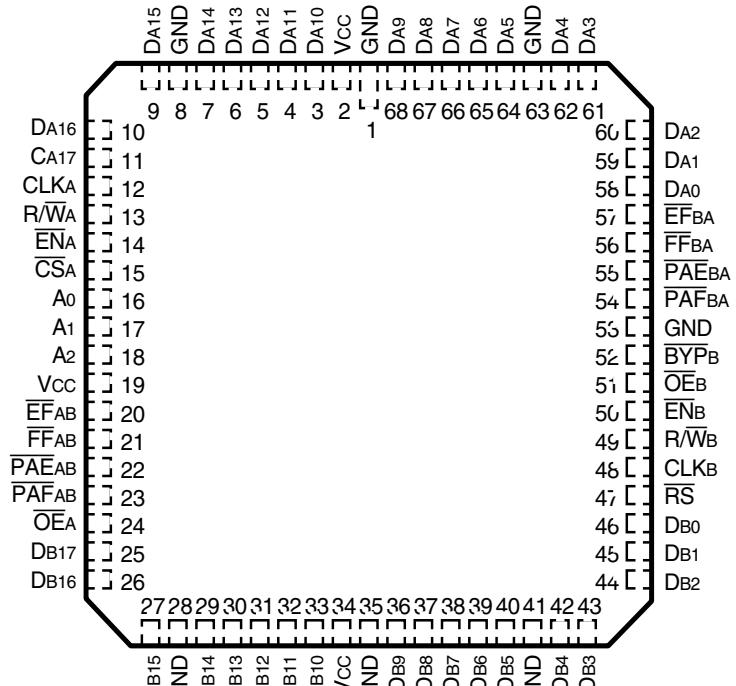


2704 drw 01

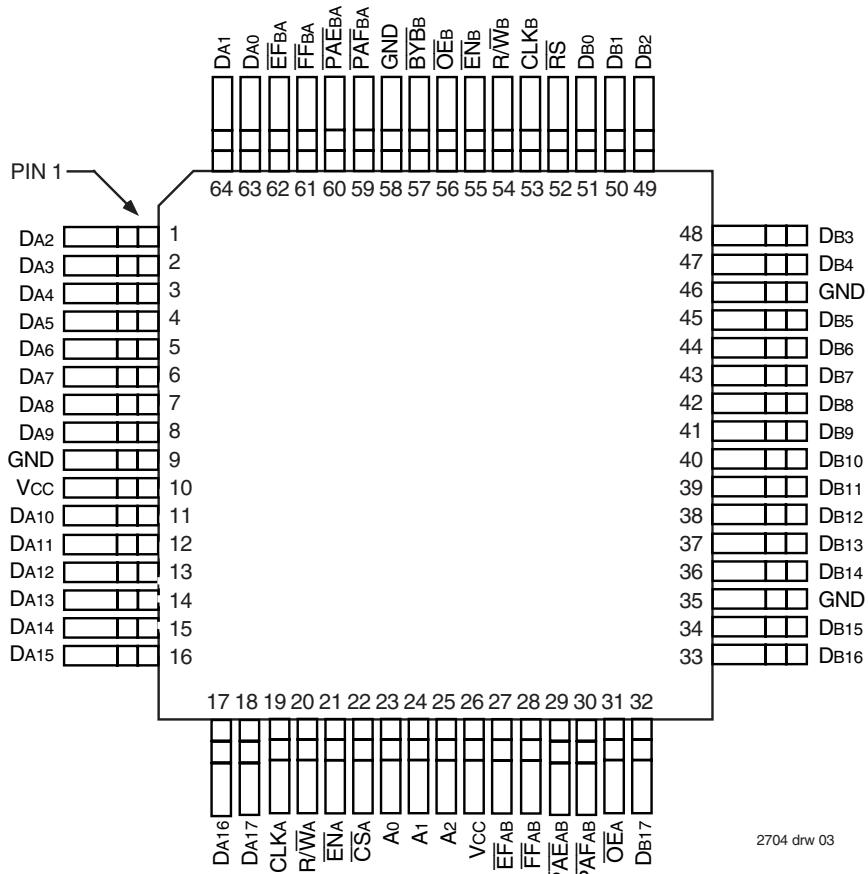
INDUSTRIAL TEMPERATURE RANGE

FEBRUARY 2009

PIN CONFIGURATIONS



PLCC (J68-1, order code: J)
TOP VIEW



TQFP (PN64-1, order code: PF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
DA0-DA17	Data A	I/O	Data inputs & outputs for the 18-bit Port A bus.
\bar{CS}_A	Chip Select A	I	Port A is accessed when \bar{CS}_A is LOW. Port A is inactive if \bar{CS}_A is HIGH.
$\bar{R/W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. If $\bar{R/W}_A$ is LOW, Data A input data is written into Port A. If $\bar{R/W}_A$ is HIGH, Data A output data is read from Port A. In bypass mode, when $\bar{R/W}_A$ is LOW, message is written into A→B output register. If $\bar{R/W}_A$ is HIGH, message is read from B→A output register.
CLKA	Clock A	I	CLKA is typically a free running clock. Data is read or written into Port A on the rising edge of CLKA.
\bar{EN}_A	Enable A	I	When \bar{EN}_A is LOW, data can be read or written to Port A. When \bar{EN}_A is HIGH, no data transfers occur.
\bar{OE}_A	Output Enable A	I	When $\bar{R/W}_A$ is HIGH, Port A is an output bus and \bar{OE}_A controls the high-impedance state of DA0-DA17. If \bar{OE}_A is HIGH, Port A is in a high-impedance state. If \bar{OE}_A is LOW while \bar{CS}_A is LOW and $\bar{R/W}_A$ is HIGH, Port A is in an active (low-impedance) state.
A0, A1, A2	Addresses	I	When \bar{CS}_A is asserted, A0, A1, A2 and $\bar{R/W}_A$ are used to select one of six internal resources.
DB0-DB17	Data B	I/O	Data inputs & outputs for the 18-bit Port B bus.
$\bar{R/W}_B$	Read/Write B	I	This pin controls the read or write direction of Port B. If $\bar{R/W}_B$ is LOW, Data B input data is written into Port B. If $\bar{R/W}_B$ is HIGH, Data B output data is read from Port B. In bypass mode, when $\bar{R/W}_B$ is LOW, message is written into B→A output register. If $\bar{R/W}_B$ is HIGH, message is read from A→B output register.
CLKB	Clock B	I	Clock B is typically a free running clock. Data is read or written into Port B on the rising edge of CLKB.
\bar{EN}_B	Enable B	I	When \bar{EN}_B is LOW, data can be read or written to Port B. When \bar{EN}_B is HIGH, no data transfers occur.
\bar{OE}_B	Output Enable B	I	When $\bar{R/W}_B$ is HIGH, Port B is an output bus and \bar{OE}_B controls the high-impedance state of DB0-DB17. If \bar{OE}_B is HIGH, Port B is in a high-impedance state. If \bar{OE}_B is LOW while $\bar{R/W}_B$ is HIGH, Port B is in an active (low-impedance) state.
\bar{EF}_{AB}	A→B Empty Flag	O	When \bar{EF}_{AB} is LOW, the A→B FIFO is empty and further data reads from Port B are inhibited. When \bar{EF}_{AB} is HIGH, the FIFO is not empty. \bar{EF}_{AB} is synchronized to CLKB. In the bypass mode, \bar{EF}_{AB} HIGH indicates that data DA0-DA17 is available for passing through. After the data DB0-DB17 has been read, \bar{EF}_{AB} goes LOW.
\bar{PAE}_{AB}	A→B Programmable Almost-Empty Flag	O	When \bar{PAE}_{AB} is LOW, the A→B FIFO is almost-empty. An almost-empty FIFO contains less than or equal to the offset programmed into \bar{PAE}_{AB} Register. When \bar{PAE}_{AB} is HIGH, the A→B FIFO contains more than offset in \bar{PAE}_{AB} Register. The default offset value for \bar{PAE}_{AB} Register is 8. \bar{PAE}_{AB} is synchronized to CLKB.
\bar{PAF}_{AB}	A→B Programmable Almost-Full Flag	O	When \bar{PAF}_{AB} is LOW, the A→B FIFO is almost-full. An almost-full FIFO contains greater than the FIFO depth minus the offset programmed into \bar{PAF}_{AB} Register. When \bar{PAF}_{AB} is HIGH, the A→B FIFO contains less than or equal to the depth minus the offset in \bar{PAF}_{AB} Register. The default offset value for \bar{PAF}_{AB} Register is 8. \bar{PAF}_{AB} is synchronized to CLKA.
\bar{FF}_{AB}	A→B Full Flag	O	When \bar{FF}_{AB} is LOW, the A→B FIFO is full and further data writes into Port A are inhibited. When \bar{FF}_{AB} is HIGH, the FIFO is not full. \bar{FF}_{AB} is synchronized to CLKA. In bypass mode, \bar{FF}_{AB} tells Port A that a message is waiting in Port B's output register. If \bar{FF}_{AB} is LOW, a bypass message is in the register. If \bar{FF}_{AB} is HIGH, Port B has read the message and another message can be written into Port A.
\bar{EF}_{BA}	B→A Empty Flag	O	When \bar{EF}_{BA} is LOW, the B→A FIFO is empty and further data reads from Port A are inhibited. When \bar{EF}_{BA} is HIGH, the FIFO is not empty. \bar{EF}_{BA} is synchronized to CLKA. In the bypass mode, \bar{EF}_{BA} HIGH indicates that data DB0-DB17 is available for passing through. After the data DA0-DA17 has been read, \bar{EF}_{BA} goes LOW on the following cycle.
\bar{PAE}_{BA}	B→A Programmable Almost-Empty Flag	O	When \bar{PAE}_{BA} is LOW, the B→A FIFO is almost-empty. An almost-empty FIFO contains less than or equal to the offset programmed into \bar{PAE}_{BA} Register. When \bar{PAE}_{BA} is HIGH, the B→A FIFO contains more than offset in \bar{PAE}_{BA} Register. The default offset value for \bar{PAE}_{BA} Register is 8. \bar{PAE}_{BA} is synchronized to CLKA.
\bar{PAF}_{BA}	B→A Programmable Almost-Full Flag	O	When \bar{PAF}_{BA} is LOW, the B→A FIFO is almost-full. An almost-full FIFO contains greater than the FIFO depth minus the offset programmed into \bar{PAF}_{BA} Register. When \bar{PAF}_{BA} is HIGH, the B→A FIFO contains less than or equal to the depth minus the offset in \bar{PAF}_{BA} Register. The default offset value for \bar{PAF}_{BA} Register is 8. \bar{PAF}_{BA} is synchronized to CLKB.
\bar{FF}_{BA}	B→A Full Flag	O	When \bar{FF}_{BA} is LOW, the B→A FIFO is full and further data writes into Port B are inhibited. When \bar{FF}_{BA} is HIGH, the FIFO is not full. \bar{FF}_{BA} is synchronized to CLKB. In bypass mode, \bar{FF}_{BA} tells Port B that a message is waiting in Port A's output register. If \bar{FF}_{BA} is LOW, a bypass message is in the register. If \bar{FF}_{BA} is HIGH, Port A has read the message and another message can be written into Port B.
\bar{BYP}_B	Port B Bypass Flag	O	This flag informs Port B that the synchronous BiFIFO is in bypass mode. When \bar{BYP}_B is LOW, Port A has placed the FIFO into bypass mode. If \bar{BYP}_B is HIGH, the synchronous BiFIFO passes data into memory. \bar{BYP}_B is synchronized to CLKB.
\bar{RS}	Reset	I	A LOW on this pin will perform a reset of all synchronous BiFIFO functions.
Vcc	Power		There are three +5V power pins for the PLCC and two for the TQFP.
GND	Ground		There are seven ground pins for the PLCC and four for the TQFP.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Industrial	Unit
VTERM	Terminal Voltage with Respect to Ground	-0.5 to +7.0	V
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	-50 to +50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL ⁽¹⁾	Input Low Voltage	—	—	0.8	V
TA	Operating Temperature	-40	—	85	°C

NOTE:

- 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C)

Symbol	Parameter	IDT72615L IDT72605L Industrial tCLK = 20, 25, 35, 50ns			Unit
		Min.	Typ.	Max.	
IL ⁽¹⁾	Input Leakage Current (Any Input)	-1	—	1	µA
ILO ⁽²⁾	Output Leakage Current	-10	—	10	µA
VOH	Output Logic "1" Voltage IOUT = -2mA	2.4	—	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	—	0.4	V
ICC ⁽³⁾	Active Power Supply Current	—	—	230	mA

NOTES:

- Measurements with 0.4V ≤ VIN ≤ VCC.
- OE_A, OE_B ≥ VIH; 0.4 ≤ VOUT ≤ VCC.
- Tested with outputs open (IOUT = 0). Testing frequency f=20MHz.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

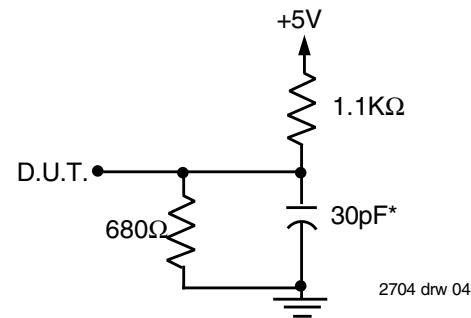
Symbol	Parameter	Conditions	Max.	Unit
CIN ⁽²⁾	Input Capacitance	VIN = 0V	10	pF
COUT ^(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES:

- With output deselected.
- Characterized values, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2



or equivalent circuit

Figure 2. Output Load

* Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 5V ± 10%, TA = -40°C to +85°C)

Symbol	Parameter	Industrial								Unit	Timing Figures
		IDT72615L20		IDT72615L25		IDT72615L35		IDT72615L50			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
f _{CLK}	Clock frequency	—	50	—	40	—	28	—	20	MHz	—
t _{CLK}	Clock cycle time	20	—	25	—	35	—	50	—	ns	4,5,6,7
t _{CLKH}	Clock HIGH time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t _{CLKL}	Clock LOW time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t _{RS}	Reset pulse width	20	—	25	—	35	—	50	—	ns	3
t _{RSS}	Reset setup time	12	—	15	—	21	—	30	—	ns	3
t _{RSR}	Reset recovery time	12	—	15	—	21	—	30	—	ns	3
t _{RSF}	Reset to flags in initial state	—	27	—	28	—	35	—	50	ns	3
t _A	Data access time	3	10	3	15	3	21	3	25	ns	5,7,8,9,10,11
t _{CS}	Control signal setup time ⁽¹⁾	6	—	6	—	8	—	10	—	ns	4,5,6,7,8,9,10,11, 12,13,14,15
t _{CH}	Control signal hold time ⁽¹⁾	1	—	1	—	1	—	1	—	ns	4,5,6,7,10,11,12, 13,14,15
t _{DS}	Data setup time	6	—	6	—	8	—	10	—	ns	4,6,8,9,10,11
t _{DH}	Data hold time	1	—	1	—	1	—	1	—	ns	4,6
t _{OE}	Output Enable LOW to output data valid ⁽²⁾	3	10	3	13	3	20	3	28	ns	5,7,8,9,10,11
t _{OLZ}	Output Enable LOW to data bus at Low-Z ⁽²⁾	0	—	0	—	0	—	0	—	ns	5,7,8,9,10,11
t _{OHZ}	Output Enable HIGH to data bus at High-Z ⁽²⁾	3	10	3	13	3	20	3	28	ns	5,7,10,11
t _{FF}	Clock to Full Flag time	—	10	—	15	—	21	—	30	ns	4,6,10,11
t _{EF}	Clock to Empty Flag time	—	10	—	15	—	21	—	30	ns	5,7,8,9,10,11
t _{PAE}	Clock to Programmable Almost-Empty Flag time	—	12	—	15	—	21	—	30	ns	12,14
t _{PAF}	Clock to Programmable Almost-Full Flag time	—	12	—	15	—	21	—	30	ns	13,15
t _{SKW1}	Skew between CLKA & CLKB for Empty/Full Flags ⁽²⁾	10	—	12	—	17	—	20	—	ns	4,5,6,7,8,9,10,11
t _{SKW2}	Skew between CLKA & CLKB for Programmable Flags ⁽²⁾	17	—	19	—	25	—	34	—	ns	4,7,12,13,14,15

NOTES:

1. Control signals refer to $\overline{\text{CS}}_{\text{A}}$, $\overline{\text{R}}\overline{\text{W}}_{\text{A}}$, $\overline{\text{EN}}_{\text{A}}$, A_2 , A_1 , A_0 , $\overline{\text{R}}\overline{\text{W}}_{\text{B}}$, $\overline{\text{EN}}_{\text{B}}$.
2. Minimum values are guaranteed by design.

FUNCTIONAL DESCRIPTION

IDT SyncBiFIFO is versatile for both multiprocessor and peripheral applications. Data can be stored or retrieved from two sources simultaneously.

The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction. Each port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the 18-bit bypass path.

The SyncBiFIFO can be used in multiples of 18-bits. In a 36- to 36-bit configuration, two SyncBiFIFOs operate in parallel. Both devices are programmed simultaneously, 18 data bits to each device. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, etc.) by adding more SyncBiFIFOs to the configuration. Figure 1 shows multiple SyncBiFIFOs configured for multiprocessor communication.

The microprocessor or microcontroller connected to Port A controls all operations of the SyncBiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B interfaces with a second processor. The Port B control pins are inputs driven by the second processor.

RESET

Reset is accomplished whenever the Reset (\overline{RS}) input is taken to a LOW state with \overline{CSA} , \overline{ENA} and \overline{ENB} HIGH. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The $A \rightarrow B$ and $B \rightarrow A$ FIFO Empty Flags (\overline{EF}_{AB} , \overline{EF}_{BA}) and Programmable Almost-Empty flags (\overline{PAE}_{AB} , \overline{PAE}_{BA}) will be set to LOW after t_{RSF}. The $A \rightarrow B$ and $B \rightarrow A$ FIFO Full Flags (\overline{FF}_{AB} , \overline{FF}_{BA}) and Programmable Almost-Full flags (\overline{PAF}_{AB} , \overline{PAF}_{BA}) will be set to HIGH after t_{RSF}. After the reset, the offsets of the Almost-Empty flags and Almost-Full flags for the $A \rightarrow B$ and $B \rightarrow A$ FIFO offset default to 8.

PORT A INTERFACE

The SyncBiFIFO is straightforward to use in micro-processor-based systems because each port has a standard microprocessor control set. Port A interfaces with microprocessor through the three address pins (A₂-A₀) and a Chip Select \overline{CSA} pins. When \overline{CSA} is asserted, A₂, A₁, A₀ and R/W_A are used to select one of six internal resources (Table 1).

With A₂=0 and A₁=0, A₀ determines whether data can be read out of output register or be written into the FIFO (A₀=0), or the data can pass through the FIFO through the bypass path (A₀=1).

With A₂=1, four programmable flags (two A \rightarrow B FIFO programmable flags and two B \rightarrow A FIFO programmable flags) can be selected: the A \rightarrow B FIFO Almost-Empty flag Offset (A₁=0, A₀=0), A \rightarrow B FIFO Almost-Full flag Offset (A₁=0, A₀=1), B \rightarrow A FIFO Almost-Empty flag Offset (A₁=1, A₀=0), B \rightarrow A FIFO Almost-Full flag Offset (A₁=1, A₀=1).

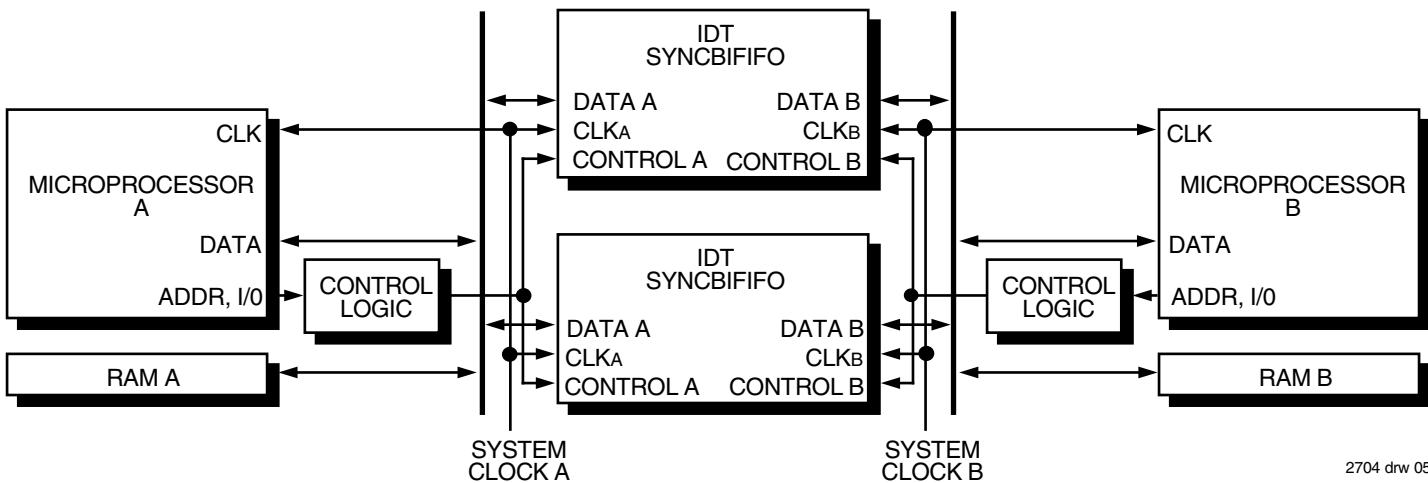
Port A is disabled when CSA is deasserted and data A is in high-impedance state.

BYPASS PATH

The bypass paths provide direct communication between Port A and Port B. There are two full 18-bit bypass paths, one in each direction. During a bypass operation, data is passed directly between the input and output registers, and the FIFO memory is undisturbed.

Port A initiates and terminates all bypass operations. The bypass flag, \overline{BYP}_B , is asserted to inform Port B that a bypass operation is beginning. The bypass flag state is controlled by the Port A controls, although the \overline{BYP}_B signal is synchronized to CLK_B. So, \overline{BYP}_B is asserted on the next rising edge of CLK_B when A₂A₁A₀=001 and CSA is LOW. When Port A returns to normal FIFO mode (A₂A₁A₀=000 or CSA is HIGH), \overline{BYP}_B is deasserted on the next CLK_B rising edge.

Once the SyncBiFIFO is in bypass mode, all data transfers are controlled by the standard Port A (R/W_A, CLK_A, \overline{ENA} , \overline{OE}_A) and Port B (R/W_B, CLK_B, \overline{ENB} , \overline{OE}_B) interface pins. Each bypass path can be considered as a one word deep FIFO. Data is held in each input register until it is read. Since the controls



2704 drw 05

NOTES:

1. Upper SyncBiFIFO only is used in 18- to 18-bit configuration.
2. Control A consists of R/W_A, \overline{ENA} , \overline{OE}_A , \overline{CSA} , A₂, A₁, A₀. Control B consists of R/W_B, \overline{ENB} , \overline{OE}_B .

Figure 1. 36- to 36-bit Processor Interface Configuration

TABLE 1 — PORT A OPERATION CONTROL SIGNALS

CSA	R/WA	ENA	OE_A	Data A I/O	Port A Operation
0	0	0	0	I	Data A is written on CLKA ≠. This write cycle immediately following low-impedance cycle is prohibited. Note that even though $\overline{OE}_A = 0$, a LOW logic level on R/WA, once qualified by a rising edge on CLKA, will put Data A into a high-impedance state.
0	0	0	1	I	Data A is written on CLKA ≠
0	0	1	X	I	Data A is ignored
0	1	0	0	O	Data is read ⁽¹⁾ from RAM array to output register on CLKA ≠, Data A is low-impedance
0	1	0	1	O	Data is read ⁽¹⁾ from RAM array to output register on CLKA ≠, Data A is high-impedance
0	1	1	0	O	Output register does not change ⁽²⁾ , Data A is low-impedance
0	1	1	1	O	Output register does not change ⁽²⁾ , Data A is high-impedance
1	0	X	X	I	Data A is ignored ⁽³⁾
1	1	X	X	O	Data A is high-impedance ⁽³⁾

NOTES:

1. When A2A1A0 = 000, the next B→A FIFO value is read out of the output register and the read pointer advances. If A2A1A0 = 001, the bypass path is selected and bypass data from the Port B input register is read from the Port A output register. If A2A1A0 = 1XX, a flag offset register is selected and its offset is read out through Port A output register.
2. Regardless of the condition of A2A1A0, the data in the Port A output register does not change and the B→A read pointer does not advance.
3. If CSA# is HIGH, then BYPB is HIGH. No bypass occur under this condition.

of each port operate independently, Port A can be reading bypass data at the same time Port B is reading bypass data.

When R/WA and ENA is LOW, data on pins DA0-DA17 is written into Port A input register. Following the rising edge of CLKA for this write, the A→B Full Flag (FFAB) goes LOW. Subsequent writes into Port A are blocked by internal logic until FFAB goes HIGH again. On the next CLK_B rising edge, the A→B Empty Flag (EFAB) goes HIGH indicating to Port B that data is available. Once R/WB is HIGH and ENB is LOW, data is read into the Port B output register. OE_B still controls whether Port B is in a high-impedance state. When OE_B is LOW, the output register data appears at DB0-DB17. EFAB goes LOW following the CLK_B rising edge for this read. FFAB goes HIGH on the next CLKA rising edge, letting Port A know that another word can be written through the bypass path.

Bypass data transfers from Port B to Port A work in a similar manner with EFBA and FFBA indicating the Port A output register state.

When the Port A address changes from bypass mode (A2A1A0=001) to FIFO mode (A2A1A0=000) on the rising edge of CLKA, the data held in the Port B output register may be overwritten. Unless Port A monitors the BYPB pin and waits for Port B to clock out the last bypass word, data from the A→B FIFO will overwrite data in the Port B output register. BYPB will go HIGH on the rising edge of CLK_B signifying that Port B has finished its last bypass operation. Port B must read any bypass data in the output register on this last CLK_B clock or it is lost and the SyncBiFIFO returns to FIFO operations. It is especially important to monitor BYPB when CLK_B is much slower than CLKA to avoid this condition. BYPB will also go HIGH after CSA is brought HIGH; in this manner the Port B bypass data may also be lost.

Since the Port A processor controls CSA and the bypass mode, this scenario can be handled for B→A bypass data. The Port A processor must be set up to read the last bypass word before leaving bypass mode.

PORT A CONTROL SIGNALS

The Port A control signals pins dictate the various operations shown in Table 2. Port A is accessed when CSA is LOW, and is inactive if CSA is HIGH. R/WA and ENA lines determine when Data A can be written or read. If R/WA and ENA are LOW, data is written into input register on the LOW-to-HIGH transition of CLKA. If R/WA is HIGH and OE_A is LOW, data comes out of bus and is read from output register into three-state buffer. Refer to pin descriptions for more information.

TABLE 2 — ACCESSING PORT A RESOURCES USING CSA, A2, A1, AND A0

CSA	A2	A1	A0	Read	Write
0	0	0	0	B→A FIFO	A→B FIFO
0	0	0	1	18-bit Bypass Path	
0	1	0	0	A→B FIFO Almost-Empty Flag Offset	
0	1	0	1	A→B FIFO Almost-Full Flag Offset	
0	1	1	0	B→A FIFO Almost-Empty Flag Offset	
0	1	1	1	B→A FIFO Almost-Full Flag Offset	
1	X	X	X	Port A Disabled	

PROGRAMMABLE FLAGS

The IDT SyncBiFIFO has eight flags: four flags for A→B FIFO (EFAB, PAEAB, PAFAB, FFAB), and four flags for B→A FIFO (EFBA, PAEBA, PAFBA, FFBA). The Empty and Full flags are fixed, while the Almost-Empty and Almost-Full offsets can be set to any depth through the Flag Offset Registers (see Table 3). The flags are asserted at the depths shown in the Flag Truth Table (Table 4). After reset, the programmable flag offsets are set to 8. This means the Almost-Empty flags are asserted at Empty +8 words deep, and the Almost-Full flags are asserted at Full -8 words deep.

The PAEAB is synchronized to CLK_B, while PAEAB is synchronized to CLKA; and PAEBA is synchronized to CLKA, while PAEBA is synchronized to CLK_B. If the minimum time (TSKEW2) between a rising CLK_B and a rising CLKA is met, the flag will change state on the current clock; otherwise, the flag may not change state until the next clock rising edge. For the specific flag timings, refer to Figures 12-15.

PORT B CONTROL SIGNALS

The Port B control signal pins dictate the various operations shown in Table 5. Port B is independent of CSA. R/WB and ENB lines determine when Data

can be written or read in Port B. If R/\bar{W}_B and \bar{E}_B are LOW, data is written into input register, and on LOW-to-HIGH transition of CLK_B data is written into input register and the FIFO memory. If R/\bar{W}_B is HIGH and \bar{O}_B is LOW, data comes out of bus and is read from output register into three-state buffer. In bypass mode,

if R/\bar{W}_B is LOW, bypass messages are transferred into $B \rightarrow A$ output register. If R/\bar{W}_B is HIGH, bypass messages are transferred into $A \rightarrow B$ output register. Refer to pin descriptions for more information.

TABLE 3—FLAG OFFSET REGISTER FORMAT

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0									
\bar{P}_{AEAB} Register	X	X	X	X	X	X	X	X	X	A \rightarrow B FIFO Almost-Empty Flag Offset																	
\bar{P}_{AFAB} Register	X	X	X	X	X	X	X	X	X	A \rightarrow B FIFO Almost-Full Flag Offset																	
\bar{P}_{AEBA} Register	X	X	X	X	X	X	X	X	X	B \rightarrow A FIFO Almost-Empty Flag Offset																	
\bar{P}_{AFBA} Register	X	X	X	X	X	X	X	X	X	B \rightarrow A FIFO Almost-Full Flag Offset																	

NOTE:

1. Bit 8 must be set to 0 for the IDT72605 (256 x 18) Synchronous BiFIFO.

TABLE 4—INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO		\bar{EF}	\bar{PAE}	\bar{PAF}	\bar{FF}
From	To				
0	0	LOW	LOW	HIGH	HIGH
1	n	HIGH	LOW	HIGH	HIGH
n+1	D-(m+1)	HIGH	HIGH	HIGH	HIGH
D-m	D-1	HIGH	HIGH	LOW	HIGH
D	D	HIGH	HIGH	LOW	LOW

NOTE:

1. n = Programmable Empty Offset (\bar{P}_{AEAB} Register or \bar{P}_{AEBA} Register)

m = Programmable Full Offset (\bar{P}_{AFAB} Register or \bar{P}_{AFBA} Register)

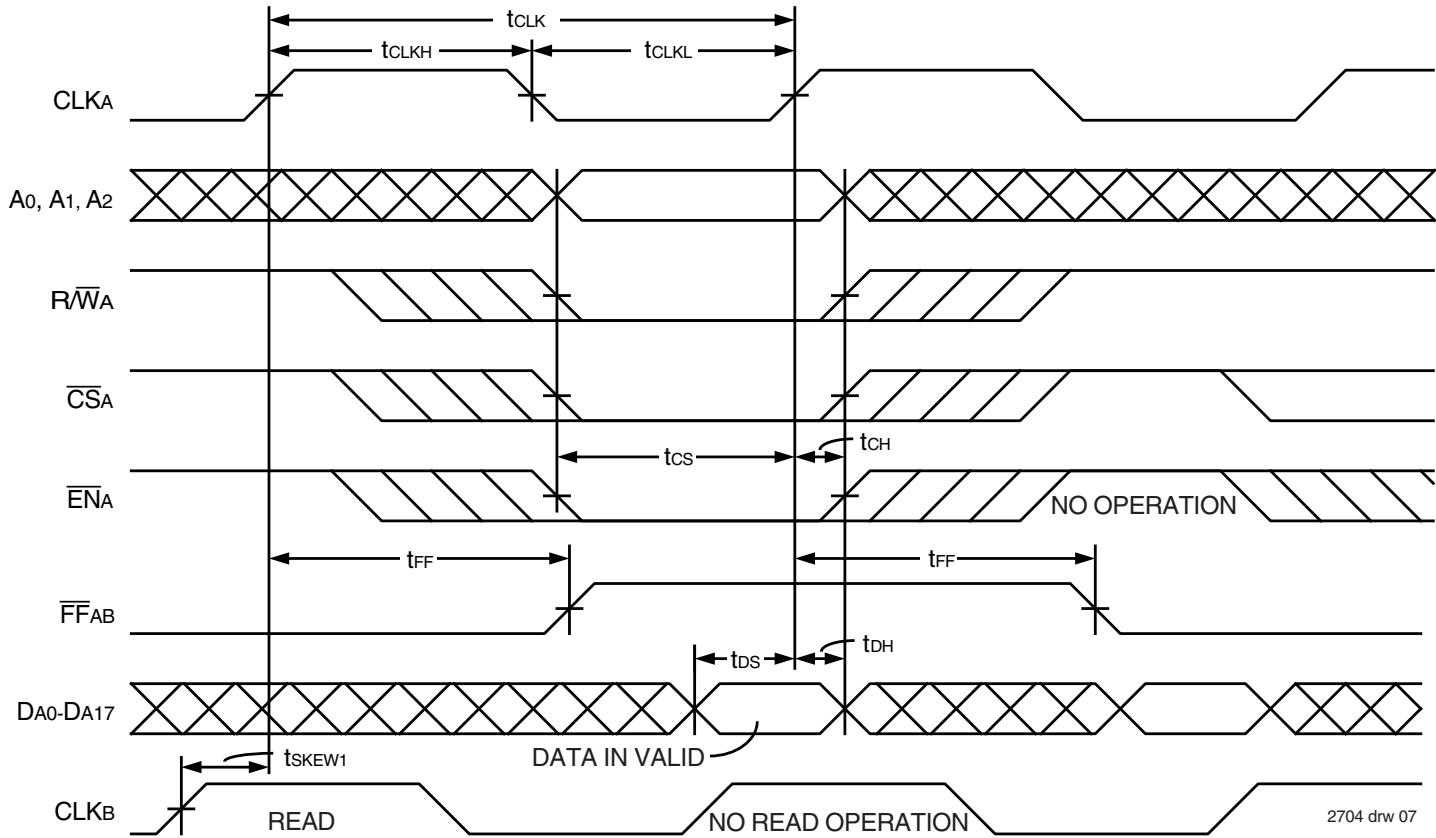
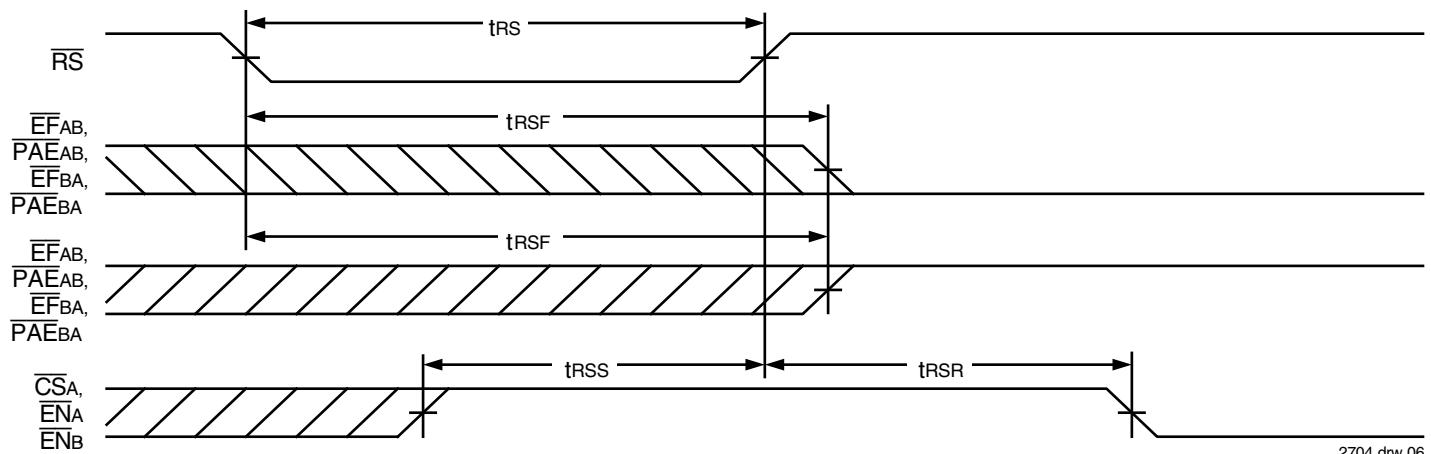
D = FIFO Depth (IDT72605 = 256 words, IDT72615 = 512 words)

TABLE 5—PORT B OPERATION CONTROL SIGNALS

R/\bar{W}_B	\bar{E}_B	\bar{O}_B	Data B I/O	Port B Operation
0	0	0	I	Data B is written on $CLK_B \uparrow$. This write cycle immediately following output low-impedance cycle is prohibited. Note that even though $\bar{O}_B = 0$, a LOW logic level on R/\bar{W}_B , once qualified by a rising edge on CLK_B , will put Data B into a high-impedance state.
0	0	1	I	Data B is written on $CLK_B \uparrow$.
0	1	X	I	Data B is ignored
1	0	0	O	Data is read ⁽¹⁾ from RAM array to output register on $CLK_B \neq$ Data B is low-impedance
1	0	1	O	Data is read ⁽¹⁾ from RAM array to output register on $CLK_B \neq$ Data B is high-impedance
1	1	0	O	Output register does not change ⁽²⁾ , Data B is low-impedance
1	1	1	O	Output register does not change ⁽²⁾ , Data B is high-impedance

NOTES:

1. When $A_2A_1A_0 = 000$ or $1XX$, the next $A \rightarrow B$ FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0 = 001$, the bypass path is selected and bypass data is read from the Port B output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port B output register does not change and the $A \rightarrow B$ read pointer does not advance.



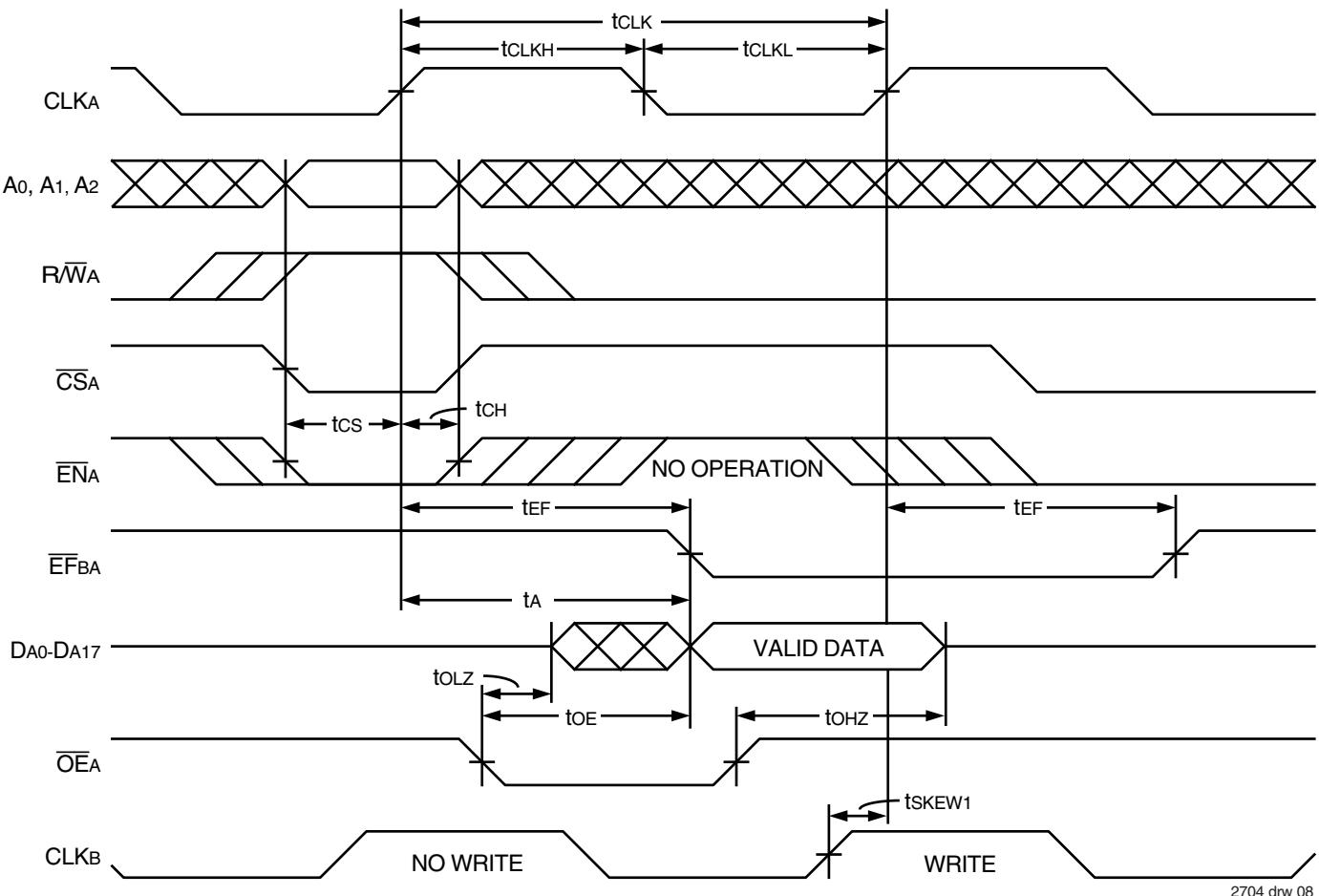


Figure 5. Port A (B→A) Read Timing

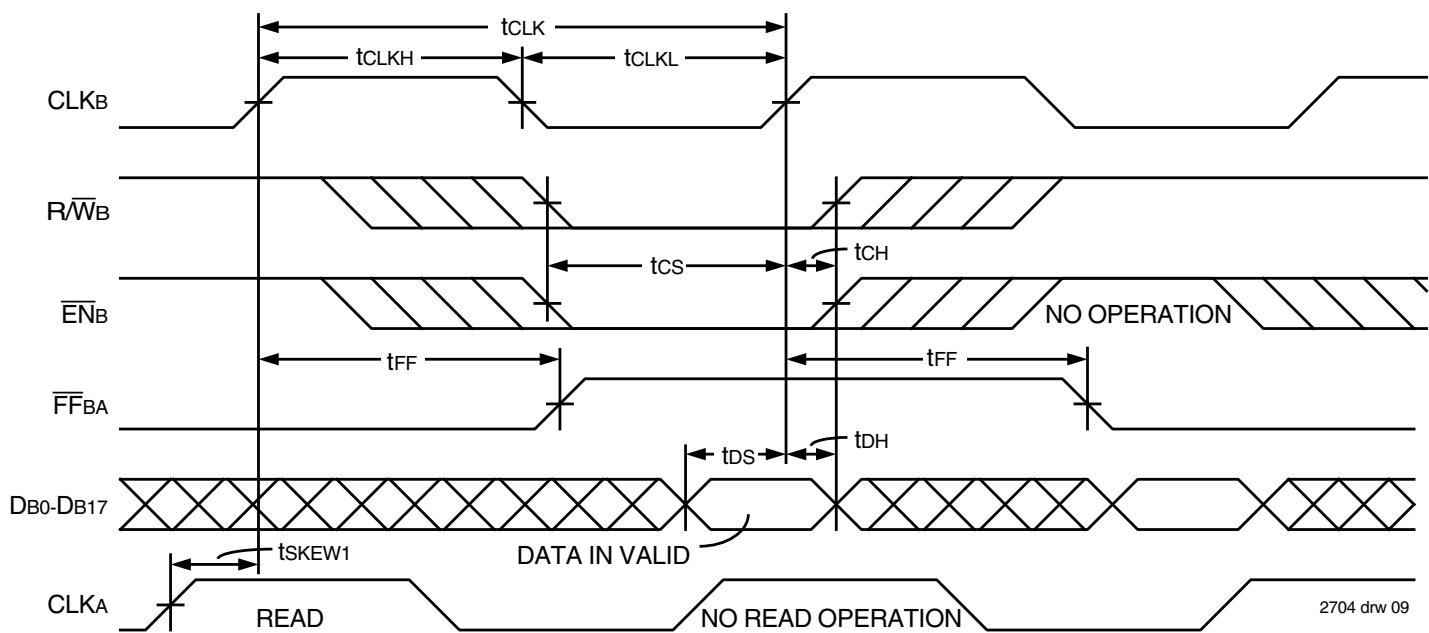


Figure 6. Port B (B→A) Write Timing

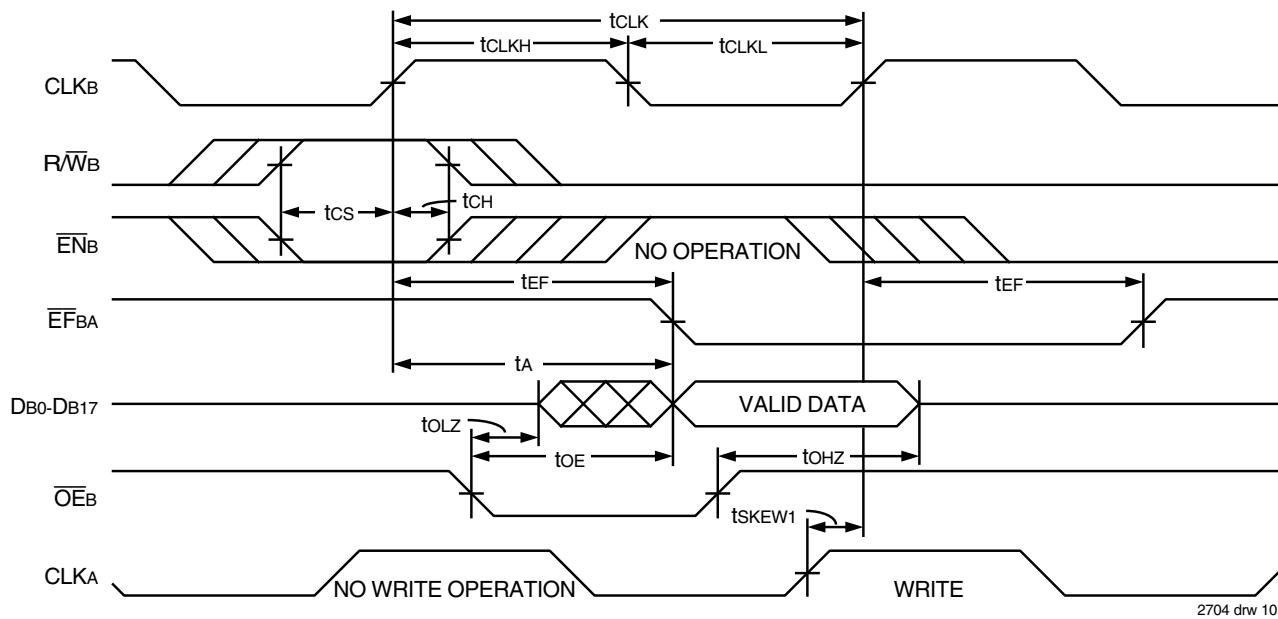
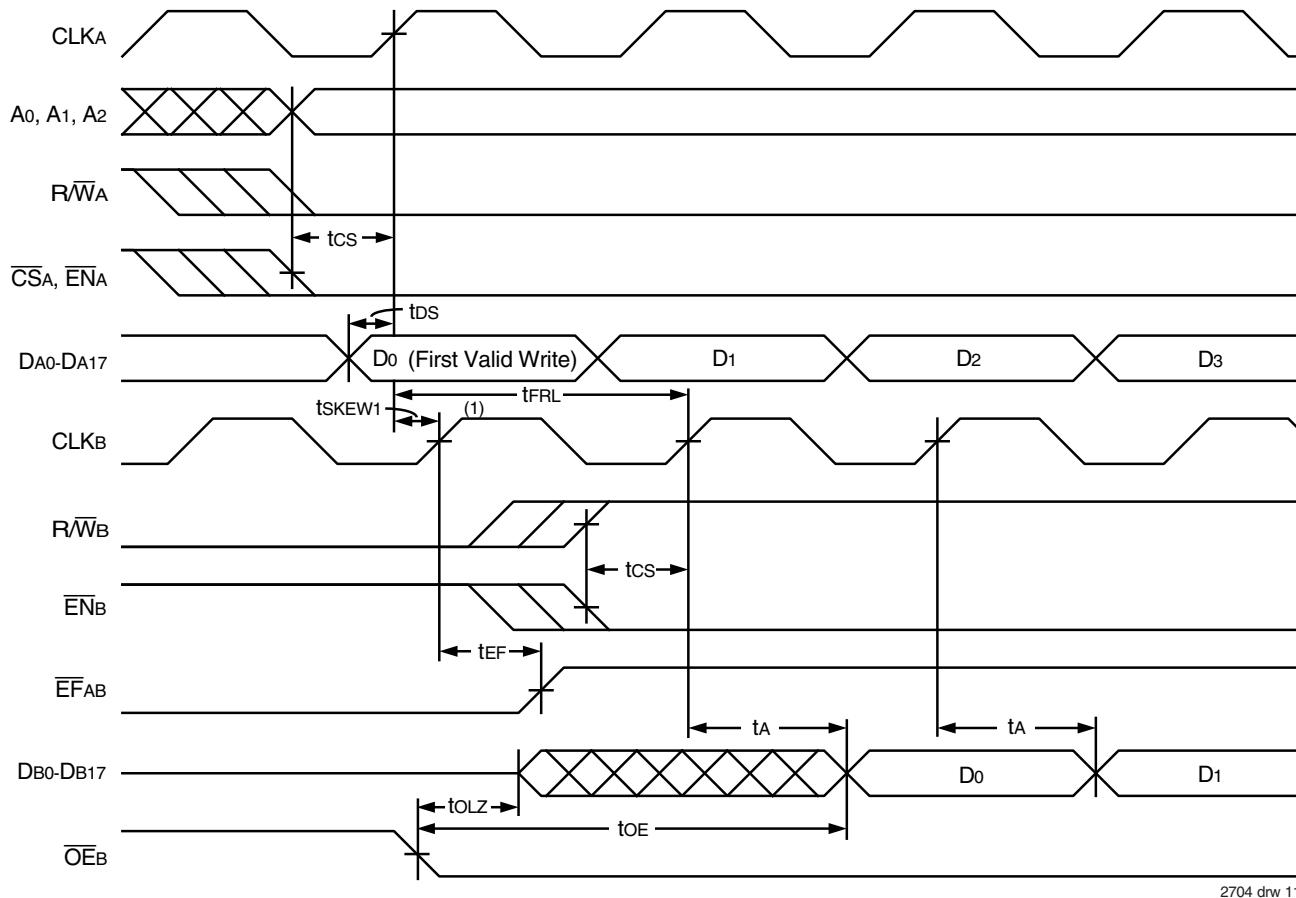


Figure 7. Port B ($A \rightarrow B$) Read Timing

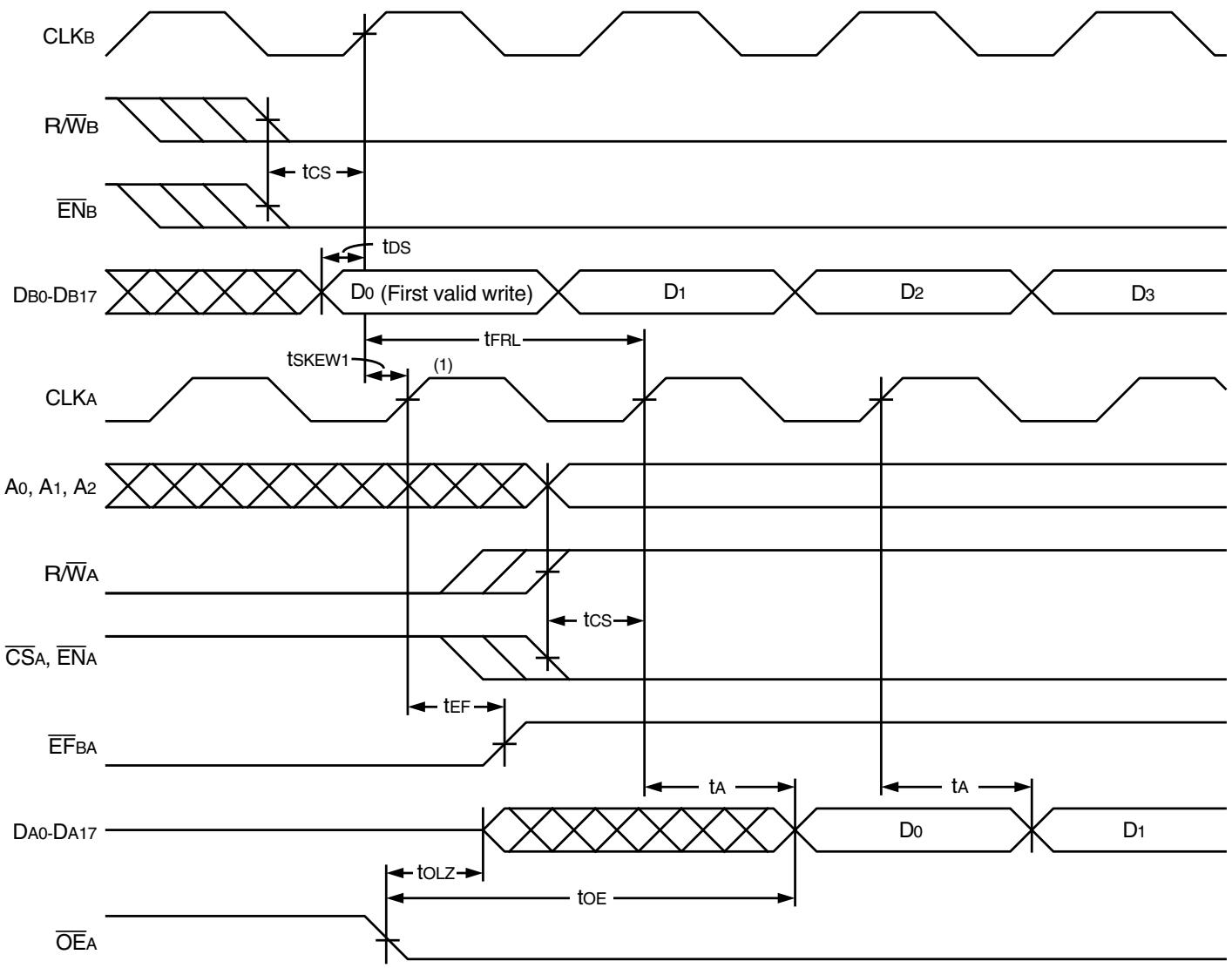


NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL}(\text{Max.}) = t_{CLK} + t_{SKEW1}$
 $t_{SKEW1} <$ minimum specification, $t_{FRL}(\text{Max.}) = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$

The Latency Timing applies only at the Empty Boundary ($\overline{EF} = \text{LOW}$).

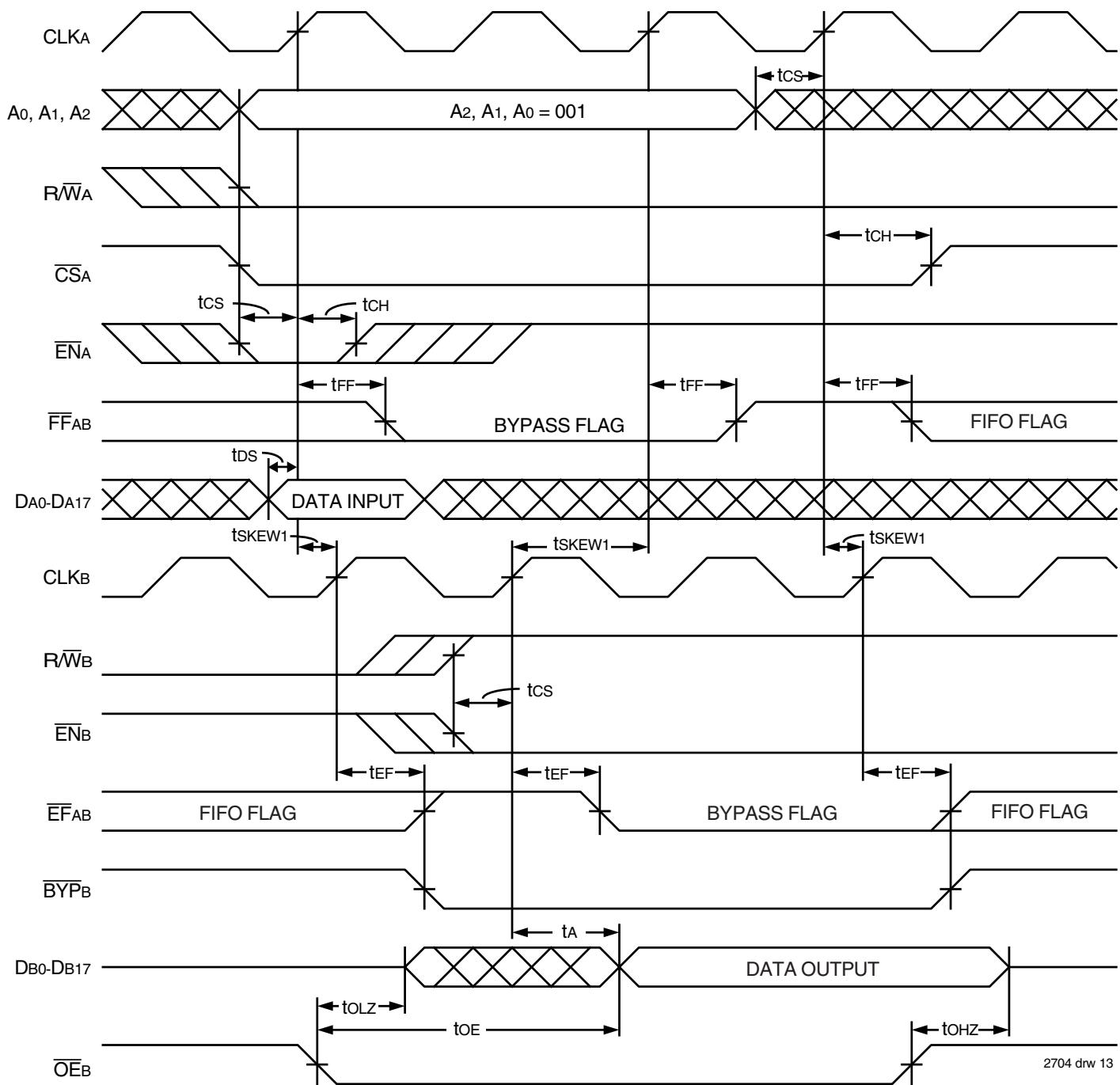
Figure 8. $A \rightarrow B$ First Data Word Latency after Reset for Simultaneous Read and Write



NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL}(\text{Max.}) = t_{CLK} + t_{SKEW1}$
 $t_{SKEW1} <$ minimum specification, $t_{FRL}(\text{Max.}) = 2t_{CLK} + t_{SKEW1}$
The Latency Timing apply only at the Empty Boundary ($\overline{E}\overline{F}$ = LOW).

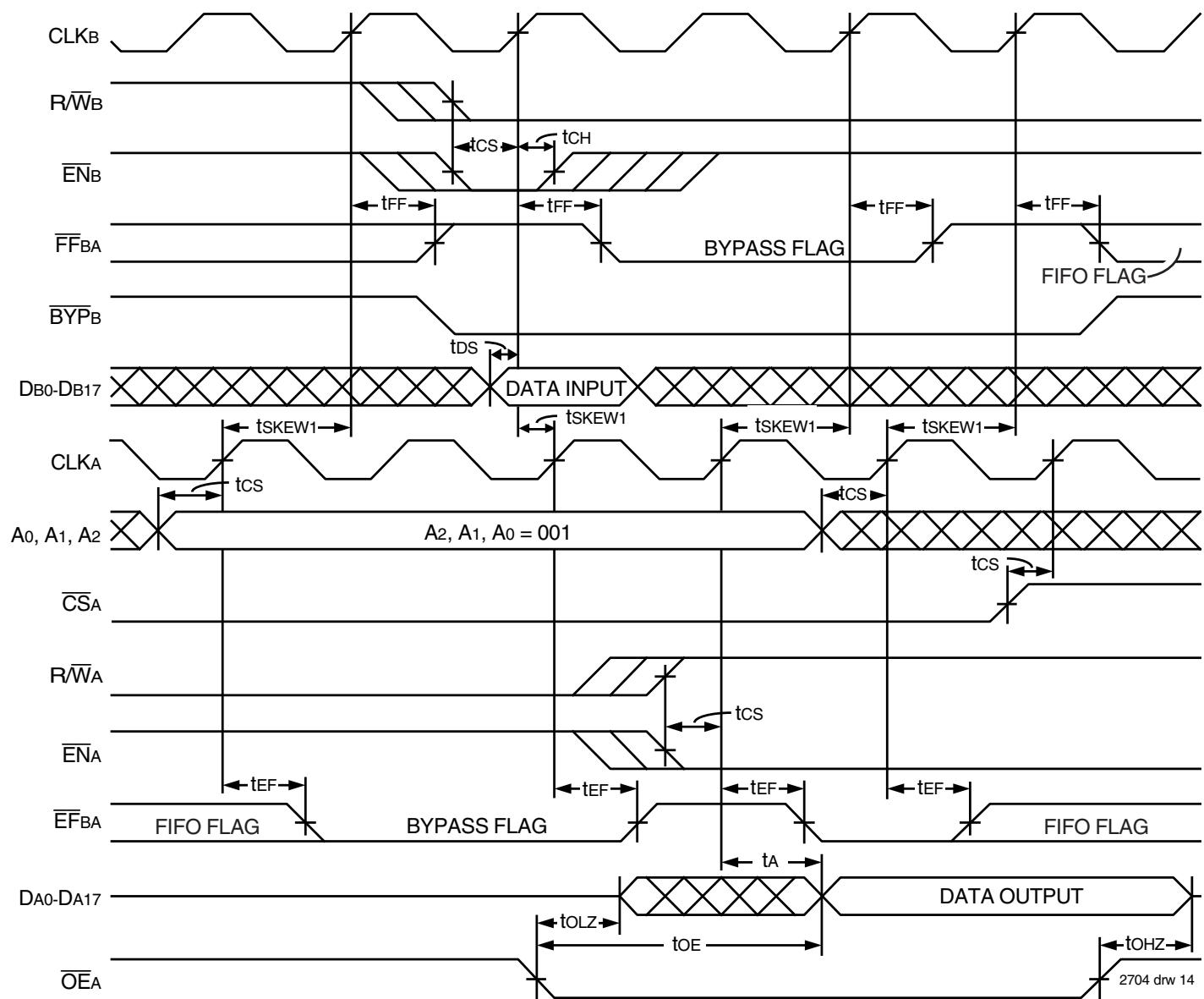
Figure 9. B→A First Data Word Latency after Reset for Simultaneous Read and Write



NOTES:

1. When \overline{CSA} is brought HIGH, A-to-B Bypass mode will switch to FIFO mode on the following CLKA LOW-to-HIGH transition.
2. After the bypass operation is completed, the \overline{BYPB} goes from LOW-to-HIGH; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

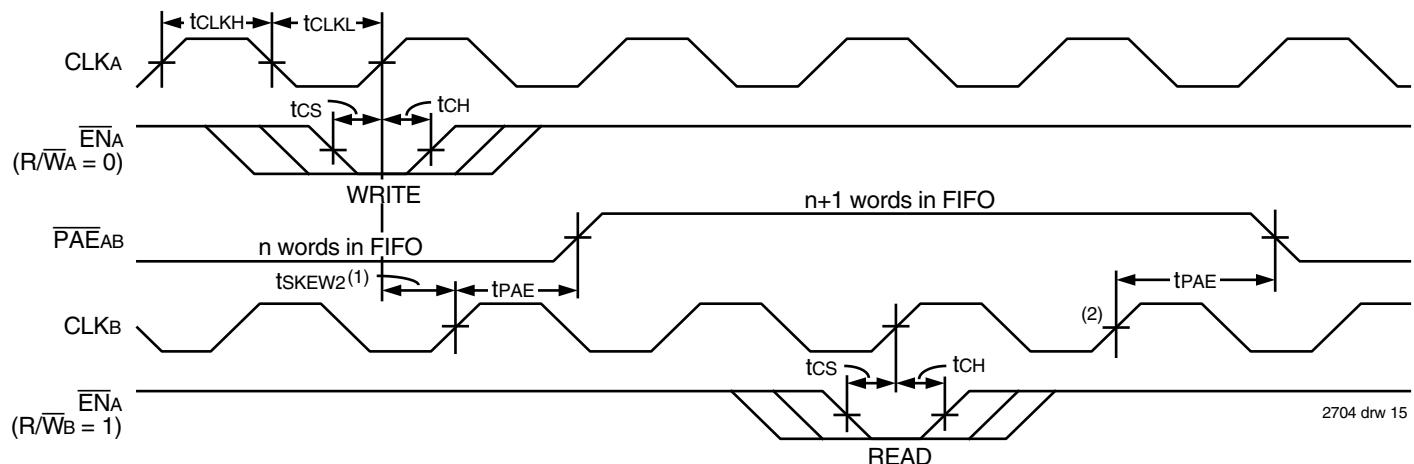
Figure 10. A-to-B Bypass Timing



NOTES:

1. When \overline{CS}_A is brought HIGH, A \rightarrow B Bypass mode will switch to FIFO mode on the following CLKA going LOW-to-HIGH.
2. After the bypass operation is completed, the \overline{BYP}_B goes from LOW-to-HIGH; this will reset all bypass flags.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

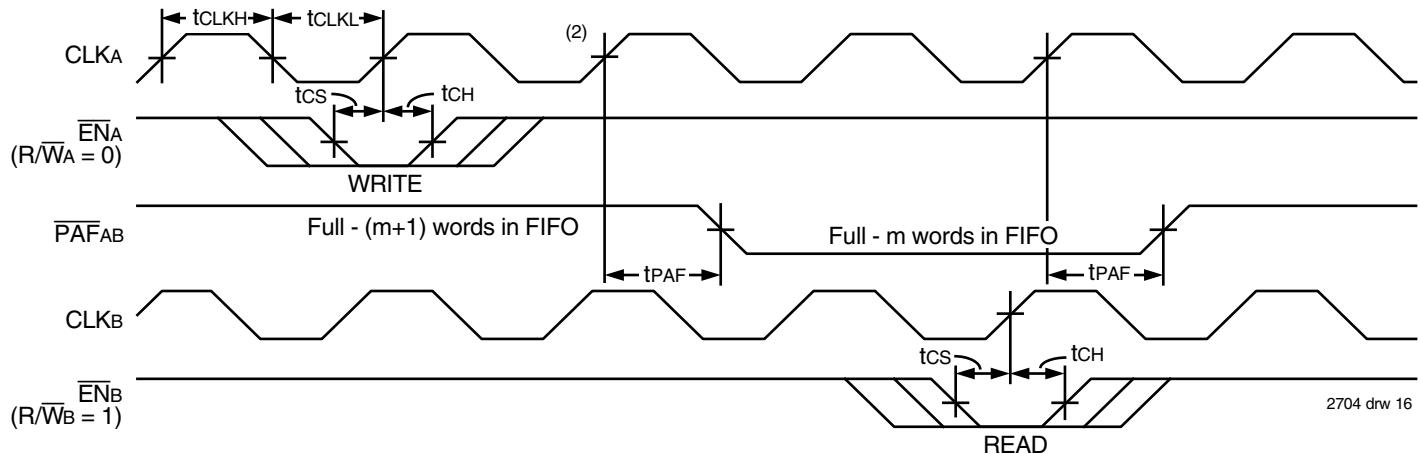
Figure 11. B \rightarrow A Bypass Timing



NOTES:

1. tskew2 is the minimum time between a rising CLKA edge and a rising CLKB edge for \overline{PAE}_{AB} to change during that clock cycle. If the time between the rising edge of CLKA and the rising edge of CLKB is less than tskew, then \overline{PAE}_{AB} may not go HIGH until the next CLKB rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n + 1) words in the FIFO when \overline{PAE} goes LOW.

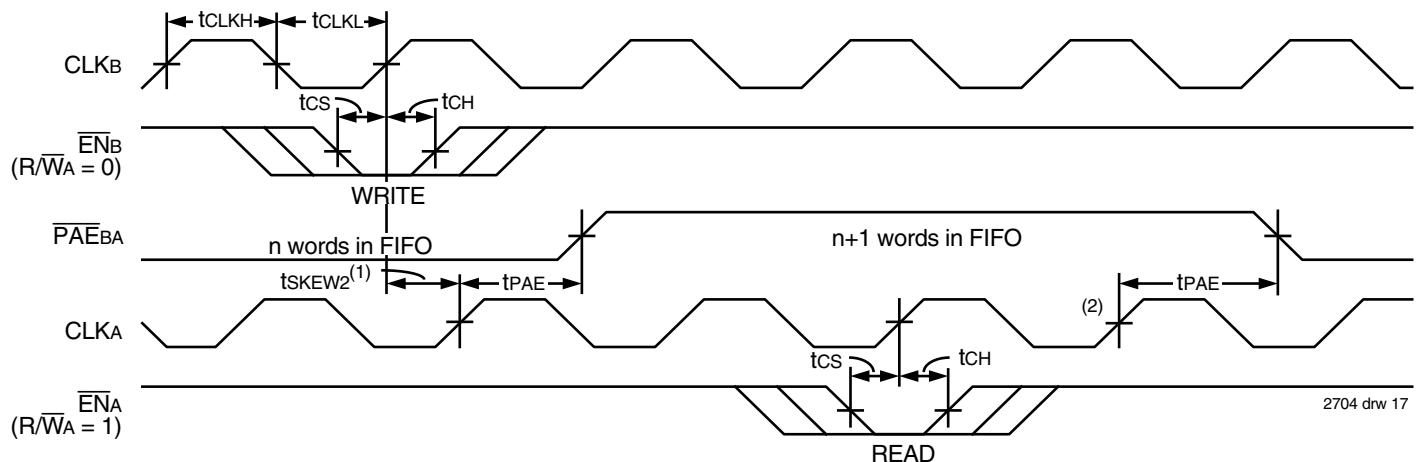
Figure 12. A→B Programmable Almost-Empty Flag Timing



NOTES:

1. tskew2 is the minimum time between a rising CLKB edge and a rising CLKA edge for \overline{PAF}_{AB} to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tskew, then \overline{PAF}_{AB} may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when \overline{PAF} goes LOW.

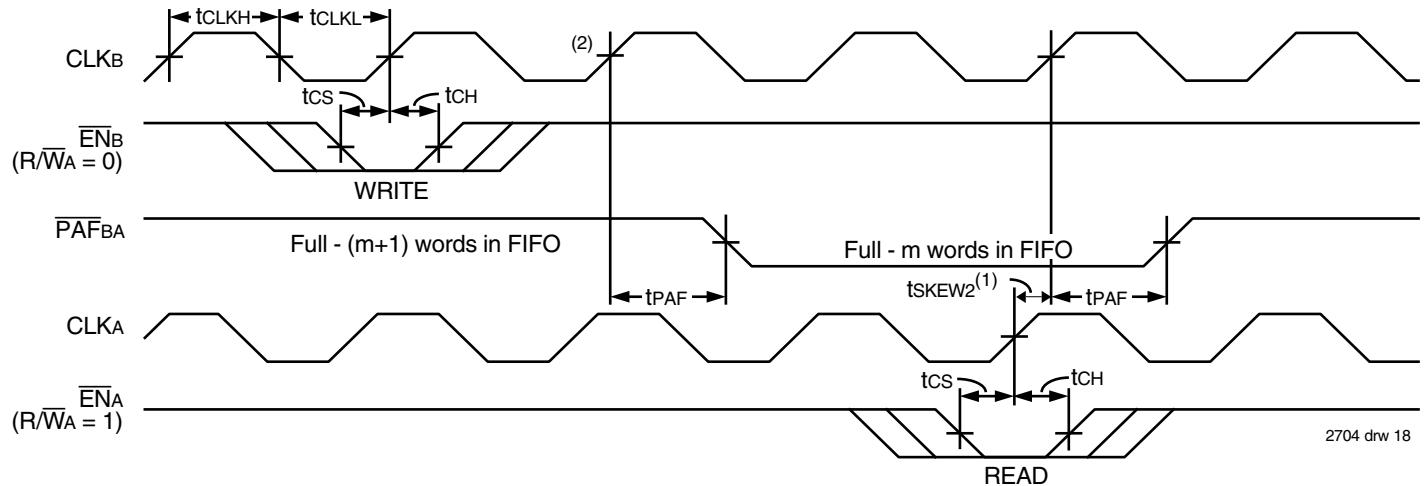
Figure 13. A→B Programmable Almost-Full Flag Timing



NOTES:

1. tsKEW2 is the minimum time between a rising CLK_B edge and a rising CLKA edge for PAE_{BA} to change during that clock cycle. If the time between the rising edge of CLK_B and the rising edge of CLKA is less than tsKEW2, then PAE_{BA} may not go HIGH until the next CLKA rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n - 1) words in the FIFO when PAE goes LOW.

Figure 14. B→A Programmable Almost-Empty Flag Timing

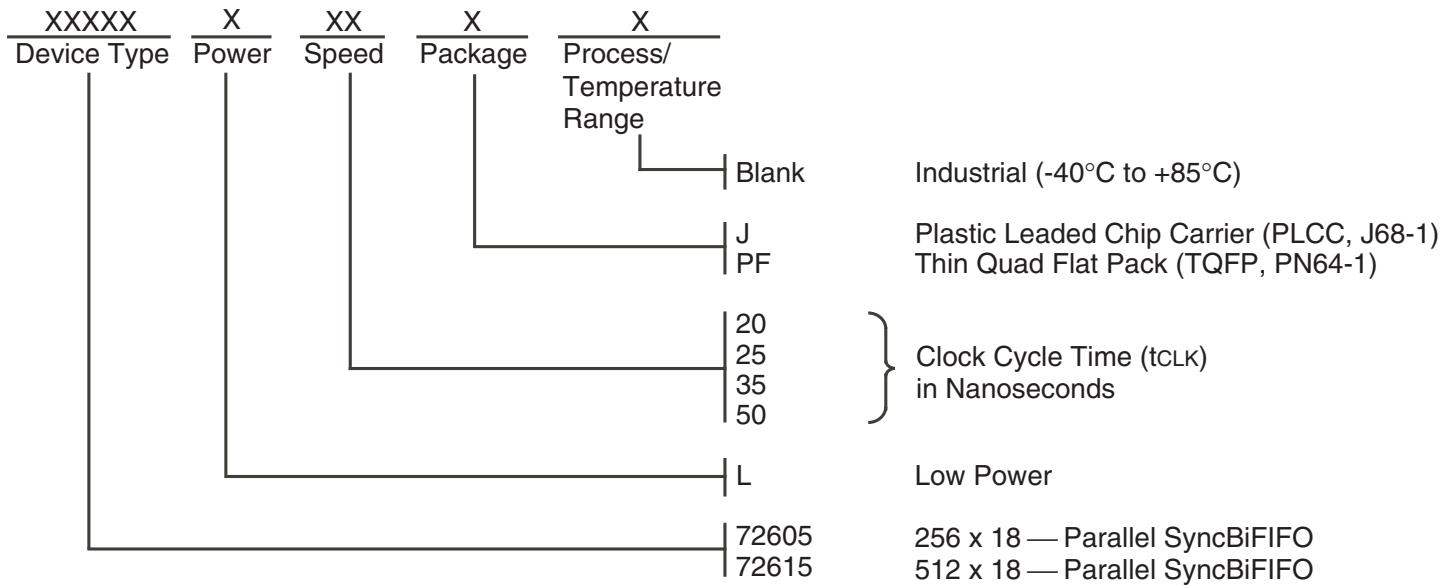


NOTES:

1. tsKEW2 is the minimum time between a rising CLK_B edge and a rising CLKA edge for PAF_{BA} to change during that clock cycle. If the time between the rising edge of CLK_B and the rising edge of CLKA is less than tsKEW2, then PAF_{BA} may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when PAF goes LOW.

Figure 15. B→A Programmable Almost-Full Flag Timing

ORDERING INFORMATION



2704 drw19

DATASHEET DOCUMENT HISTORY

11/02/2000	pgs. 1, 2, 3, 4, 16
04/08/2003	pg. 17.
02/08/2009	pgs. 1 and 17.
11/21/2014	PDN# CQ-14-08 issued. See IDT.com for PDN specifics.
09/06/2019	Datasheet changed to Obsolete Status.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.