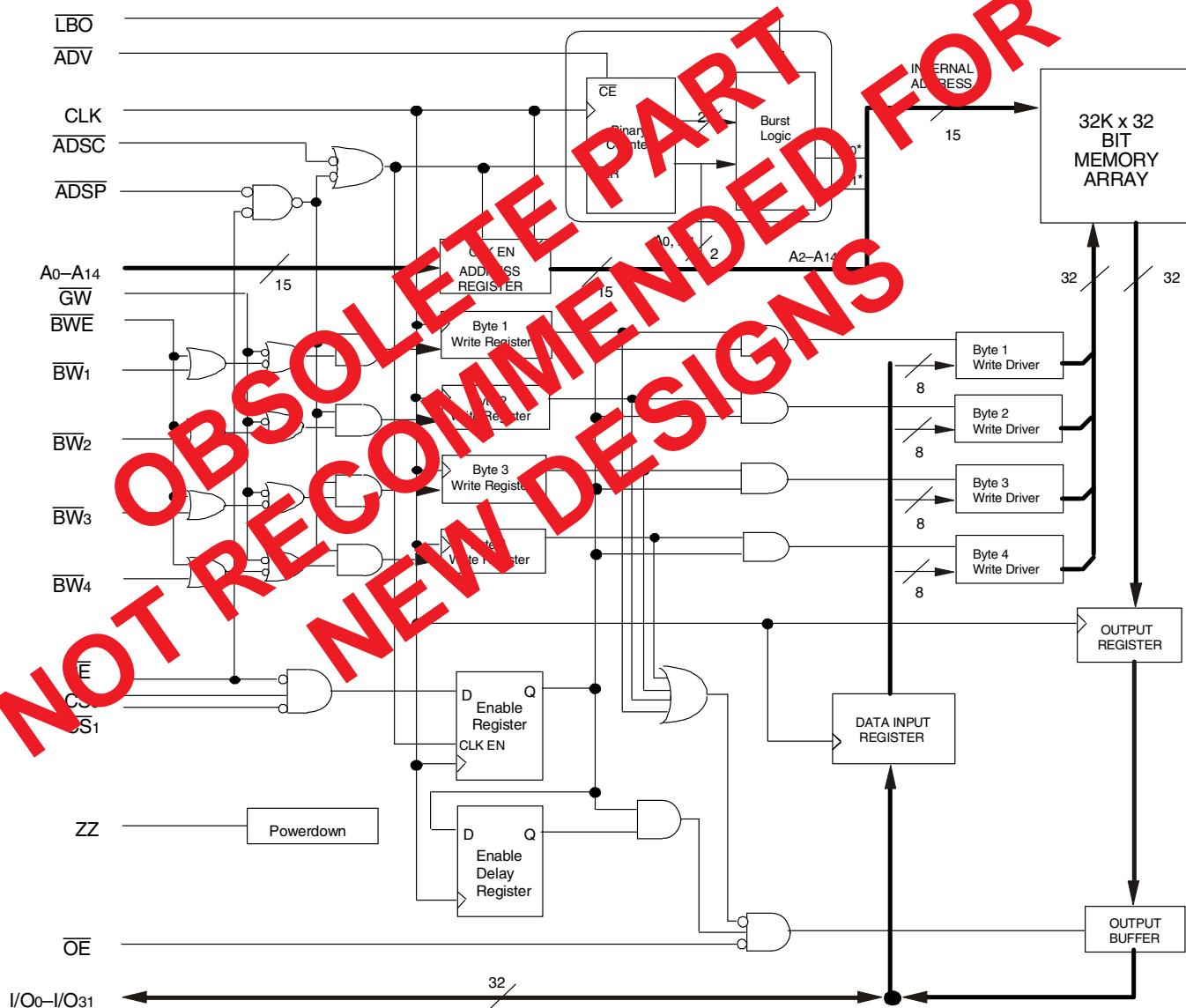


Features

- ♦ 32K x 32 memory configuration
- ♦ Supports high-performance system speed:
Commercial and Industrial:
 - 5ns Clock-to-Data Access (100MHz)
 - 6ns Clock-to-Data Access (83MHz)
- ♦ Single-cycle deselect functionality (Compatible with Micron Part # MT58LC32K32D7LG-XX)

- ♦ \overline{LBO} input selects interleaved or linear burst mode
- ♦ Self-timed write cycle with global write control (\overline{GW}), byte write enable (\overline{BWE}), and byte writes (\overline{BWx})
- ♦ Power down controlled by ZZ input
- ♦ Operates with a single 3.3V power supply (+10/-5%)
- ♦ Packaged in a JEDEC Standard 100-pin rectangular plastic thin quad flatpack (TQFP)
- ♦ Green parts available, see ordering information

Functional Block Diagram



3104 dw 01

OCTOBER 2014

Description

The IDT71V432 is a 3.3V high-speed 1,048,576-bit CacheRAM organized as 32K x 32 with full support of the Pentium™ and PowerPC™ processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 100 MHz.

The IDT71V432 CacheRAM contains write, data, address, and control registers. Internal logic allows the CacheRAM to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V432 can provide four cycles of data for a single address presented to the

CacheRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}=LOW$), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses will be defined by the internal burst counter and the \overline{LBO} input pin.

The IDT71V432 CacheRAM utilizes high-performance, high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

Pin Description Summary

A0-A14	Address Inputs	Input	Synchronous
\overline{CE}	Chip Enable	Input	Synchronous
$\overline{CS}_0, \overline{CS}_1$	Chips Selects	Input	Synchronous
\overline{OE}	Output Enable	Input	Asynchronous
\overline{GW}	Global Write Enable	Input	Synchronous
\overline{BWE}	Byte Write Enable	Input	Synchronous
$\overline{BW}_1, \overline{BW}_2, \overline{BW}_3, \overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
\overline{ADV}	Burst Address Advance	Input	Synchronous
\overline{ADSC}	Address Status (Cache Controller)	Input	Synchronous
\overline{ADSP}	Address Status (Processor)	Input	Synchronous
\overline{LBO}	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O ₀ -I/O ₃₁	Data Input/Output	I/O	Synchronous
V _{DD}	3.3V Power	Power	DC
V _{SS}	Ground	Ground	DC

3104tbl01

CacheRAM is a trademark of Integrated Device Technology.

Pentium processor is a trademark of Intel Corp.

PowerPC is a trademark of International Business Machines, Inc.

Pin Definitions⁽¹⁾

Symbol	Pin Function	I/O	Active	Description
A0-A14	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and ADSC Low or ADSP Low and CE Low.
ADSC	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. ADSC is an active LOW input that is used to load the address registers with new addresses. ADSC is NOT GATED by CE.
ADSP	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. ADSP is an active LOW input that is used to load the address registers with new addresses. ADSP is gated by CE.
ADV	Burst Address Advance	I	LOW	Synchronous Address Advance. ADV is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When this input is HIGH the burst counter is not incremented; that is, there is no address advance.
BWE	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs BW1-BW4. If BWE is LOW at the rising edge of CLK then BWx inputs are passed to the next stage in the circuit. A byte write can still be blocked if ADSP is LOW at the rising edge of CLK. If ADSP is HIGH and BWx is LOW at the rising edge of CLK then data will be written to the SRAM. If BWE is HIGH then the byte write inputs are blocked and only GW can initiate a write cycle.
BW1 - BW4	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. BW1 controls I/O(7:0), BW2 controls I/O(15:8), etc. Any active byte write causes all outputs to be disabled. ADSP LOW disables all byte writes. BW1-BW4 must meet specified setup and hold times with respect to CLK.
CE	Chip Enable	I	LOW	Synchronous chip enable. CE is used with CS0 and CS1 to enable the IDT71V432. CE also gates ADSP.
CLK	Clock	I	N/A	This is the clock input to the IDT71V432. All timing references for the device are made with respect to this input.
CS0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS0 is used with CE and CS1 to enable the chip.
CS1	Chip Select 1	I	LOW	Synchronous active LOW chip select. CS1 is used with CE and CS0 to enable the chip.
GW	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 8-bit data bytes when LOW on the rising edge of CLK. GW supercedes individual byte write enables.
I/O0-I/O31	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
LBO	Linear Burst Order	I	LOW	Asynchronous burst order selection DC input. When LBO is HIGH the Interleaved (Intel) burst sequence is selected. When LBO is LOW the Linear (PowerPC) burst sequence is selected. LBO is a static DC input and must not change state while the device is operating.
OE	Output Enable	I	LOW	Asynchronous output enable. When OE is LOW the data output drivers are enabled on the I/O pins. OE is gated internally by a delay circuit driven by CE, CS0, and CS1. In dual-bank mode, when the user is utilizing two banks of IDT71V432 and toggling back and forth between them using CE, the internal delay circuit delays the OE activation of the data output drivers by one cycle to prevent bus contention between the banks. When used in single bank mode CE, CS0, and CS1 are all tied active and there is no output enable delay. When OE is HIGH the I/O pins are in a high-impedance state.
VDD	Power Supply	N/A	N/A	3.3V power supply inputs.
Vss	Ground	N/A	N/A	Ground pins.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V432 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Value	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VDD+0.5	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

3104 tbl 05

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD and Input terminals only.
3. I/O terminals.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	VDD
Commercial	0°C to +70°C	0V	3.3V+10/-5%
Industrial	-40°C to +85°C	0V	3.3V+10/-5%

3104 tbl 03

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	3.135	3.3	3.63	V
Vss	Ground	0	0	0	V
VIH	Input High Voltage — Inputs	2.0	—	4.6 ⁽²⁾	V
VIH	Input High Voltage — I/O	2.0	—	VDD+0.3	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

3104 tbl 04

NOTES:

1. VIL (min) = -1.0V for pulse width less than tcyc/2, once per cycle.
2. VIH (max) = 6.0V for pulse width less than tcyc/2, once per cycle.

Capacitance

(TA = +25°C, f = 1.0MHz, TQFP package)

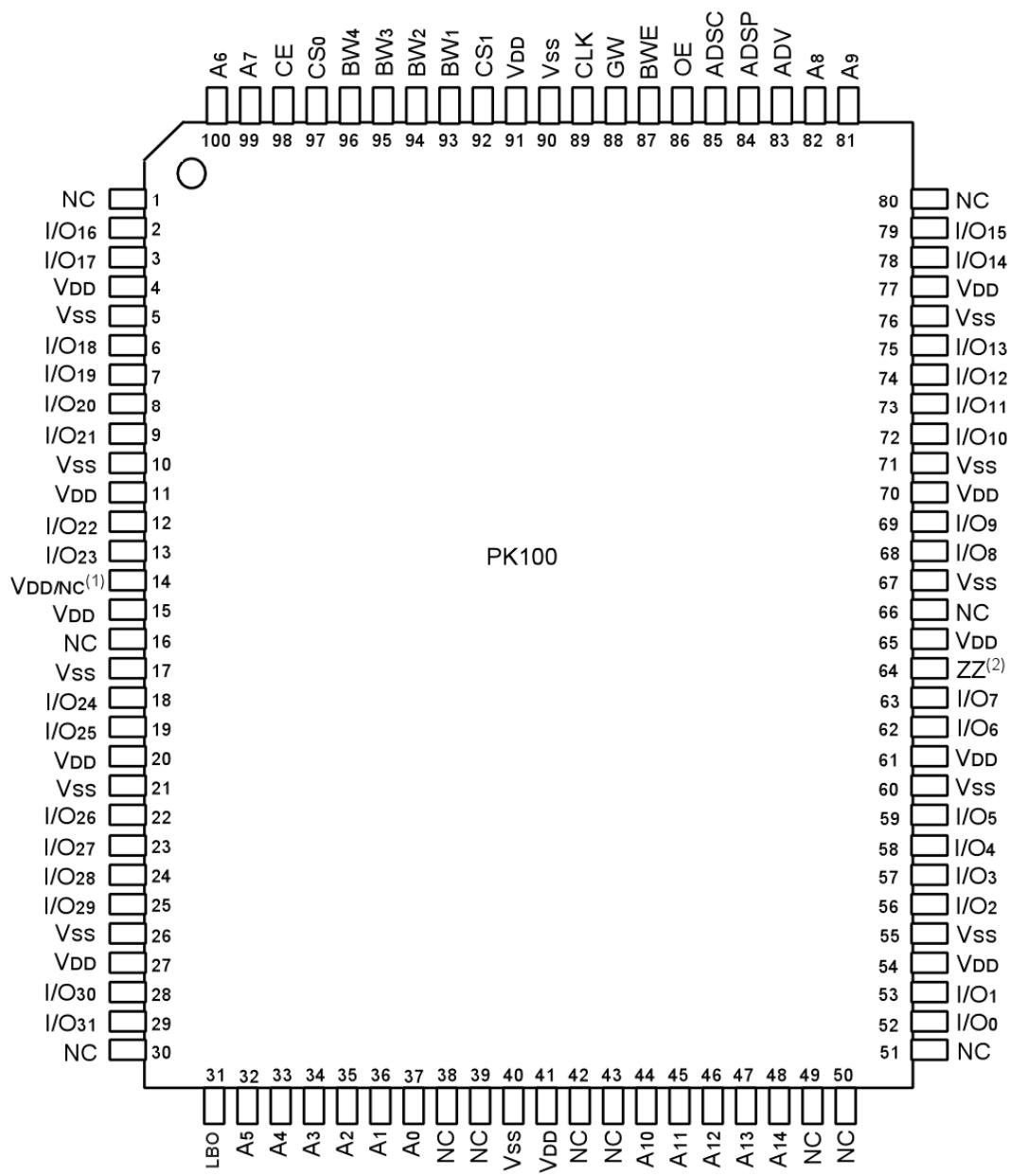
Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
C _{I/O}	I/O Capacitance	VOUT = 3dV	7	pF

3104 tbl 06

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Pin Configuration



3104 drw 02

Top View TQFP

NOTES:

1. Pin 14 can either be directly connected to VDD or not connected.
2. Pin 64 can be left unconnected and the device will always remain in active mode.

Synchronous Truth Table^(1,2)

Operation	Address Used	\overline{CE}	CS_0	CS_1	$ADSP$	$ADSC$	ADV	\overline{GW}	\overline{BWE}	\overline{BWx}	$\overline{OE}^{(3)}$	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	↑	Hi-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	↑	Dout
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	↑	Hi-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	↑	Dout
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	↑	Dout
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	↑	Hi-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	↑	Din
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	↑	Din
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	↑	Dout
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	↑	Dout
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	↑	Dout
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	Hi-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	↑	Dout
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	↑	Din
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	↑	Din
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	↑	Din
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	↑	Din
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	↑	Dout
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	↑	Dout
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	↑	Dout
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Hi-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Dout
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	↑	Hi-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	↑	Din
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	↑	Din
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	↑	Din
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	X	X	↑	Din

NOTES:

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. ZZ = LOW for this table.
3. \overline{OE} is an asynchronous input.

3104 tbl 07

Synchronous Write Function Truth Table⁽¹⁾

Operation	\overline{GW}	\overline{BWE}	\overline{BW}_1	\overline{BW}_2	\overline{BW}_3	\overline{BW}_4
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1 ⁽²⁾	H	L	L	H	H	H
Write Byte 2 ⁽²⁾	H	L	H	L	H	H
Write Byte 3 ⁽²⁾	H	L	H	H	L	H
Write Byte 4 ⁽²⁾	H	L	H	H	H	L

NOTES:

3104 tbl 08

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table⁽¹⁾

Operation ⁽²⁾	\overline{OE}	ZZ	I/O Status	Power
Read	L	L	Data Out (I/O ₀ - I/O ₃₁)	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z — Data In (I/O ₀ - I/O ₃₁)	Active
Deselected	X	L	High-Z	Standby
Sleep	X	H	High-Z	Sleep

NOTES:

3104 tbl 09

1. L = V_{IL} , H = V_{IH} , X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO} = V_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

NOTE:

3104 tbl 10

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO} = V_{SS}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

NOTE:

3104 tbl 11

1. Upon completion of the Burst sequence the counter wraps around to its initial state.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3V +10/-5\%$, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$ I_{L1} $	Input Leakage Current	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	5	μA
$ I_{L1} $	ZZ and $\overline{LB0}$ Input Leakage Current ⁽¹⁾	$V_{DD} = \text{Max.}, V_{IN} = 0V \text{ to } V_{DD}$	—	30	μA
$ I_{L0} $	Output Leakage Current	$\overline{CE} \geq V_{IH} \text{ or } \overline{OE} \geq V_{IH}, V_{OUT} = 0V \text{ to } V_{DD}, V_{DD} = \text{Max.}$	—	5	μA
V_{OL}	Output Low Voltage ($I/O_1 - I/O_31$)	$I_{OL} = 5\text{mA}, V_{DD} = \text{Min.}$	—	0.4	V
V_{OH}	Output High Voltage ($I/O_1 - I/O_31$)	$I_{OH} = -5\text{mA}, V_{DD} = \text{Min.}$	2.4	—	V

NOTE:

1. The $\overline{LB0}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

3104 tbl 12

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ ($V_{DD} = 3.3V +10/-5\%$, $V_{HD} = V_{DD} - 0.2V$, $V_{LD} = 0.2V$)

Symbol	Parameter	Test Conditions	IDT71V432S5		IDT71V432S6		Unit
			Com'l.	Ind.	Com'l.	Ind.	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$	200	200	180	180	mA
I_{SB}	Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX}^{(2)}$	65	65	60	60	mA
I_{SB1}	Full Standby Power Supply Current	Device Deselected, Outputs Open, $V_{DD} = \text{Max.}, V_{IN} \geq V_{HD} \text{ or } \leq V_{LD}, f = 0^{(2)}$	15	15	15	15	mA
I_{ZZ}	Full Sleep Mode Power Supply Current	$ZZ \geq V_{HD}, V_{DD} = \text{Max.}$	10	10	10	10	mA

3104 tbl 13a

NOTES:

1. All values are maximum guaranteed values.
2. At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{cyc}$ while $\overline{ADSC} = \text{LOW}$; $f=0$ means no input lines are changing.

AC Test Loads

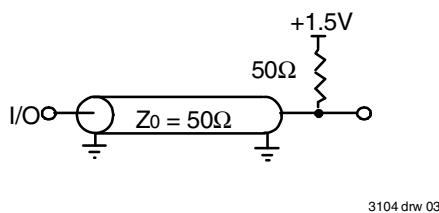
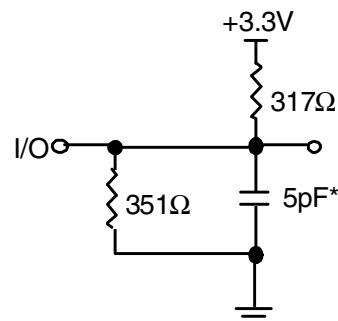


Figure 1. AC Test Load



* Including scope and jig capacitance.

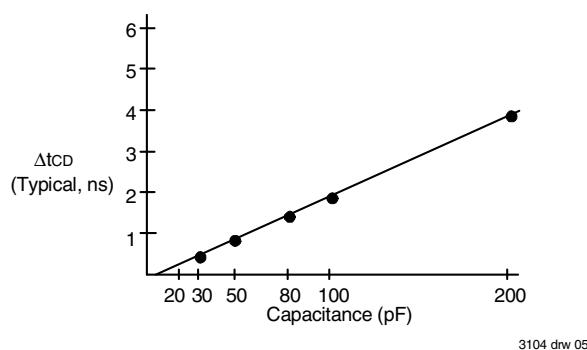
Figure 2. AC Test Load
(for t_{HD} , t_{CHZ} , $tolZ$, and t_{DC1})

Figure 3. Lumped Capacitive Load, Typical Derating

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3104 drw 14

AC Electrical Characteristics

($V_{DD} = 3.3V \pm 10\% / -5\%$, Commercial and Industrial Temperature Ranges)

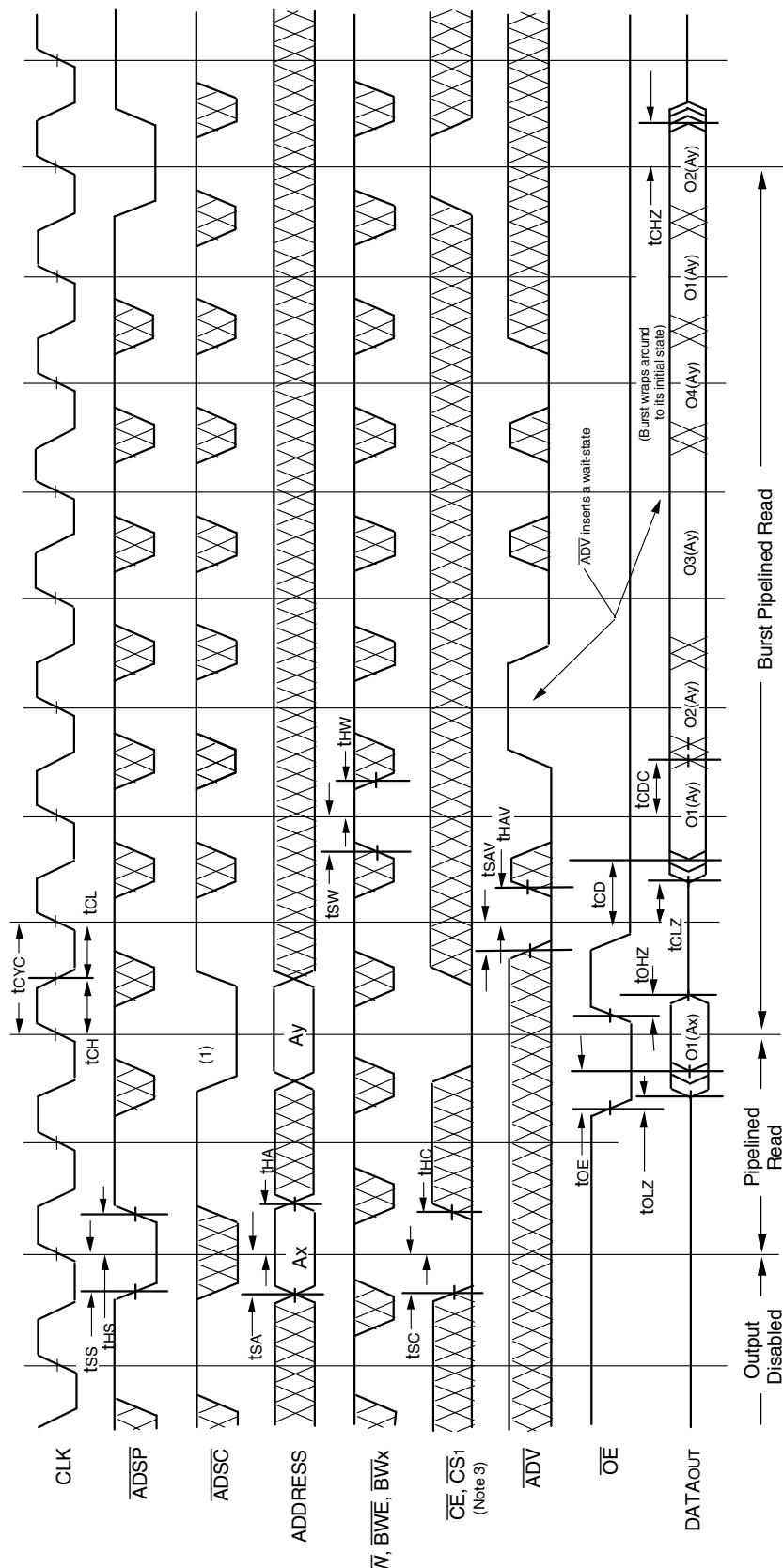
Symbol	Parameter	71V432S5		71V432S6		Unit
		Min.	Max.	Min.	Max.	
CLOCK PARAMETERS						
tcyc	Clock Cycle Time	10	—	12	—	ns
tch ⁽¹⁾	Clock High Pulse Width	4	—	4.5	—	ns
tcl ⁽¹⁾	Clock Low Pulse Width	4	—	4.5	—	ns
OUTPUT PARAMETERS						
tcd	Clock High to Valid Data	—	5	—	6	ns
tcdc	Clock High to Data Change	1.5	—	2	—	ns
tclz ⁽²⁾	Clock High to Output Active	0	—	0	—	ns
tchz ⁽²⁾	Clock High to Data High-Z	1.5	5	2	5	ns
toe	Output Enable Access Time	—	5	—	5	ns
tolz ⁽²⁾	Output Enable Low to Data Active	0	—	0	—	ns
tohz ⁽²⁾	Output Enable High to Data High-Z	—	4	—	5	ns
SETUP TIMES						
tSA	Address Setup Time	2.5	—	2.5	—	ns
tss	Address Status Setup Time	2.5	—	2.5	—	ns
tSD	Data in Setup Time	2.5	—	2.5	—	ns
tsw	Write Setup Time	2.5	—	2.5	—	ns
tSAV	Address Advance Setup Time	2.5	—	2.5	—	ns
tsc	Chip Enable/Select Setup Time	2.5	—	2.5	—	ns
HOLD TIMES						
tHA	Address Hold Time	0.5	—	0.5	—	ns
tHS	Address Status Hold Time	0.5	—	0.5	—	ns
tHD	Data In Hold Time	0.5	—	0.5	—	ns
tHW	Write Hold Time	0.5	—	0.5	—	ns
tHAV	Address Advance Hold Time	0.5	—	0.5	—	ns
tHC	Chip Enable/Select Hold Time	0.5	—	0.5	—	ns
SLEEP MODE AND CONFIGURATION PARAMETERS						
tZZPW	ZZ Pulse Width	100	—	100	—	ns
tZZR ⁽³⁾	ZZ Recovery Time	100	—	100	—	ns
tCFG ⁽⁴⁾	Configuration Set-up Time	40	—	50	—	ns

3104 tbl 15a

NOTES:

1. Measured as HIGH above 2.0V and LOW below 0.8V.
2. Transition is measured $\pm 200\text{mV}$ from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. tcfg is the minimum time required to configure the device based on the $\overline{\text{LBO}}$ input. $\overline{\text{LBO}}$ is a static input and must not change during normal operation.

Timing Waveform of Pipelined Read Cycle^(1,2)



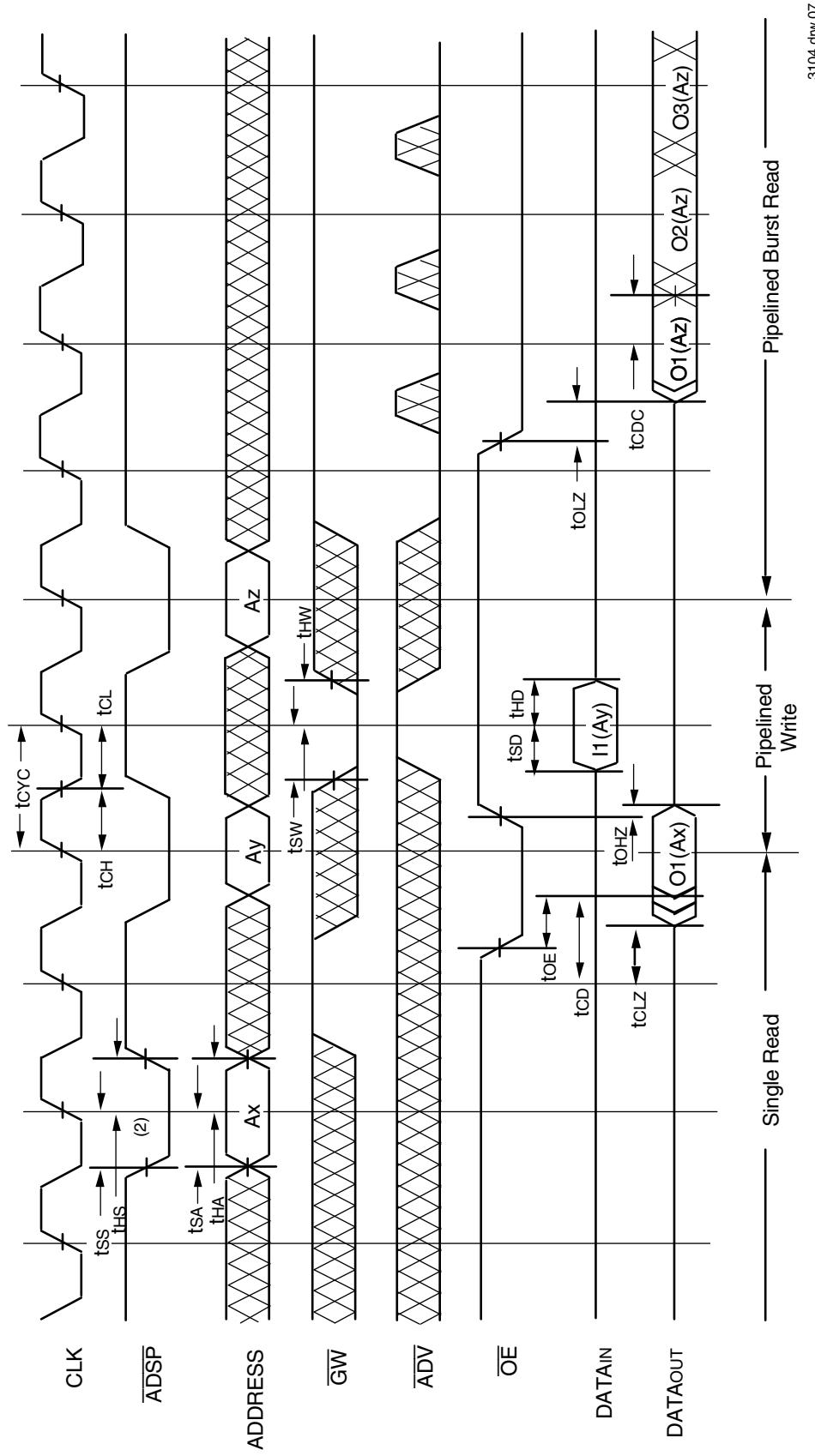
NOTES.

1. 01 (A₀) represents the first output from the external address Ax. 01 (A₀) represents the first output from the external address Ay. 02 (A₀) represents the next output data in the burst sequence of the base address Ay, etc. where A₀ and A₁ are advancing for the four word burst in the sequence defined by the state of the $\overline{[BO]}$ input.

2. ZZ input is LOW and $\overline{[BO]}$ is Dont Care for this cycle.

3. CS0 timing transitions are identical but inverted in the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

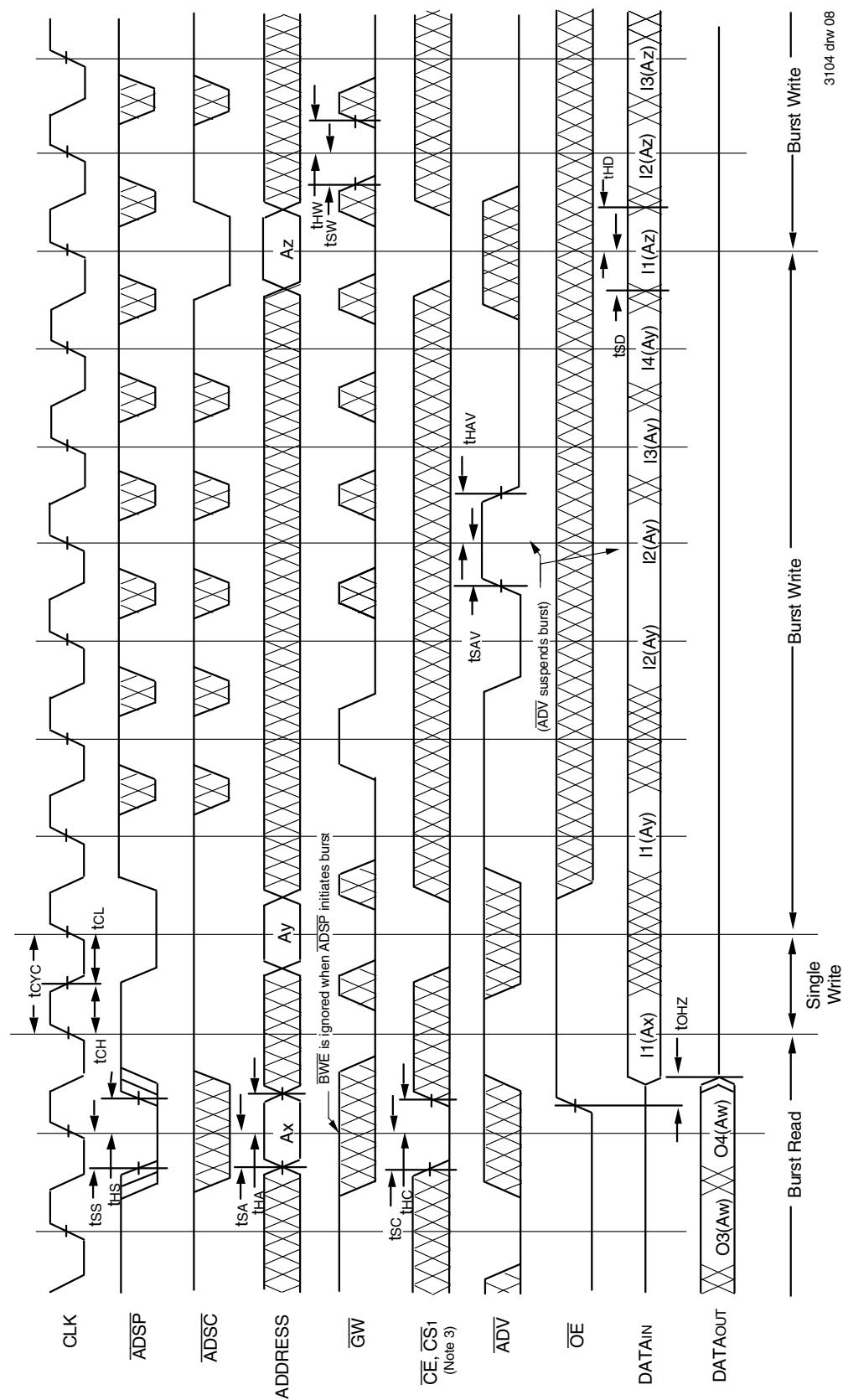
3104 drw 06

Timing Waveform of Combined Pipelined Read and Write Cycles^(1,2,3)

NOTES:

1. Device is selected through entire cycle; \overline{OE} and $\overline{CS_1}$ are LOW, CS_0 is HIGH.
2. ZZ input is LOW and \overline{LBIO} is Don't Care for this cycle.
3. $O1(Ax)$ represents the first output from the external address Ax . $O1(Ay)$ represents the first output from the external address Ay . $O2(Az)$ represents the second output from the external address Az . $O3(Az)$ represents the third output from the external address Az . $O1(Az)$ represents the first output from the external address Az . $O2(Az)$ represents the second output from the external address Az . $O3(Az)$ represents the third output from the external address Az . $O1(Az)$ represents the first output from the external address Az . $O2(Az)$ represents the second output from the external address Az . $O3(Az)$ represents the third output from the external address Az .

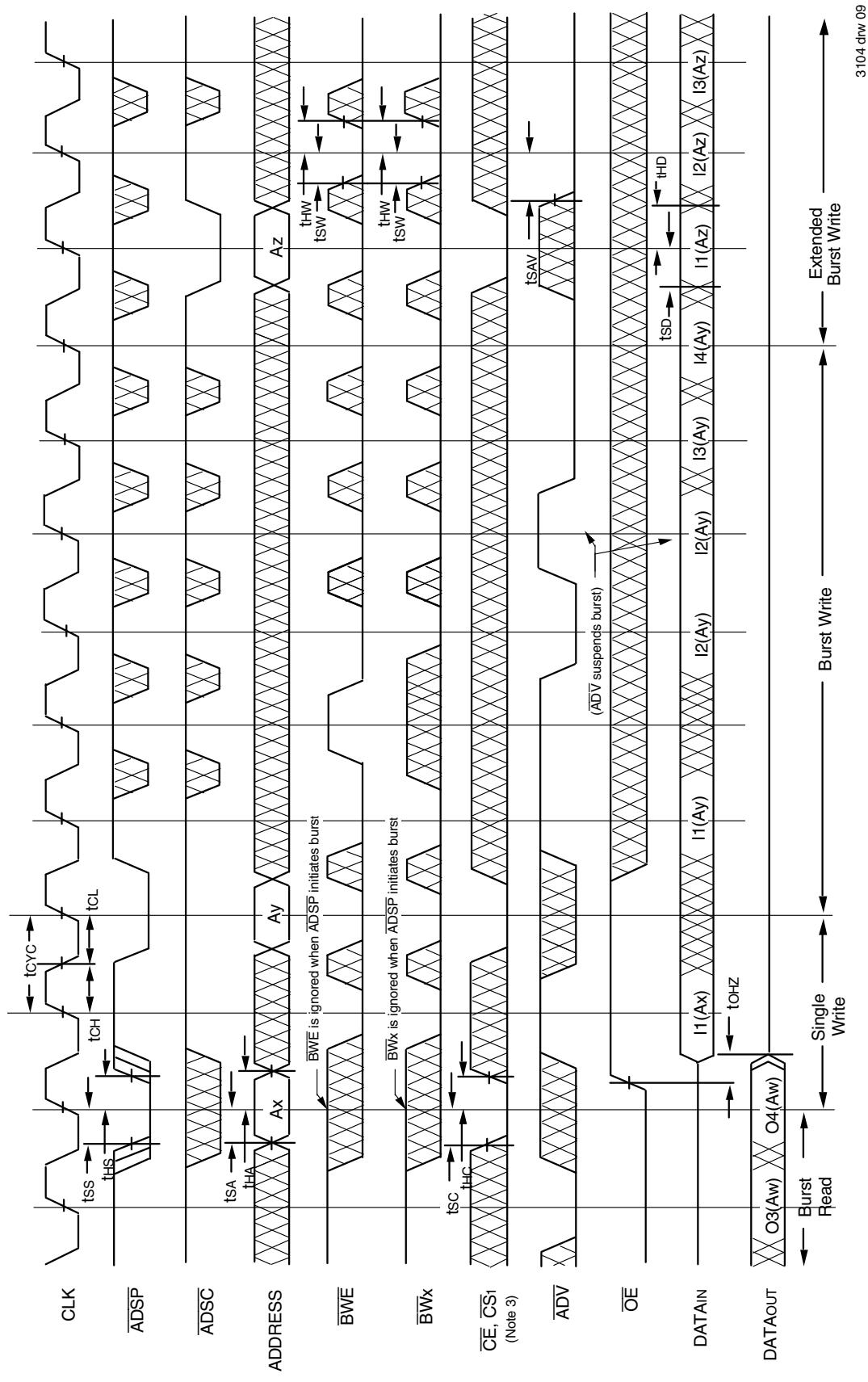
3104 drw 07

Timing Waveform of Write Cycle No. 1 — **GW** Controlled^(1,2,3)

NOTES:

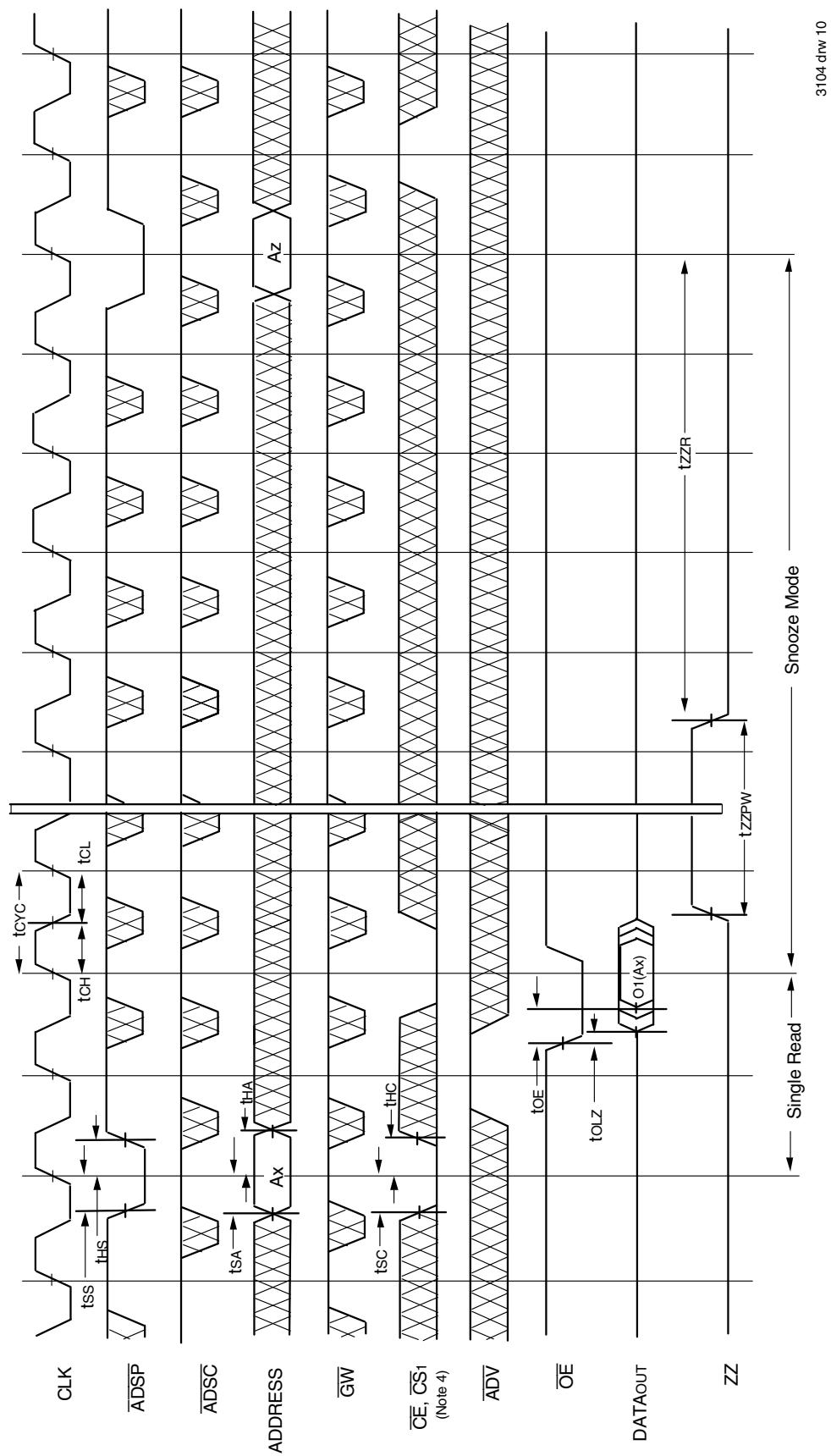
1. ZZ input is LOW, \overline{BWE} is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. 11(Ax) represents the first input from the external address Ay. 12(Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input 12(Ay) this data is valid for two cycles because \overline{ADV} is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the \overline{OE} and $\overline{CS1}$ signals. For example, when \overline{OE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Write Cycle No. 2 – Byte Controlled^(1,2,3)



NOTES:

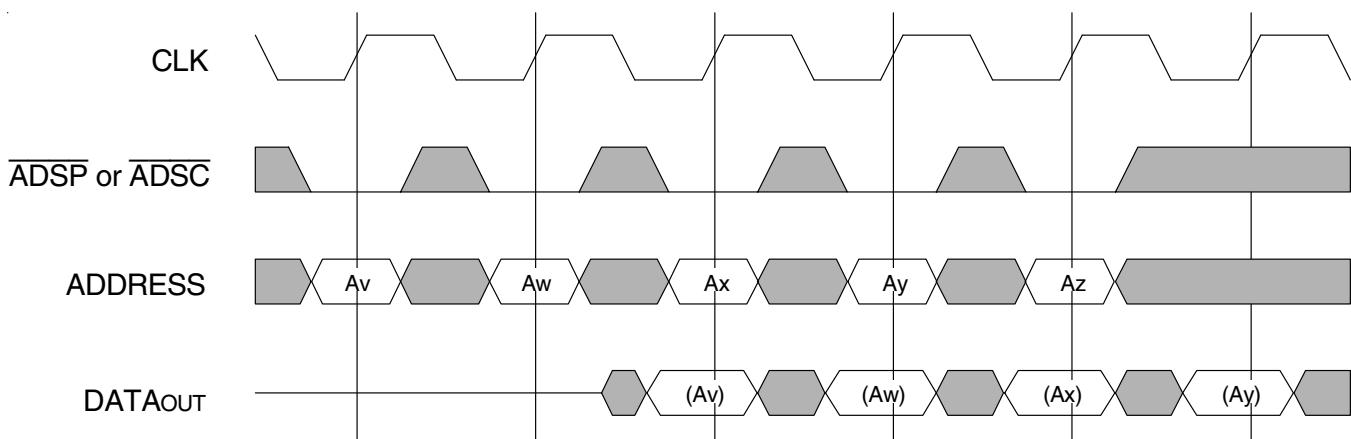
1. ZZ input is LOW, \overline{GW} is HIGH, and \overline{LBO} is Don't Care for this cycle.
2. O4(Aw) represents the final output data in the burst sequence of the base address Aw. 11(Ay) represents the first input from the external address Ay; 12(Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the \overline{LBO} input. In the case of input 12(Ay) this data is valid for two cycles because \overline{ADV} is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes^(1,2,3)

NOTES:

1. Device must power up in deselected Mode.
2. $\overline{LB0}$ input is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS0 timing transitions are identical but inverted to the \overline{CE} and $\overline{CS1}$ signals. For example, when \overline{CE} and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Non-Burst Read Cycle Timing Waveform^(1,2,3,4)

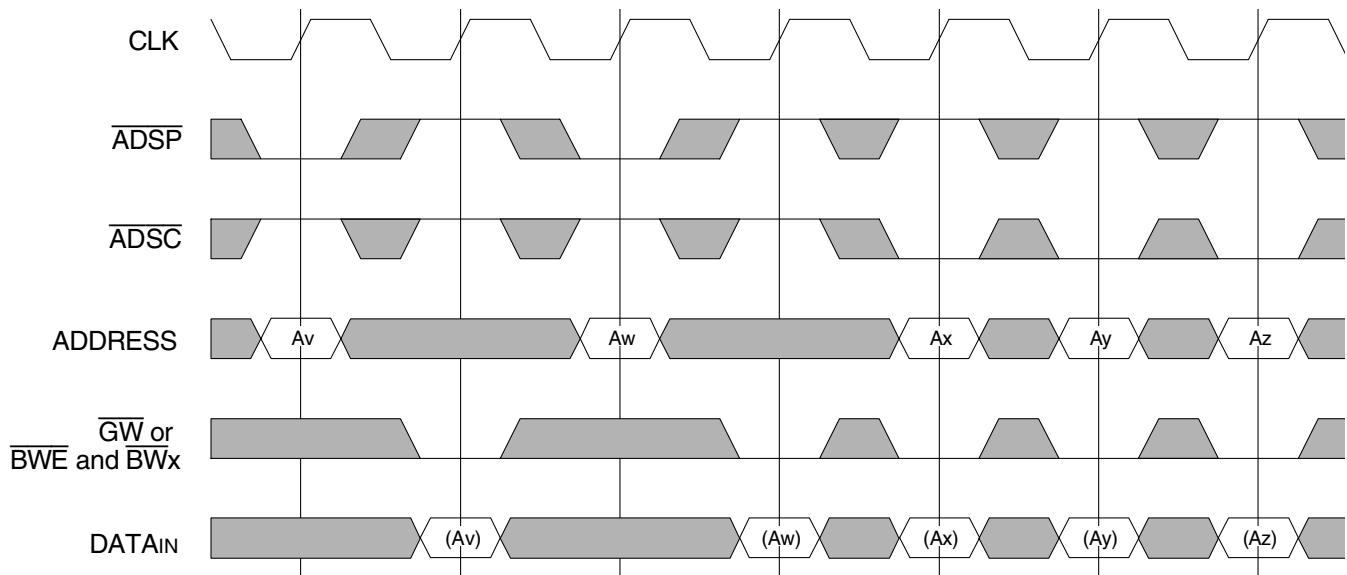


NOTES:

1. ZZ, CE, CS₁, and OE are LOW for this cycle.
2. ADV, GW, BWE, BW_x, and CS₀ are HIGH for this cycle.
3. (Ax) represents the data for address Ax, etc.
4. For read cycles, ADSP and ADSC function identically and are therefore interchangeable.

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Non-Burst Write Cycle Timing Waveform^(1,2,3,4)

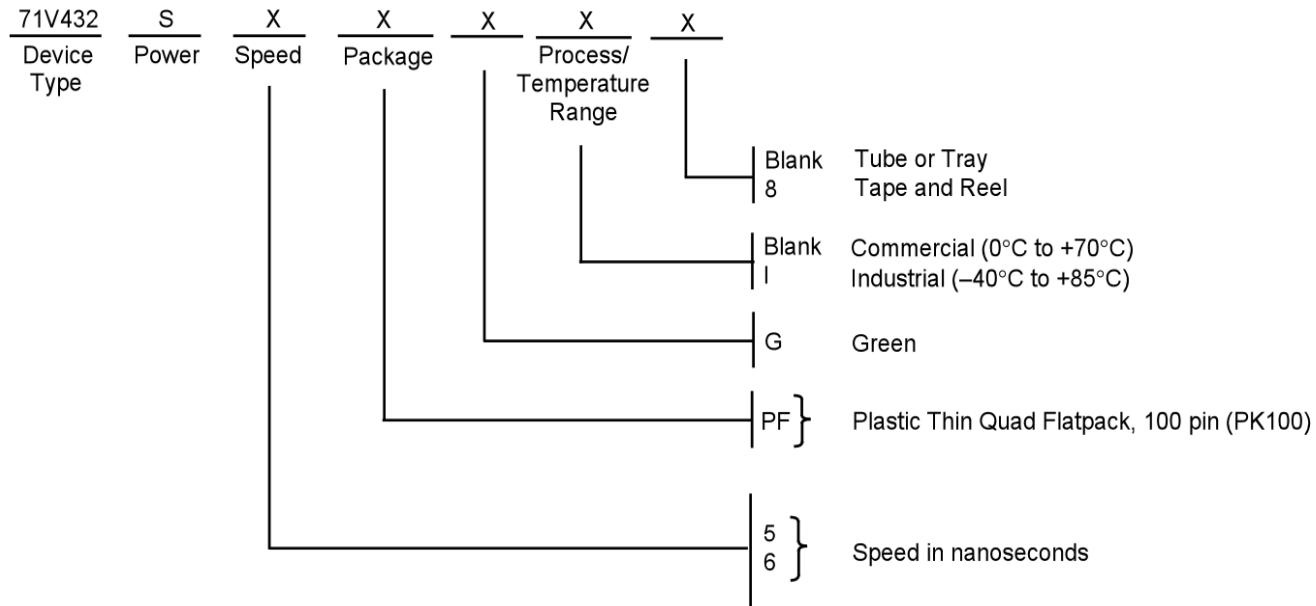


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NOTES:

1. ZZ, CE and CS₁ are LOW for this cycle.
2. ADV, OE and CS₀ are HIGH for this cycle.
3. (Ax) represents the data for address Ax, etc.
4. For write cycles, ADSP and ADSC have different limitations.

Ordering Information



PART NUMBER	SPEED IN MEGAHERTZ	t _{CD} PARAMETER	CLOCK CYCLE TIME
71V432S5PF	100 MHz	5 ns	10 ns
71V432S6PF	83 MHz	6 ns	12 ns

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Datasheet Document History

9/10/99		Updated to new format
	Pg. 3-5	Adjusted page layout, added extra page
	Pg. 5	Added notes to pin configuration
	Pg. 11-14	Revised notes
	Pg. 17	Added Datasheet Document History
03/09/00	Pg. 1, 4, 8, 9, 16	Added Industrial temperature range offerings
04/04/00	Pg. 16	Added 100pinTQFP package Diagram Outline
08/09/00		Added "Not recommended for new designs"
08/17/01		Removed "Not recommended for new designs" from the background on the datasheet
03/31/05	Pg. 17	Added RoHS "Restricted Hazardous Substance Device" to ordering information
08/01/14	Pg. 1-3	Moved the FBD, the pin description and pin definition tables to pages 1 - 3 respectively to align the datasheet reading flow to that of our other established datasheets
	Pg. 17	In the Ordering Information, Tape & Reel added & RoHS designation changed to Green
10/03/14	Pg. 1	Removed <i>7ns Clock-to-Data Access (66MHz)</i> , and added green availability in Features
	Pg. 1-2	Moved notes regarding IDT's use of the CacheRAM, the Pentium processor & the PowerPC terminology
	Pg. 2	Removed the reference to IDT with regards to the CMOS process
	Pg. 5	The package code PK100-1 changed to PK100 to match standard package codes
	Pg. 8	Removed IDT71V432S7 speed grade offering in the DC Chars table
	Pg. 9	Removed 71V432S7 speed grade offering in the AC Chars table
	Pg. 16	Removed TQFP Package Diagram Outline
		In the Ordering Information, PK100-1 package code changed to PK100 and 7ns speed grade was removed
	Pg. 17	Updated Customer's SRAM Tech Support phone number and email address
03/16/22		71V432 Datasheet changed to Obsolete status



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