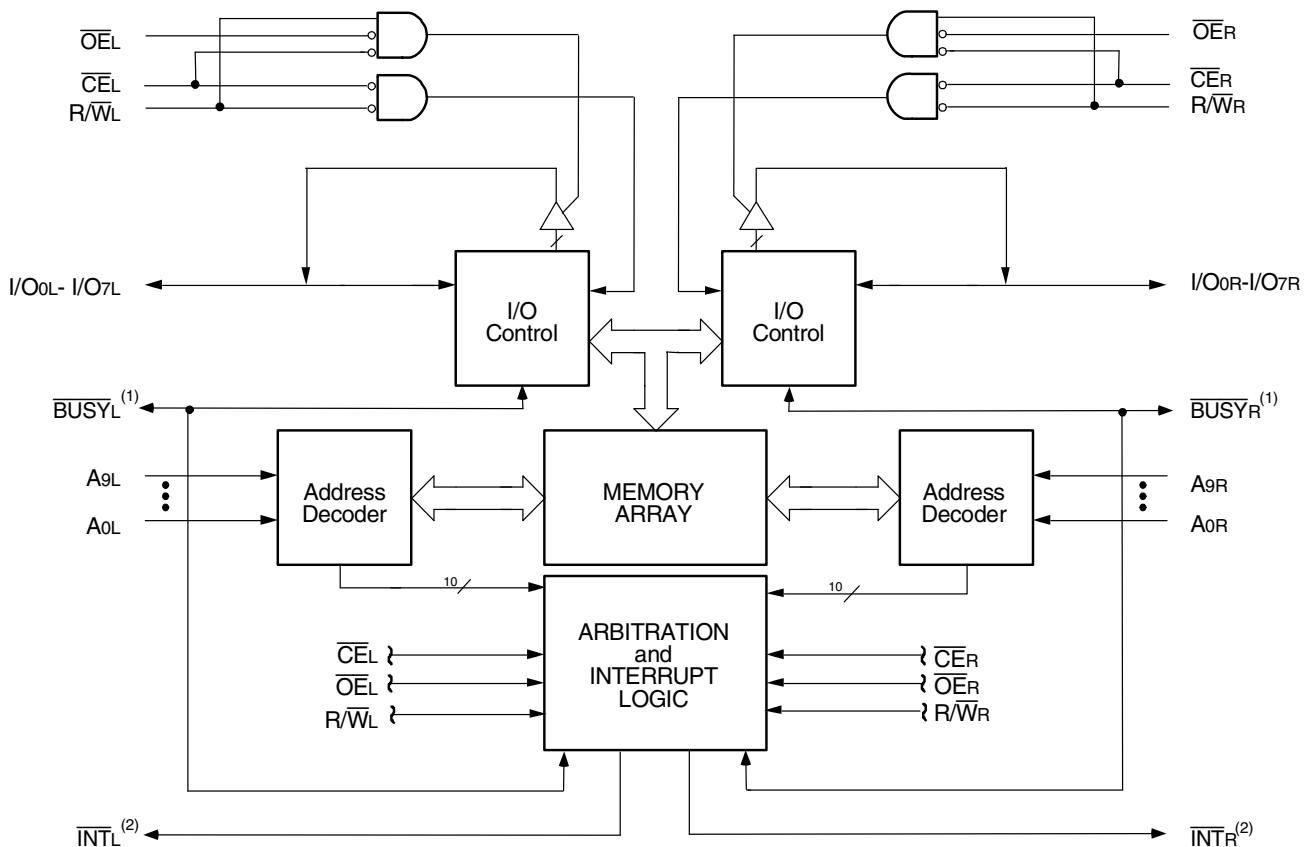


### Features

- ◆ High-speed access
  - Commercial: 25/55ns (max.)
  - Industrial 35ns (max.)
- ◆ Low-power operation
  - IDT71V30S  
Active: 375mW (typ.)  
Standby: 5mW (typ.)
  - IDT71V30L  
Active: 375mW (typ.)  
Standby: 1mW (typ.)
- ◆ On-chip port arbitration logic
- ◆ Interrupt flags for port-to-port communication
- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation, 2V data retention (L Only)
- ◆ TTL-compatible, single 3.3V ±0.3V power supply
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

### Functional Block Diagram



3741 drw 01

#### NOTES:

1. IDT71V30:  $\overline{\text{BUSY}}$  outputs are non-tristatable push-pulls.
2.  $\overline{\text{INT}}$  outputs are non-tristatable push-pull output structure.

### Description

The IDT71V30 is a high-speed 1K x 8 Dual-Port Static RAM. The IDT71V30 is designed to be used as a stand-alone 8-bit Dual-Port SRAM.

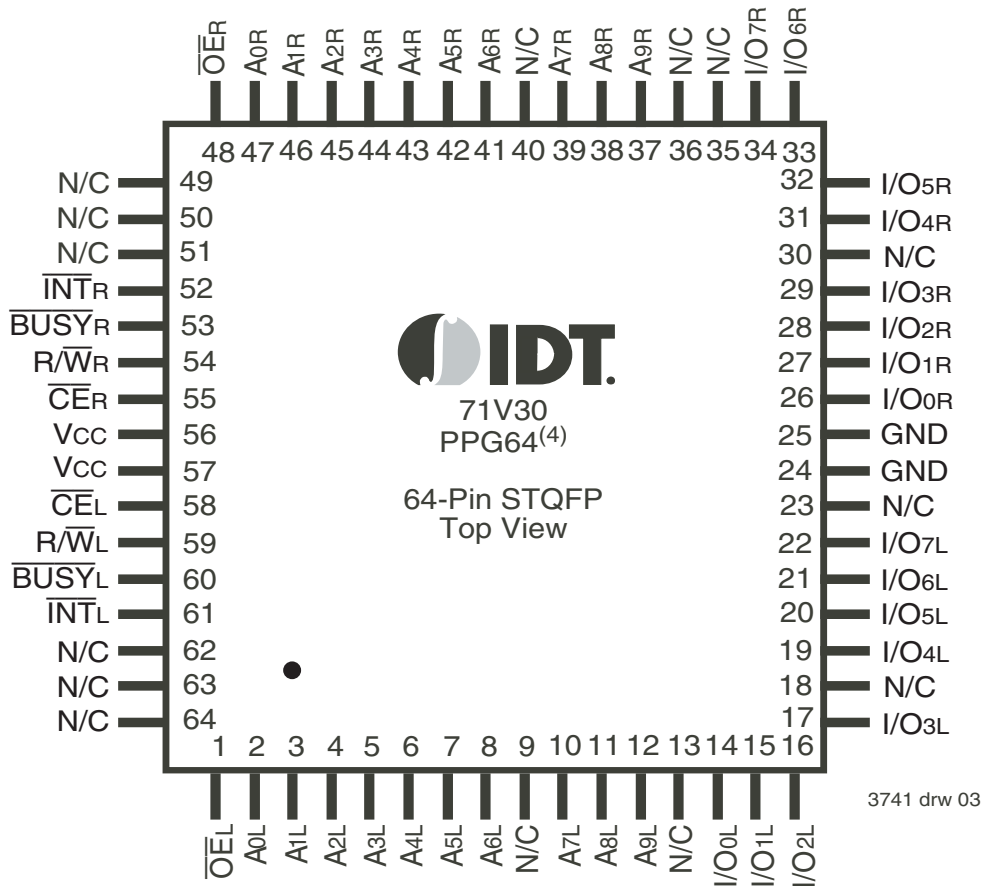
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power

down feature, controlled by  $\overline{CE}$ , permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 375mW of power. Low-power (L) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71V30 devices are packaged in 64-pin STQFPs.

### Pin Configurations<sup>(1,2,3)</sup>



3741 drw 03

**NOTES:**

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Com'l & Ind	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.60	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub> <sup>(3)</sup>	Junction Temperature	+150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

**NOTES:**

3741 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 0.3V.
- This is the absolute maximum junction temperature for the device. No DC Bias.

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>CC</sub> +0.3V	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

3741 tbl 02

**NOTE:**

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 20ns.

### Maximum Operating Temperature and Supply Voltage<sup>(1,2)</sup>

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	3.3V ± 0.3
Industrial	-40°C to +85°C	0V	3.3V ± 0.3

3741 tbl 03

**NOTES:**

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.
- Industrial temperature: for specific speeds, packages and powers, contact your sales office.

### Capacitance<sup>(1)</sup> (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

3741 tbl 04

**NOTES:**

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>CC</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	71V30S		71V30L		Unit
			Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ , V <sub>OUT</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
V <sub>OL</sub>	Output Low Voltage (I/O <sub>0</sub> -I/O <sub>7</sub> )	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	V

**NOTE:**

- At V<sub>CC</sub> ≤ 2.0V input leakages are undefined.

3741 tbl 05

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1,6,7)</sup> ( $V_{CC} = 3.3V \pm 0.3V$ )

Symbol	Parameter	Test Condition	Version	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit	
				Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.		
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	CE <sub>L</sub> and CE <sub>R</sub> = V <sub>IL</sub> , Outputs Disabled f = f <sub>MAX</sub> <sup>(3)</sup>	COM'L	S	75	150	75	145	75	135	mA
				L	75	120	75	115	75	105	
			IND	S	—	—	—	—	—	—	
				L	—	—	75	145	—	—	
I <sub>SB1</sub>	Standby Current (Both Ports - TTL Level Inputs)	CE <sub>L</sub> and CE <sub>R</sub> = V <sub>IL</sub> , f = f <sub>MAX</sub> <sup>(3)</sup>	COM'L	S	20	50	20	50	20	50	mA
				L	20	35	20	35	20	35	
			IND	S	—	—	—	—	—	—	
				L	—	—	20	50	—	—	
I <sub>SB2</sub>	Standby Current (One Port - TTL Level Inputs)	CE <sup>'A'</sup> = V <sub>IL</sub> and CE <sup>'B'</sup> = V <sub>IH</sub> <sup>(5)</sup> Active Port Outputs Disabled, f=f <sub>MAX</sub> <sup>(3)</sup>	COM'L	S	30	105	30	100	30	90	mA
				L	30	75	30	70	30	60	
			IND	S	—	—	—	—	—	—	
				L	—	—	30	100	—	—	
I <sub>SB3</sub>	Full Standby Current (Both Ports - CMOS Level Inputs)	CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0 <sup>(4)</sup>	COM'L	S	1.0	5.0	1.0	5.0	1.0	5.0	mA
				L	0.2	3.0	0.2	3.0	0.2	3.0	
			IND	S	—	—	—	—	—	—	
				L	—	—	1.0	5.0	—	—	
I <sub>SB4</sub>	Full Standby Current (One Port - CMOS Level Inputs)	CE <sup>'A'</sup> ≤ 0.2V and CE <sup>'B'</sup> ≥ V <sub>CC</sub> - 0.2V <sup>(5)</sup> V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V Active Port Outputs Disabled f=f <sub>MAX</sub> <sup>(3)</sup>	COM'L	S	30	90	30	85	30	75	mA
				L	30	75	30	70	30	60	
			IND	S	—	—	—	—	—	—	
				L	—	—	30	85	—	—	

3741 tbl 06

NOTES:

- 'X' in part number indicates power rating (S or L)
- V<sub>CC</sub> = 3.3V, T<sub>A</sub> = +25°C, and are not production tested. I<sub>CCDC</sub> = 70mA (Typ.)
- At f = f<sub>MAX</sub>, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t<sub>RC</sub>.
- f = 0 means no address or control lines change.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- Refer to chip enable Truth Table I.
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

Data Retention Characteristics (L Version Only)

Symbol	Parameter	Test Condition	71V30L			Unit	
			Min.	Typ. <sup>(1)</sup>	Max.		
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	V <sub>CC</sub> = 2V, $\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	2.0	—	—	V	
I <sub>CCDR</sub>	Data Retention Current		Ind.	—	100	1000	μA
			Com'l.	—	100	500	
t <sub>CDR</sub> <sup>(3)</sup>	Chip Deselect to Data Retention Time		0	—	—	ns	
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	ns	

3741 tbl 07

NOTES:

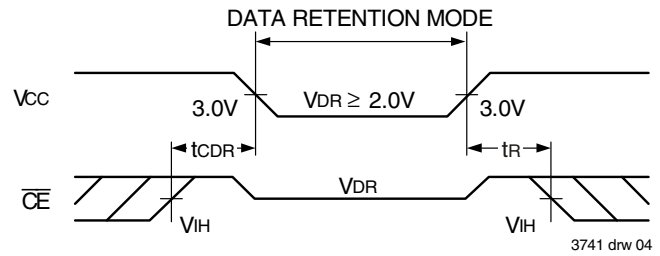
- V<sub>CC</sub> = 2V, T<sub>A</sub> = +25°C, and is not production tested.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed by device characterization but not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

3741 tbl 08

Data Retention Waveform



3741 drw 04

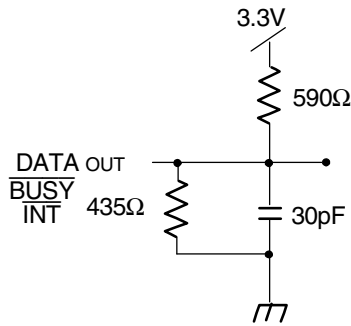
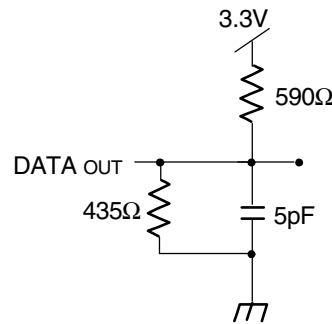


Figure 1. AC Output Test Load



3741 drw 05

Figure 2. Output Test Load  
(For tHZ, tLZ, tWZ and tOW)

\* Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(3,4)</sup>

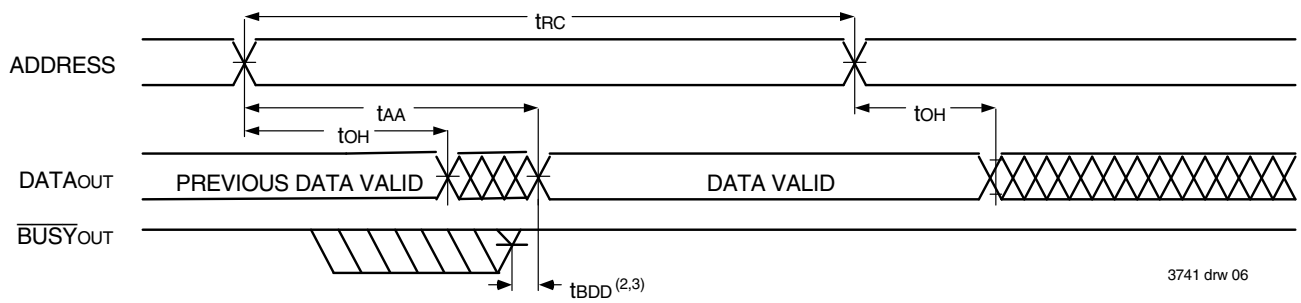
Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	12	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time <sup>(1,2)</sup>	0	—	0	—	0	—	ns
tHZ	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	30	ns
tPU	Chip Enable to Power Up Time <sup>(2)</sup>	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time <sup>(2)</sup>	—	50	—	50	—	50	ns

3741 tbl 09

NOTES:

1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (S or L).
4. Industrial temperature: for specific speeds, packages and power contact your sales office.

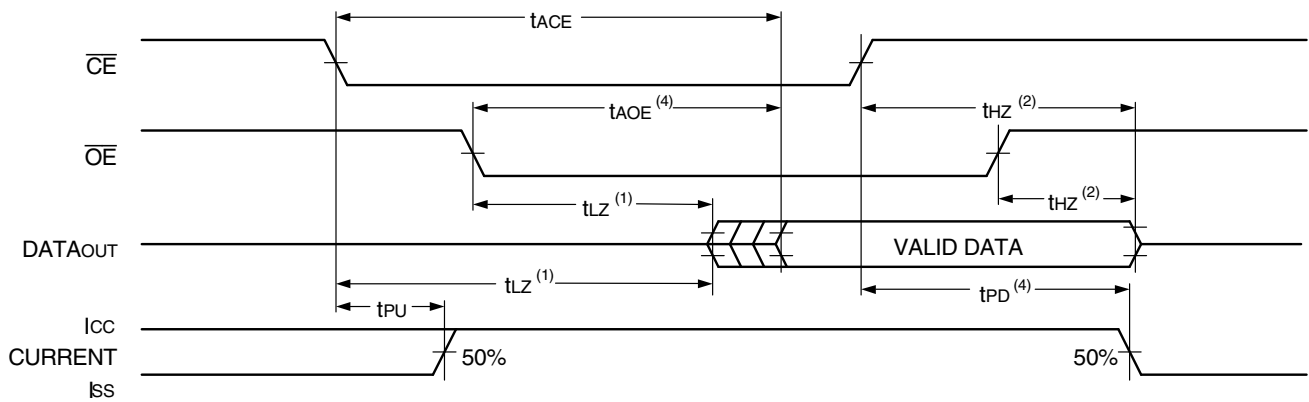
Timing Waveform of Read Cycle No. 1, Either Side<sup>(1)</sup>



NOTES:

1.  $R/\bar{W} = V_{IH}$ ,  $\bar{CE} = V_{IL}$ , and is  $\bar{OE} = V_{IL}$ . Address is valid prior to the coincidental with  $\bar{CE}$  transition LOW.
2.  $t_{BDD}$  delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultaneous read operations  $\bar{BUSY}$  has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last  $t_{AOE}$ ,  $t_{ACE}$ ,  $t_{AA}$ , and  $t_{BDD}$ .

Timing Waveform of Read Cycle No. 2, Either Side<sup>(3)</sup>



NOTES:

1. Timing depends on which signal is asserted last,  $\bar{OE}$  or  $\bar{CE}$ .
2. Timing depends on which signal is desasserted first,  $\bar{OE}$  or  $\bar{CE}$ .
3.  $R/\bar{W} = V_{IH}$  and the address is valid prior to or coincidental with  $\bar{CE}$  transition LOW.
4. Start of valid data depends on which timing becomes effective last  $t_{AOE}$ ,  $t_{ACE}$ , and  $t_{BDD}$ .

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(4,5)</sup>

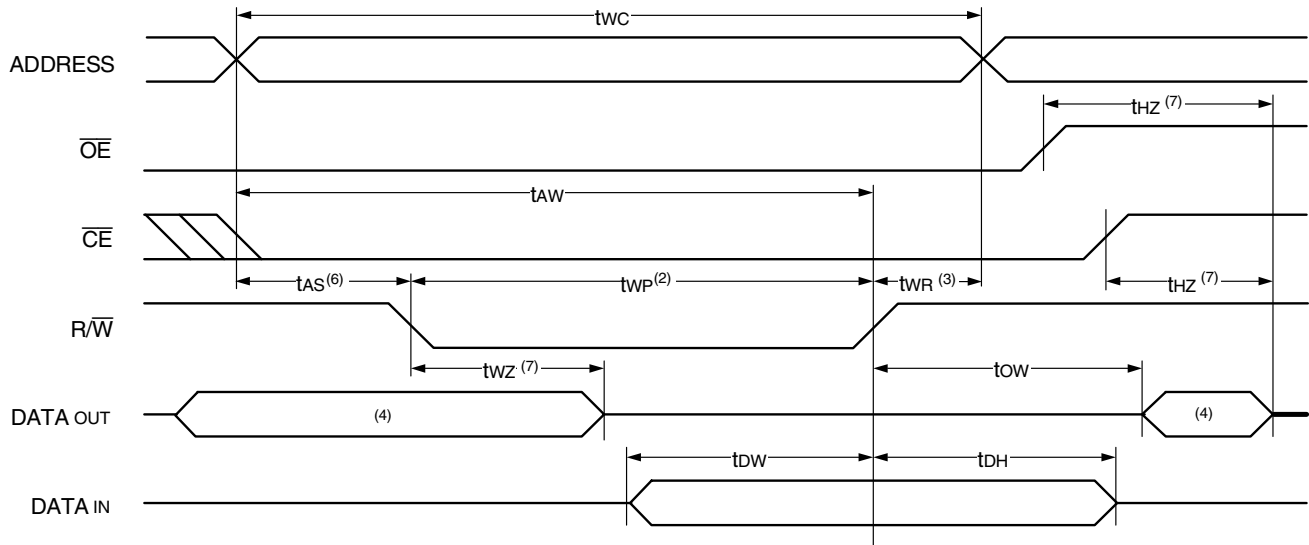
Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
t <sub>wc</sub>	Write Cycle Time	25	—	35	—	55	—	ns
t <sub>ew</sub>	Chip Enable to End-of-Write	20	—	30	—	40	—	ns
t <sub>aw</sub>	Address Valid to End-of-Write	20	—	30	—	40	—	ns
t <sub>as</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>wp</sub>	Write Pulse Width	20	—	30	—	40	—	ns
t <sub>wr</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>dw</sub>	Data Valid to End-of-Write	12	—	20	—	20	—	ns
t <sub>hz</sub>	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	30	ns
t <sub>dh</sub>	Data Hold Time <sup>(3)</sup>	0	—	0	—	0	—	ns
t <sub>wz</sub>	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	15	—	15	—	30	ns
t <sub>ow</sub>	Output Active from End-of-Write <sup>(1,2,3)</sup>	0	—	0	—	0	—	ns

3741 tbl 10

**NOTES:**

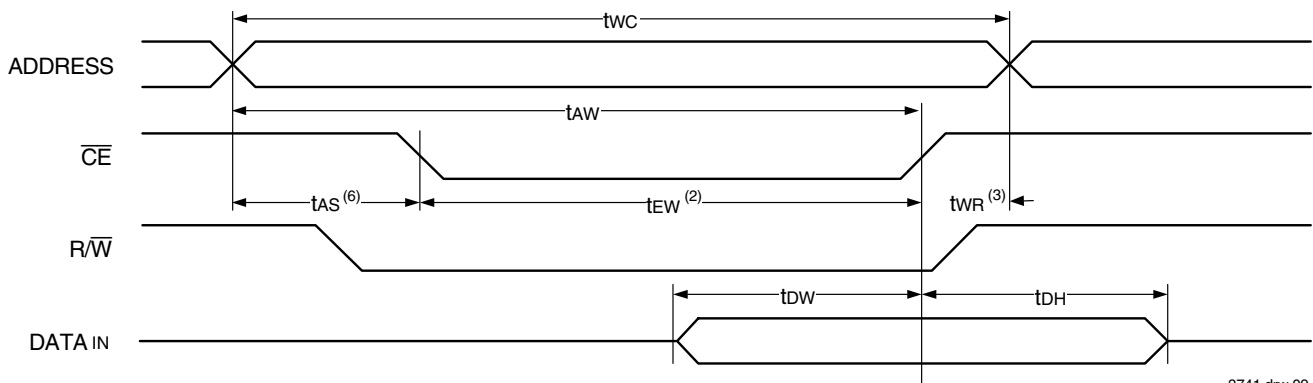
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t<sub>dh</sub> must be met by the device supplying write data to the SRAM under all operating conditions. Although t<sub>dh</sub> and t<sub>ow</sub> values will vary over voltage and temperature, the actual t<sub>dh</sub> will always be smaller than the actual t<sub>ow</sub>.
4. 'X' in part number indicates power rating (S or L).
5. Industrial temperatures: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)<sup>(1,5,8)</sup>



3741 drw 08

Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing<sup>(1,5)</sup>



3741 drw 09

NOTES:

1. R/W or CE must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of CE = VIL and R/W = VIL.
3. tWR is measured from the earlier of CE or R/W going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (CE or R/W) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (twz + tOW) to allow the I/O drivers to turn off data to be placed on the bus for the required tOW. If OE is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(6,7)</sup>

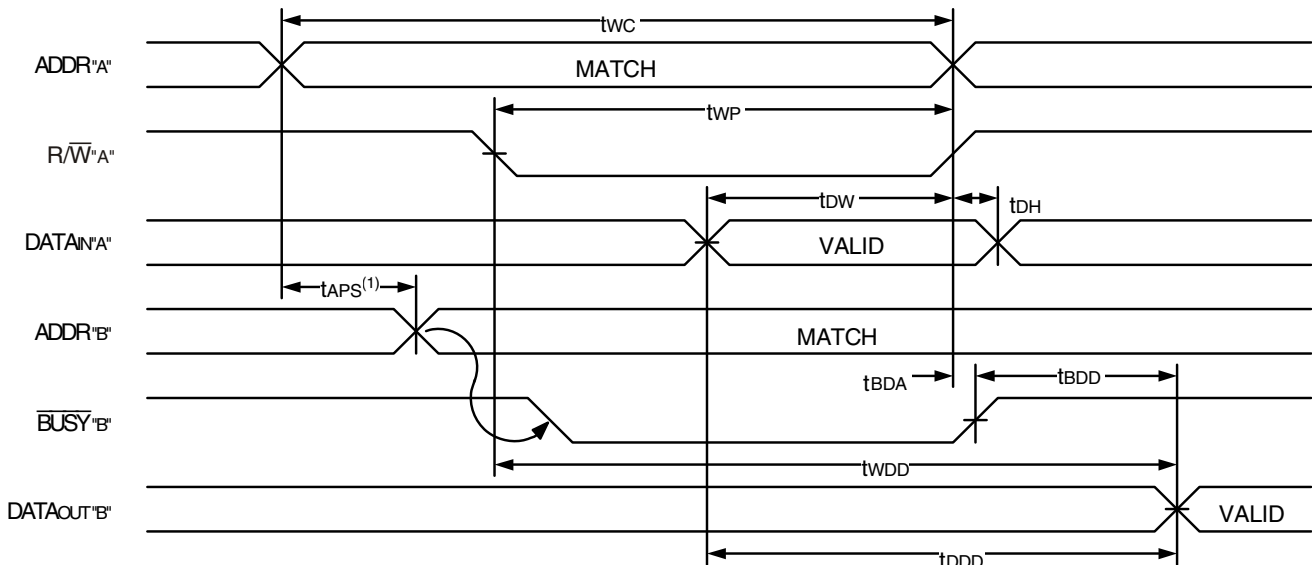
Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUSY TIMING (M/S=VIH)</b>								
tBAA	$\overline{\text{BUSY}}$ Access Time from Address Match	—	20	—	20	—	30	ns
tBDA	$\overline{\text{BUSY}}$ Disable Time from Address Not Matched	—	20	—	20	—	30	ns
tBAC	$\overline{\text{BUSY}}$ Access Time from Chip Enable	—	20	—	20	—	30	ns
tBDC	$\overline{\text{BUSY}}$ Disable Time from Chip Enable	—	20	—	20	—	30	ns
tWH	Write Hold After $\overline{\text{BUSY}}^{(5)}$	20	—	30	—	40	—	ns
twDD	Write Pulse to Data Delay <sup>(1)</sup>	—	50	—	60	—	80	ns
tDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	35	—	45	—	65	ns
tAPS	Arbitration Priority Set-up Time <sup>(2)</sup>	5	—	5	—	5	—	ns
tBDD	$\overline{\text{BUSY}}$ Disable to Valid Data <sup>(3)</sup>	—	30	—	30	—	45	ns

3741 tbl 11

NOTES:

1. Port-to-port delay through SRAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read with  $\overline{\text{BUSY}}$ ".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, twDD – twP (actual) or tDD – tw (actual).
4. To ensure that the Write Cycle is inhibited on Port "B" during contention on Port "A".
5. To ensure that the Write Cycle is completed on Port "B" after contention on Port "A".
6. 'X' in part number indicates power rating (S or L).
7. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Write with Port-to-Port Read with  $\overline{\text{BUSY}}^{(1,2,3,4)}$

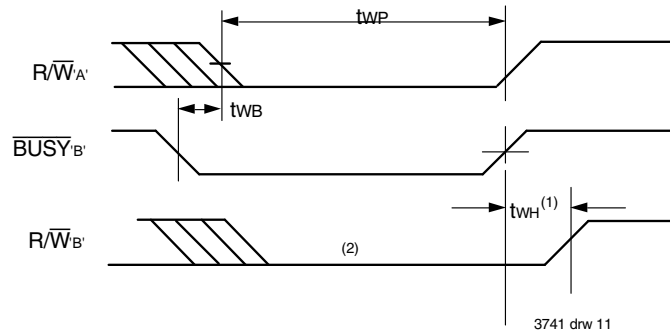


3741 drw 10

NOTES:

1. To ensure that the earlier of the two ports wins.
2.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = \text{VIL}$
3.  $\overline{\text{OE}} = \text{VIL}$  for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

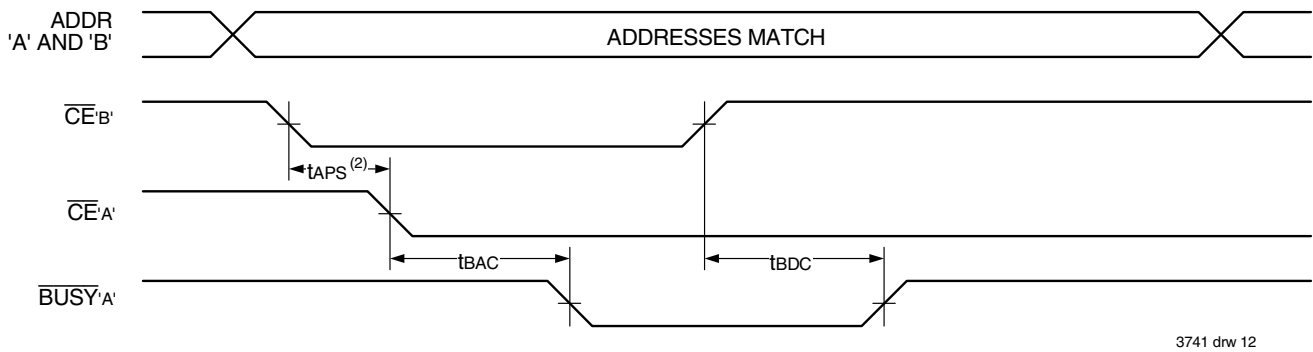
Timing Waveform of Write with **BUSY**<sup>(3)</sup>



NOTES:

1.  $t_{WH}$  must be met for  $\overline{BUSY}$ .
2.  $\overline{BUSY}$  is asserted on port 'B' blocking  $R/\overline{W}_B$ , until  $\overline{BUSY}_B$  goes HIGH.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

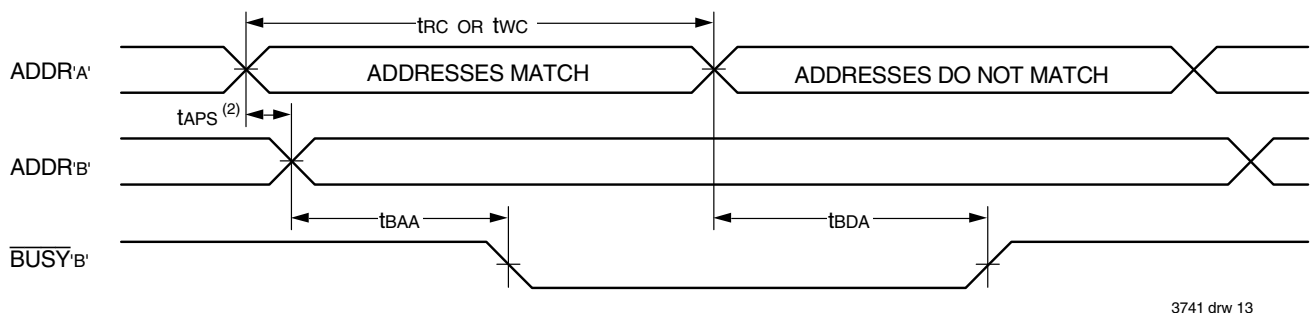
Timing Waveform of **BUSY** Arbitration Controlled by  $\overline{CE}$  Timing<sup>(1)</sup>



NOTES:

1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If  $t_{APS}$  is not satisfied, the  $\overline{BUSY}$  will be asserted on one side or the other, but there is no guarantee on which side  $\overline{BUSY}$  will be asserted.

Timing Waveform of **BUSY** Arbitration Controlled Address Match Timing<sup>(1)</sup>



NOTES:

1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If  $t_{APS}$  is not satisfied, the  $\overline{BUSY}$  will be asserted on one side or the other, but there is no guarantee on which side  $\overline{BUSY}$  will be asserted.

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1,2)</sup>

Symbol	Parameter	71V30X25 Com'l Only		71V30X35 Com'l & Ind		71V30X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>INTERRUPT TIMING</b>								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	25	—	45	ns
tINR	Interrupt Reset Time	—	25	—	25	—	45	ns

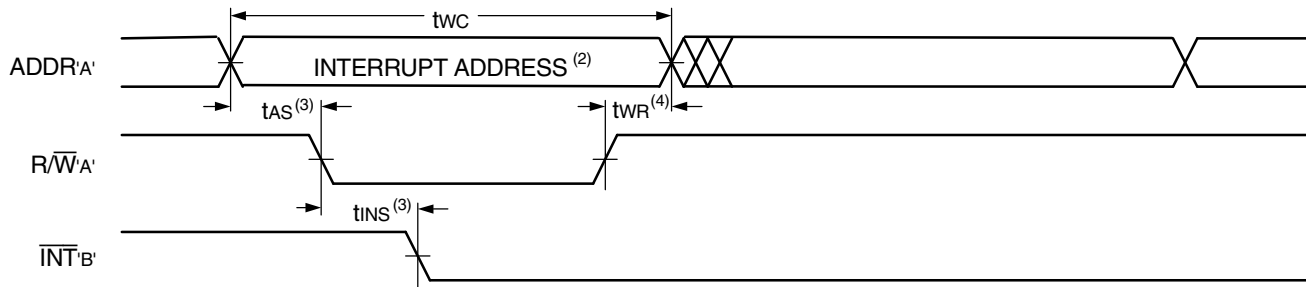
3741 tbl 12

**NOTES:**

1. 'X' in part number indicates power rating (S or L).
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

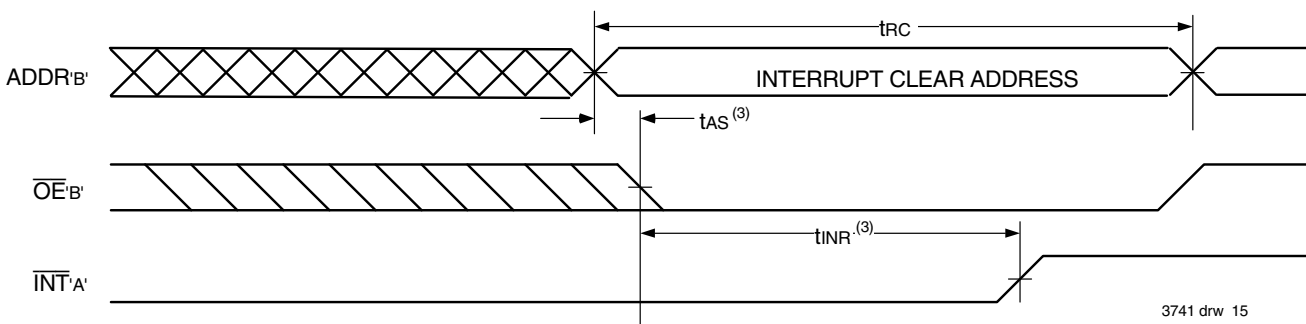
### Timing Waveform of Interrupt Mode<sup>(1)</sup>

#### INT Sets



3741 drw 14

#### INT Clears



3741 drw 15

**NOTES:**

1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal ( $\overline{CE}$  or  $R/\overline{W}$ ) is asserted last.
4. Timing depends on which enable signal ( $\overline{CE}$  or  $R/\overline{W}$ ) is de-asserted first.

Truth Tables

Table I — Non-Contention Read/Write Control<sup>(4)</sup>

Left or Right Port <sup>(1)</sup>				Function
R $\overline{W}$	$\overline{C\!E}$	$\overline{O\!E}$	D <sub>0-7</sub>	
X	H	X	Z	Port Disabled and in Power-Down Mode, ISB2 or ISB4
X	H	X	Z	$\overline{C\!E}_R = \overline{C\!E}_L = V_{IH}$ , Power-Down Mode, ISB1 or ISB3
L	L	X	DATA <sub>IN</sub>	Data on Port Written Into Memory <sup>(2)</sup>
H	L	L	DATA <sub>OUT</sub>	Data in Memory Output on Port <sup>(3)</sup>
H	L	H	Z	High Impedance Outputs

3741 tbl 13

NOTES:

1. A<sub>0L</sub> – A<sub>9L</sub> ≠ A<sub>0R</sub> – A<sub>9R</sub>.
2. If  $\overline{B\!U\!S\!Y} = L$ , data is not written.
3. If  $\overline{B\!U\!S\!Y} = L$ , data may not be valid, see t<sub>WDD</sub> and t<sub>DD</sub> timing.
4. 'H' = V<sub>IH</sub>, 'L' = V<sub>IL</sub>, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Table II — Interrupt Flag<sup>(1,4)</sup>

Left Port					Right Port					Function
R/ $\overline{W}$	$\overline{C\!E}_L$	$\overline{O\!E}_L$	A <sub>9L</sub> -A <sub>0L</sub>	$\overline{I\!N\!T}_L$	R/ $\overline{W}$	$\overline{C\!E}_R$	$\overline{O\!E}_R$	A <sub>9R</sub> -A <sub>0R</sub>	$\overline{I\!N\!T}_R$	
L	L	X	3FF	X	X	X	X	X	L <sup>(2)</sup>	Set Right $\overline{I\!N\!T}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H <sup>(3)</sup>	Reset Right $\overline{I\!N\!T}_R$ Flag
X	X	X	X	L <sup>(3)</sup>	L	L	X	3FE	X	Set Left $\overline{I\!N\!T}_L$ Flag
X	L	L	3FE	H <sup>(2)</sup>	X	X	X	X	X	Reset Left $\overline{I\!N\!T}_L$ Flag

3741 tbl 14

NOTES:

1. Assumes  $\overline{B\!U\!S\!Y}_L = \overline{B\!U\!S\!Y}_R = V_{IH}$
2. If  $\overline{B\!U\!S\!Y}_L = V_{IL}$ , then No Change.
3. If  $\overline{B\!U\!S\!Y}_R = V_{IL}$ , then No Change.
4. 'H' = HIGH, 'L' = LOW, 'X' = DON'T CARE

Table III — Address  $\overline{B\!U\!S\!Y}$  Arbitration

Inputs			Outputs		Function
$\overline{C\!E}_L$	$\overline{C\!E}_R$	A <sub>0L</sub> -A <sub>9L</sub> A <sub>0R</sub> -A <sub>9R</sub>	$\overline{B\!U\!S\!Y}_L$ <sup>(1)</sup>	$\overline{B\!U\!S\!Y}_R$ <sup>(1)</sup>	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

3741 tbl 15

NOTES:

1. Pins  $\overline{B\!U\!S\!Y}_L$  and  $\overline{B\!U\!S\!Y}_R$  are both outputs for IDT71V30.  $\overline{B\!U\!S\!Y}_x$  outputs on the IDT71V30 are non-tristatable push-pull.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t<sub>APS</sub> is not met, either  $\overline{B\!U\!S\!Y}_L$  or  $\overline{B\!U\!S\!Y}_R = LOW$  will result.  $\overline{B\!U\!S\!Y}_L$  and  $\overline{B\!U\!S\!Y}_R$  outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when  $\overline{B\!U\!S\!Y}_L$  outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when  $\overline{B\!U\!S\!Y}_R$  outputs are driving LOW regardless of actual logic level on the pin.

## Functional Description

The IDT71V30 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V30 has an automatic power down feature controlled by CE. The CE controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{CE} = V_{IH}$ ). When a port is enabled, access to the entire memory array is permitted.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ( $\overline{INTL}$ ) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the  $\overline{CE} = R/\overline{W} = V_{IL}$  per Truth Table II. The left port clears the interrupt by accessing address location 3FE access with  $\overline{CE}_R = \overline{OE}_R = V_{IL}$ ,  $R/\overline{W}$  is a "don't care". Likewise, the right port interrupt flag ( $\overline{INTR}$ ) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ( $\overline{INTR}$ ), the right port must access the memory location 3FF. The message (8 bits)

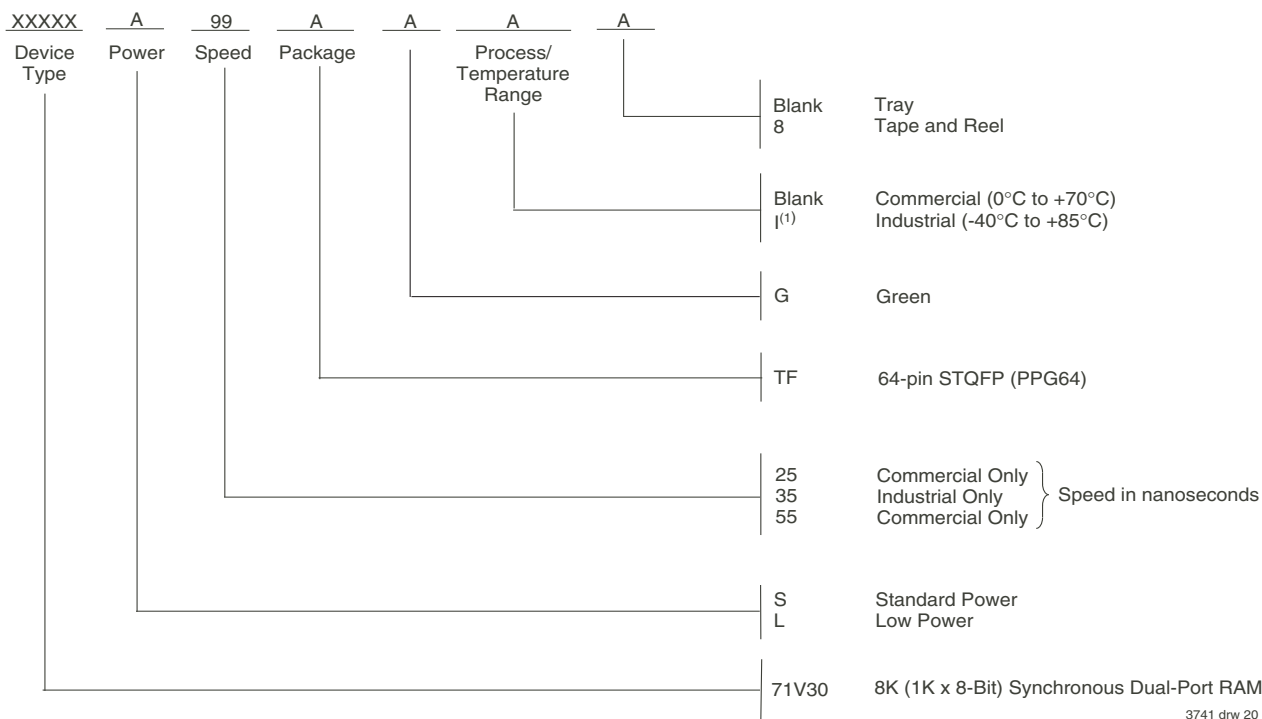
at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, and are part of the random access memory. Refer to Table II for the interrupt operation.

## Busy Logic

Busy Logic provides a hardware indication that both ports of the SRAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the SRAM is "Busy". The  $\overline{BUSY}$  pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a  $\overline{BUSY}$  indication, the write signal is gated internally to prevent the write from proceeding.

The use of  $\overline{BUSY}$  logic is not required or desirable for all applications. In some cases it may be useful to logically OR the  $\overline{BUSY}$  outputs together and use any  $\overline{BUSY}$  indication as an interrupt source to flag the event of an illegal or illogical operation.

### Ordering Information



**NOTES:**

- Contact your sales office for Industrial Temperature range in other speeds, packages and powers.
- LEAD FINISH (SnPb) are Obsolete - Product Discontinuation Notice - PDN#SP-17-02  
Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

### Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
25	71V30L25TFG	PPG64	TQFP	C
	71V30L25TFG8	PPG64	TQFP	C
35	71V30L35TFGI	PPG64	TQFP	I
	71V30L35TFGI8	PPG64	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
55	71V30S55TFG	PPG64	TQFP	C
	71V30S55TFG8	PPG64	TQFP	C

## Datasheet Document History

- 12/09/98: Initiated datasheet document history  
 Converted to new format  
 Cosmetic and typographical corrections  
 Added additional notes to pin configurations
- 06/15/99: Changed drawing format
- 08/03/99: Page 2 Fixed typographical error
- 09/01/99: Removed Preliminary
- 11/12/99: Replaced IDT logo
- 01/17/01: Pages 1 and 2 Moved all of "Description" to page 2 and adjusted page layouts  
 Page 3 Increased storage temperature parameters  
 Clarified TA parameter  
 Page 4 DC Electrical parameters—changed wording from "open" to "disabled"  
 Changed  $\pm 200\text{mV}$  to  $0\text{mV}$  in notes
- 03/14/05: Page 1 Added green availability to features  
 Page 17 Added green indicator to ordering information  
 Page 1 & 17 Replaced old <sup>TM</sup> logo with new <sup>TM</sup> logo
- 07/16/07: Page 3 Added Junction Temperature spec values to the Absolute Maximum Rating table  
 Added footnote 3 for additional clarification of Junction Temperature
- 10/23/08: Page 14 Removed "IDT" from orderable part number
- 11/25/09: Page 4 In order to correct the DC Chars table for the 71V30L35 speed grade and to the Data Retention Chars table, I Temp values have been added to each table respectively. In addition, all of the AC tables and the ordering information also now reflect this I temp correction
- 06/22/15: Page 2 Removed IDT in reference to fabrication  
 Page 2 & 14 The package code PP64-1 changed to PP64 to match standard package codes  
 Page 14 Added Tape and Reel indicator to Ordering Information
- 07/23/15: Entire datasheet Removed the 55ns Industrial speed offering. 55ns speed only offered in commercial grade
- 12/20/17: Product Discontinuation Notice - PDN# SP-17-02  
 Last time buy expires June 15, 2018
- 06/24/19: Page 1 & 14 Deleted obsolete Commercial speed grade 35ns in Features and Ordering Information  
 Page 2 Rotated PPG64 STQFP pin configuration to accurately reflect pin 1 orientation  
 Page 14 Added Orderable Part Information tables

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