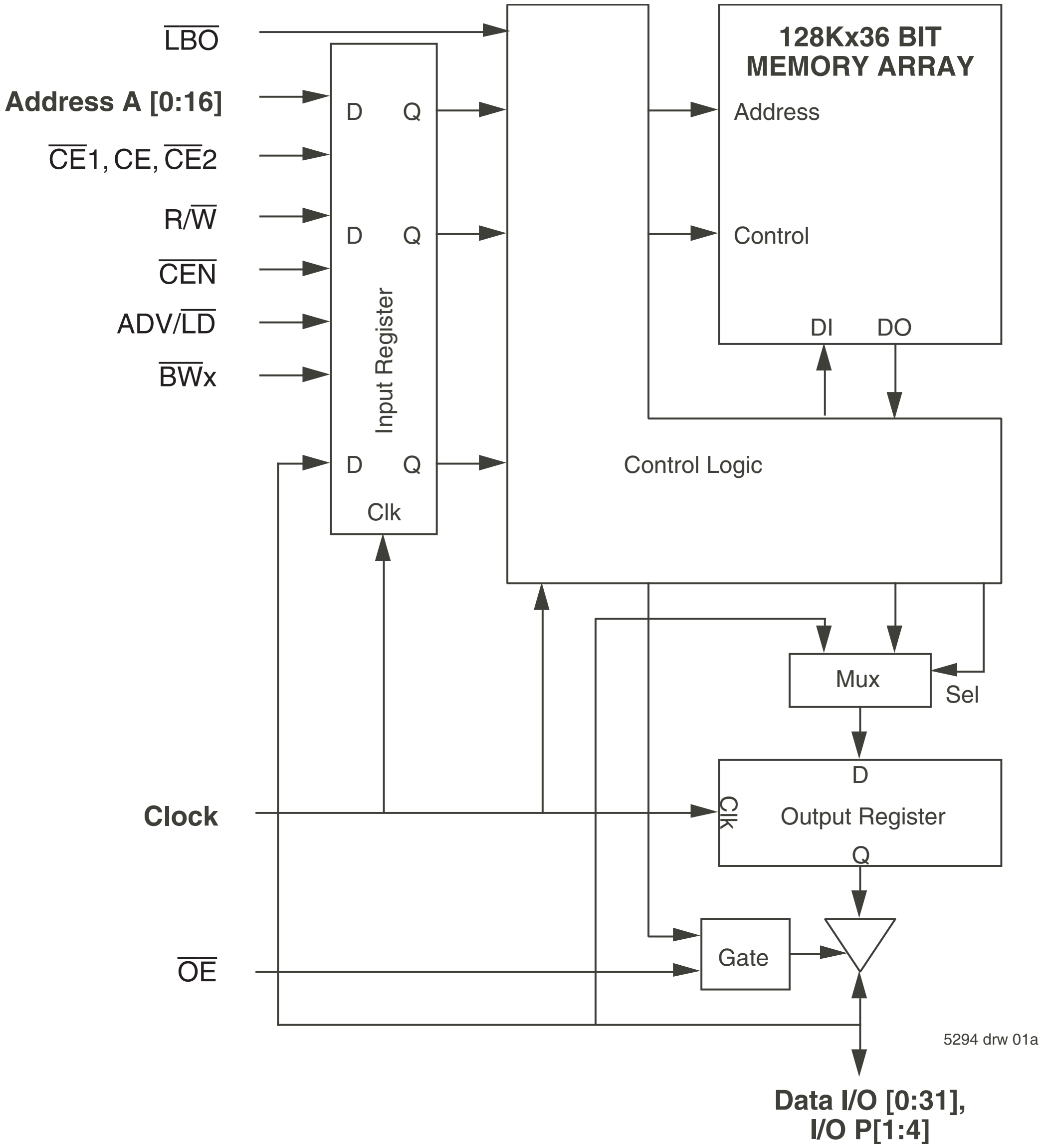
128K x 36
3.3V Synchronous ZBT™ SRAM
2.5V I/O, Burst Counter
Pipelined Outputs

71V2546S

Features

- 128K x 36 memory configurations
- Supports high performance system speed - 150 MHz (3.8 ns Clock-to-Data Access)
- ZBT^{TM} Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control $\overline{OE}$
- Single R/$\overline{W}$ (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications
- 4-word burst capability (interleaved or linear)
- Individual byte write ($\overline{BW_1}$ - $\overline{BW_4}$) control (May tie active)
- Three chip enables for simple depth expansion
- 3.3V power supply (±5%), 2.5V I/O Supply (V_{DDQ})
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP) and 119 ball grid array (BGA)
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



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Description

The IDT71V2546 is a 3.3V high-speed 4,718,592-bit (4.5 Megabit) synchronous SRAM. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT^{TM}, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71V2546 contains data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V2546 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CEN}$) is high and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}_1$, CE_2, $\overline{CE}_2$) that allow the user to deselect the device when desired. If any one of these three are not asserted when ADV/$\overline{LD}$ is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after chip is deselected or a write is initiated.

The IDT71V2546 has an on-chip burst counter. In the burst mode, the IDT71V2546 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the $\overline{LBO}$ input pin. The $\overline{LBO}$ pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH).

The IDT71V2546 SRAM utilizes a high-performance CMOS process and is packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA).

Pin Description Summary

A_0-A_{16}	Address Inputs	Input	Synchronous
$\overline{CE}_1$, CE_2, $\overline{CE}_2$	Chip Enables	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
R/$\overline{W}$	Read/Write Signal	Input	Synchronous
$\overline{CEN}$	Clock Enable	Input	Synchronous
$\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$, $\overline{BW}_4$	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/$\overline{LD}$	Advance burst address / Load new address	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	Static
ZZ	Sleep Mode	Input	Synchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	Static
V_{SS}	Ground	Supply	Static

5294 tbl 01

Pin Definitions[1]

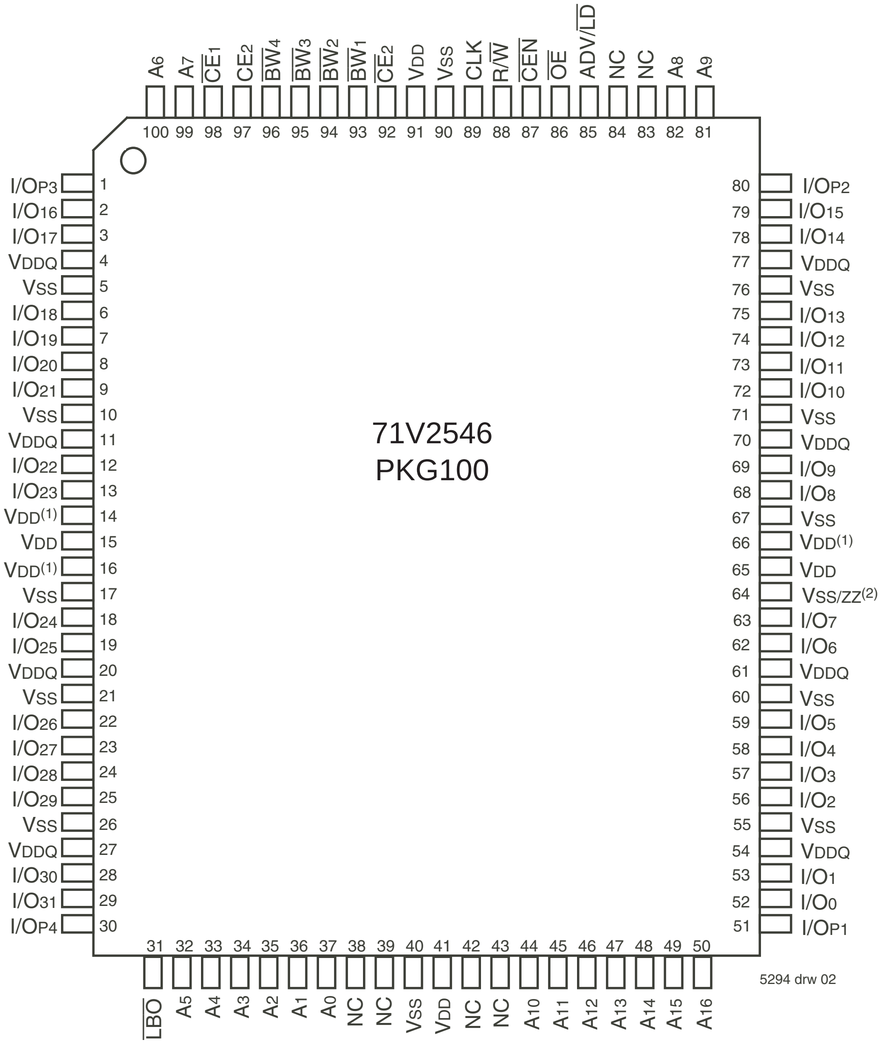
Symbol	Pin Function	I/O	Active	Description
A_0-A_{16}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/$\overline{LD}$ low, $\overline{CEN}$ low, and true chip enables.
ADV/$\overline{LD}$	Advance / Load	I	N/A	ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/$\overline{LD}$ is low with the chip deselected, any burst in progress is terminated. When ADV/$\overline{LD}$ is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/$\overline{LD}$ is sampled high.
R/$\overline{W}$	Read / Write	I	N/A	R/$\overline{W}$ signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous Clock Enable Input. When $\overline{CEN}$ is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CEN}$ sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, $\overline{CEN}$ must be sampled low at rising edge of clock.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled low) the appropriate byte write signal ($\overline{BW_1}$-$\overline{BW_4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/$\overline{W}$ is sampled high. The appropriate byte(s) of data are written into the device two cycles later. $\overline{BW_1}$-$\overline{BW_4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE_1}$ and $\overline{CE_2}$ are used with CE_2 to enable the IDT71V2546. ($\overline{CE_1}$ or $\overline{CE_2}$ sampled high or CE_2 sampled low) and ADV/$\overline{LD}$ low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.
CE_2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE_2 is used with $\overline{CE_1}$ and $\overline{CE_2}$ to enable the chip. CE_2 has inverted polarity but otherwise identical to $\overline{CE_1}$ and $\overline{CE_2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V2546. Except for $\overline{OE}$, all timing references for the device are made with respect to the rising edge of CLK.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Burst order selection input. When $\overline{LBO}$ is high the Interleaved burst sequence is selected. When $\overline{LBO}$ is low the Linear burst sequence is selected. $\overline{LBO}$ is a static input and it must not change during device operation.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. $\overline{OE}$ must be low to read data from the IDT71V2546. When $\overline{OE}$ is high the I/O pins are in a high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied low.
ZZ	Sleep Mode	I	HIGH	Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V2546 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	2.5V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.

5294 tbl 02

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Pin Configuration(3) — 128K x 36, PKG100



Top View
100 TQFP

NOTES:

1. Pins 14, 16 and 66 do not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pin 64 does not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$; on the latest die revision this pin supports ZZ (sleep mode).
3, This text does not indicate the orientation of actual part-marking..

Pin Configuration(3) — 128K x 36, BG119

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	NC	A8	A16	V_{DDQ}
B	NC	CE2	A3	ADV/$\overline{\text{LD}}$	A9	$\overline{\text{CE}}_2$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	I/O16	I/OP3	V_{SS}	NC	V_{SS}	I/OP2	I/O15
E	I/O17	I/O18	V_{SS}	$\overline{\text{CE}}_1$	V_{SS}	I/O13	I/O14
F	V_{DDQ}	I/O19	V_{SS}	$\overline{\text{OE}}$	V_{SS}	I/O12	V_{DDQ}
G	I/O20	I/O21	$\overline{\text{BW}}_3$	NC	$\overline{\text{BW}}_2$	I/O11	I/O10
H	I/O22	I/O23	V_{SS}	R/$\overline{\text{W}}$	V_{SS}	I/O9	I/O8
J	V_{DDQ}	V_{DD}	V_{DD}(1)	V_{DD}	V_{DD}(1)	V_{DD}	V_{DDQ}
K	I/O24	I/O26	V_{SS}	CLK	V_{SS}	I/O6	I/O7
L	I/O25	I/O27	$\overline{\text{BW}}_4$	NC	$\overline{\text{BW}}_1$	I/O4	I/O5
M	V_{DDQ}	I/O28	V_{SS}	$\overline{\text{CEN}}$	V_{SS}	I/O3	V_{DDQ}
N	I/O29	I/O30	V_{SS}	A1	V_{SS}	I/O2	I/O1
P	I/O31	I/OP4	V_{SS}	A0	V_{SS}	I/OP1	I/O0
R	NC	A5	$\overline{\text{LBO}}$	V_{DD}	V_{DD}(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	NC/ZZ(2)
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

5294 drw 13a

Top View
119 BGA

NOTES:
1. J3, J5, and R5 do not have to be directly connected to V_{DD} as long as the input voltage is $\geq V_{IH}$.
2. Pin T7 supports ZZ (sleep mode) on the latest die revision.
3. This text does not indicate orientation of actual part-marking.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature(1)	VSS	VDD	VDDQ
Commercial	0°C to +70°C	0V	3.3V±5%	2.5V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	2.5V±5%

5294 tbl 05

NOTE:

1. TA is the "instant on" case temperature.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial Values	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM(3,6)	Terminal Voltage with Respect to GND	-0.5 to VDD	V
VTERM(4,6)	Terminal Voltage with Respect to GND	-0.5 to VDD +0.5	V
VTERM(5,6)	Terminal Voltage with Respect to GND	-0.5 to VDDQ +0.5	V
TA(7)	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	2.0	W
IOUT	DC Output Current	50	mA

5294 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD terminals only.
3. VDDQ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed VDDQ during power supply ramp up.
7. TA is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.135	3.3	3.465	V
VDDQ	I/O Supply Voltage	2.375	2.5	2.625	V
VSS	Supply Voltage	0	0	0	V
VIH	Input High Voltage - Inputs	1.7	—	VDD +0.3	V
VIH	Input High Voltage - I/O	1.7	—	VDDQ +0.3(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.7	V

5294 tbl 03

NOTES:

1. VIL (min.) = –1.0V for pulse width less than tCYC/2, once per cycle.
2. VIH (max.) = +6.0V for pulse width less than tCYC/2, once per cycle.

100 TQFP Capacitance(1)

(TA = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	5	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

5294 tbl 07

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

119 BGA Capacitance(1)

(TA = +25° C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	7	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

5294 tbl 07a

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Synchronous Truth Table(1)

$\overline{\text{CEN}}$	R/$\overline{\text{W}}$	Chip(5) Enable	ADV/$\overline{\text{LD}}$	$\overline{\text{BW}}$x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O(6) (2 cycles later)
L	L	Select	L	Valid	External	X	LOAD WRITE	D(7)
L	H	Select	L	X	External	X	LOAD READ	Q(7)
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter)(2)	D(7)
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter)(2)	Q(7)
L	X	Deselect	L	X	X	X	DESELECT or STOP(3)	HiZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HiZ
H	X	X	X	X	X	X	SUSPEND(4)	Previous Value

5294 tbl 08

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. When ADV/$\overline{\text{LD}}$ signal is sampled high, the internal burst counter is incremented. The R/$\overline{\text{W}}$ signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/$\overline{\text{W}}$ signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either ($\overline{\text{CE}}_1$, or $\overline{\text{CE}}_2$ is sampled high or CE_2 is sampled low) and ADV/$\overline{\text{LD}}$ is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When $\overline{\text{CEN}}$ is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L, CE_2 = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

OPERATION	R/$\overline{\text{W}}$	$\overline{\text{BW}}_1$	$\overline{\text{BW}}_2$	$\overline{\text{BW}}_3$	$\overline{\text{BW}}_4$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/O$_{P1}$)(2)	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/O$_{P2}$)(2)	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/O$_{P3}$)(2)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/O$_{P4}$)(2)	L	H	H	H	L
NO WRITE	L	H	H	H	H

5294 tbl 09

NOTES:

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.

Interleaved Burst Sequence Table ($\overline{\text{LBO}}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	**A0**	**A1**	**A0**	**A1**	**A0**	**A1**	**A0**
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5294 tbl 10

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table ($\overline{\text{LBO}}$=V_{SS})

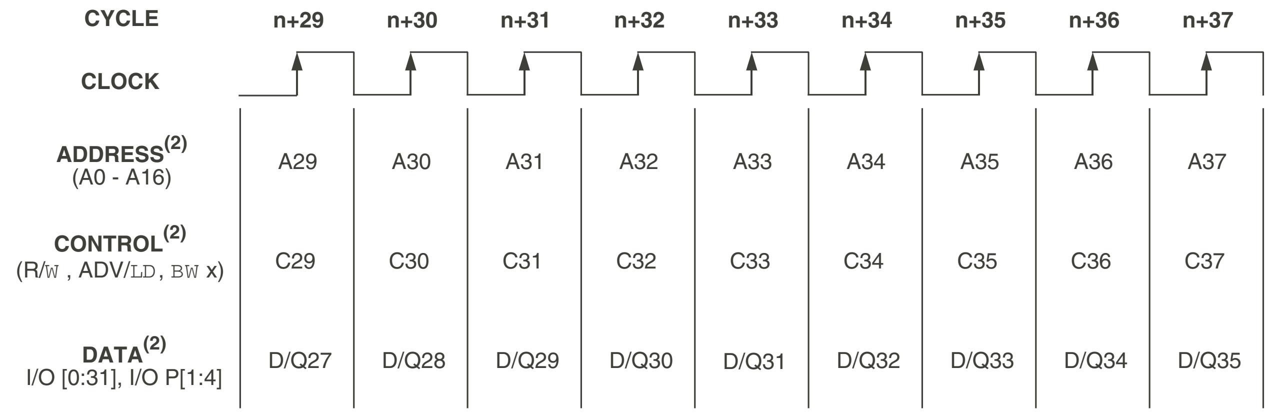
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	**A0**	**A1**	**A0**	**A1**	**A0**	**A1**	**A0**
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5294 tbl 11

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram(1)



5294 drw 03

NOTES:

1. This assumes $\overline{CEN}$, $\overline{CE}_1$, CE_2, $\overline{CE}_2$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles(2)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(1)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Load read
n+1	X	X	H	X	L	X	X	X	Burst read
n+2	A_1	H	L	L	L	X	L	Q_0	Load read
n+3	X	X	L	H	L	X	L	Q_{0+1}	Deselect or STOP
n+4	X	X	H	X	L	X	L	Q_1	NOOP
n+5	A_2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	X	Z	Burst read
n+7	X	X	L	H	L	X	L	Q_2	Deselect or STOP
n+8	A_3	L	L	L	L	L	L	Q_{2+1}	Load write
n+9	X	X	H	X	L	L	X	Z	Burst write
n+10	A_4	L	L	L	L	L	X	D_3	Load write
n+11	X	X	L	H	L	X	X	D_{3+1}	Deselect or STOP
n+12	X	X	H	X	L	X	X	D_4	NOOP
n+13	A_5	L	L	L	L	L	X	Z	Load write
n+14	A_6	H	L	L	L	X	X	Z	Load read
n+15	A_7	L	L	L	L	L	X	D_5	Load write
n+16	X	X	H	X	L	L	L	Q_6	Burst write
n+17	A_8	H	L	L	L	X	X	D_7	Load read
n+18	X	X	H	X	L	X	X	D_{7+1}	Burst read
n+19	A_9	L	L	L	L	L	L	Q_8	Load write

5294 tbl 12

NOTES:
1. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.
2. H = High; L = Low; X = Don't Care; Z = High Impedance.

Read Operation(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	X	X	L	Q_0	Contents of Address A_0 Read Out

5294 tbl 13

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Burst Read Operation(1)

Cycle	Address	R/$\overline{\text{W}}$	ADV/$\overline{\text{LD}}$	$\overline{\text{CE}}$(2)	$\overline{\text{CEN}}$	$\overline{\text{BWx}}$	$\overline{\text{OE}}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	X	X	Clock Setup Valid, Advance Counter
n+2	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q_{0+1}	Address A_{0+1} Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q_{0+2}	Address A_{0+2} Read Out, Inc. Count
n+5	A_1	H	L	L	L	X	L	Q_{0+3}	Address A_{0+3} Read Out, Load A_1
n+6	X	X	H	X	L	X	L	Q_0	Address A_0 Read Out, Inc. Count
n+7	X	X	H	X	L	X	L	Q_1	Address A_1 Read Out, Inc. Count
n+8	A_2	H	L	L	L	X	L	Q_{1+1}	Address A_{1+1} Read Out, Load A_2

5294 tbl 14

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance..
2. $\overline{\text{CE}}$ = L is defined as $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L and CE_2 = H. $\overline{\text{CE}}$ = H is defined as $\overline{\text{CE}}_1$ = H, $\overline{\text{CE}}_2$ = H or CE_2 = L.

Write Operation(1)

Cycle	Address	R/$\overline{\text{W}}$	ADV/$\overline{\text{LD}}$	$\overline{\text{CE}}$(2)	$\overline{\text{CEN}}$	$\overline{\text{BWx}}$	$\overline{\text{OE}}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	X	Clock Setup Valid
n+2	X	X	X	X	L	X	X	D_0	Write to Address A_0

5294 tbl 15

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{\text{CE}}$ = L is defined as $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L and CE_2 = H. $\overline{\text{CE}}$ = H is defined as $\overline{\text{CE}}_1$ = H, $\overline{\text{CE}}_2$ = H or CE_2 = L.

Burst Write Operation(1)

Cycle	Address	R/$\overline{\text{W}}$	ADV/$\overline{\text{LD}}$	$\overline{\text{CE}}$(2)	$\overline{\text{CEN}}$	$\overline{\text{BWx}}$	$\overline{\text{OE}}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	X	Clock Setup Valid, Inc. Count
n+2	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+3	X	X	H	X	L	L	X	D_{0+1}	Address A_{0+1} Write, Inc. Count
n+4	X	X	H	X	L	L	X	D_{0+2}	Address A_{0+2} Write, Inc. Count
n+5	A1	L	L	L	L	L	X	D_{0+3}	Address A_{0+3} Write, Load A_1
n+6	X	X	H	X	L	L	X	D_0	Address A_0 Write, Inc. Count
n+7	X	X	H	X	L	L	X	D_1	Address A_1 Write, Inc. Count
n+8	A_2	L	L	L	L	L	X	D_{1+1}	Address A_{1+1} Write, Load A_2

5294 tbl 16

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{\text{CE}}$ = L is defined as $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L and CE_2 = H. $\overline{\text{CE}}$ = H is defined as $\overline{\text{CE}}_1$ = H, $\overline{\text{CE}}_2$ = H or CE_2 = L.

Read Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A_1	H	L	L	L	X	X	X	Clock Valid
n+3	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+4	X	X	X	X	H	X	L	Q_0	Clock Ignored. Data Q_0 is on the bus.
n+5	A_2	H	L	L	L	X	L	Q_0	Address A_0 Read out (bus trans.)
n+6	A_3	H	L	L	L	X	L	Q_1	Address A_1 Read out (bus trans.)
n+7	A_4	H	L	L	L	X	L	Q_2	Address A_2 Read out (bus trans.)

5294 tbl 17

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Write Operation with Clock Enable Used(1)

Cycle	Address	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$(2)	$\overline{CEN}$	$\overline{BW}$x	$\overline{OE}$	I/O	Comments
n	A_0	L	L	L	L	L	X	X	Address and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A_1	L	L	L	L	L	X	X	Clock Valid.
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A_2	L	L	L	L	L	X	D_0	Write Data D_0
n+6	A_3	L	L	L	L	L	X	D_1	Write Data D_1
n+7	A_4	L	L	L	L	L	X	D_2	Write Data D_2

5294 tbl 18

NOTES:
1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\overline{CE}$ = L is defined as $\overline{CE}_1$ = L, $\overline{CE}_2$ = L and CE_2 = H. $\overline{CE}$ = H is defined as $\overline{CE}_1$ = H, $\overline{CE}_2$ = H or CE_2 = L.

Read Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{\text{W}}$	ADV/$\overline{\text{LD}}$	$\overline{\text{CE}}$[2]	$\overline{\text{CEN}}$	$\overline{\text{BW}}$x	$\overline{\text{OE}}$	I/O[3]	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	H	L	L	L	X	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	H	L	L	L	X	L	Q_0	Address A_0 Read out. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	L	Q_1	Address A_1 Read out. Deselected.
n+7	A_2	H	L	L	L	X	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	L	Q_2	Address A_2 Read out. Deselected.

5294 tbl 19

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{\text{CE}}$ = L is defined as $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L and CE_2 = H. $\overline{\text{CE}}$ = H is defined as $\overline{\text{CE}}_1$ = H, $\overline{\text{CE}}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

Write Operation with Chip Enable Used[1]

Cycle	Address	R/$\overline{\text{W}}$	ADV/$\overline{\text{LD}}$	$\overline{\text{CE}}$[2]	$\overline{\text{CEN}}$	$\overline{\text{BW}}$x	$\overline{\text{OE}}$	I/O[3]	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	?	Deselected.
n+2	A_0	L	L	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+4	A_1	L	L	L	L	L	X	D_0	Address D_0 Write in. Load A_1.
n+5	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+6	X	X	L	H	L	X	X	D_1	Address D_1 Write in. Deselected.
n+7	A_2	L	L	L	L	L	X	Z	Address and control meet setup.
n+8	X	X	L	H	L	X	X	Z	Deselected or STOP.
n+9	X	X	L	H	L	X	X	D_2	Address D_2 Write in. Deselected.

5294 tbl 20

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\overline{\text{CE}}$ = L is defined as $\overline{\text{CE}}_1$ = L, $\overline{\text{CE}}_2$ = L and CE_2 = H. $\overline{\text{CE}}$ = H is defined as $\overline{\text{CE}}_1$ = H, $\overline{\text{CE}}_2$ = H or CE_2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\lvert I_{LI}\rvert$	LBO, JTAG and ZZ Input Leakage Current$^{(1)}$	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +6mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -6mA, V_{DD} = Min.	2.0	—	V

5294 tbl 21

NOTE:
1. The $\overline{LBO}$, TMS, TDI, TCK and $\overline{TRST}$ pins will be internally pulled to V_{DD} and ZZ will be internally pulled to V_{SS} if it is not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range$^{(1)}$ (V_{DD} = 3.3V±5%)

Symbol	Parameter	Test Conditions	150MHz		133MHz		100MHz		Unit
			Com'l	Ind'l	Com'l	Ind'l	Com'l	Ind'l	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/$\overline{LD}$ = X, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = $f_{MAX}$$^{(2)}$	325	335	300	310	250	260	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0$^{(2,3)}$	40	45	40	45	40	45	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $< V_{LD}$, f = $f_{MAX}$$^{(2,3)}$	120	130	110	120	100	110	mA
I_{SB3}	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{CEN} \geq V_{IH}$, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = $f_{MAX}$$^{(2,3)}$	40	45	40	45	40	45	mA

5294 tbl 22

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} – 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} – 0.2V, V_{LD} = 0.2V.

AC Test Loads

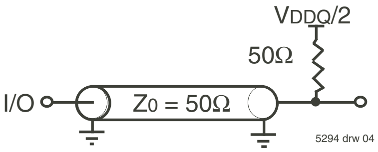


Figure 1. AC Test Load

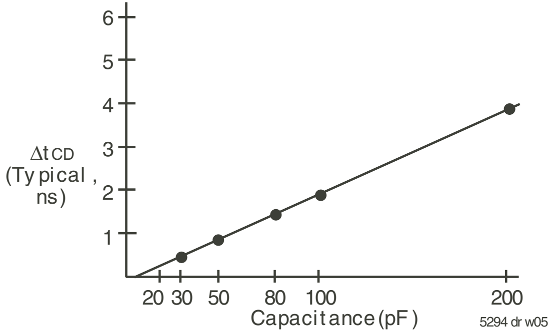


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions

(V_{DDQ} = 2.5V)

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	(V_{DDQ}/2)
Output Timing Reference Levels	(V_{DDQ}/2)
AC Test Load	See Figure 1

5294 tbl 23

AC Electrical Characteristics

(V_{DD} = 3.3V±5%, Commercial and Industrial Temperature Ranges)

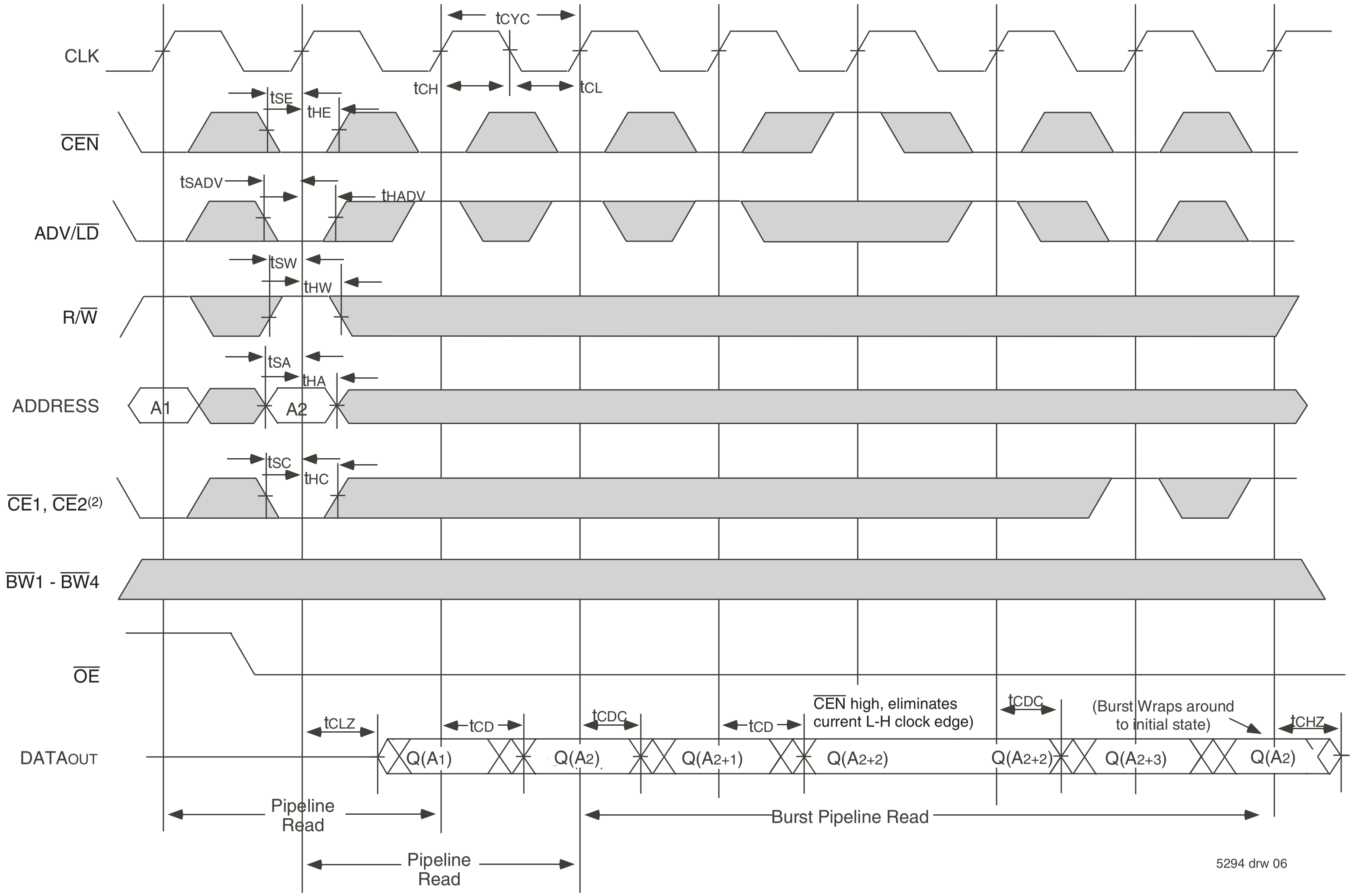
Symbol	Parameter	150MHz		133MHz		100MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	6.7	—	7.5	—	10	—	ns
t_F(1)	Clock Frequence	—	150	—	133	—	100	MHz
t_{CH}(2)	Clock High Pulse Width	2.0	—	2.2	—	3.2	—	ns
t_{CL}(2)	Clock Low Pulse Width	2.0	—	2.2	—	3.2	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.8	—	4.2	—	5	ns
t_{CDC}	Clock High to Data Change	1.5	—	1.5	—	1.5	—	ns
t_{CLZ}(3,4,5)	Clock High to Output Active	1.5	—	1.5	—	1.5	—	ns
t_{CHZ}(3,4,5)	Clock High to Data High-Z	1.5	3	1.5	3	1.5	3.3	ns
t_{OE}	Output Enable Access Time	—	3.8	—	4.2	—	5	ns
t_{OLZ}(3,4)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(3,4)	Output Enable High to Data High-Z	—	3.8	—	4.2	—	5	ns
Set Up Times								
t_{SE}	Clock Enable Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SA}	Address Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SD}	Data In Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SW}	Read/Write (R/$\overline{W}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SADV}	Advance/Load (ADV/$\overline{LD}$) Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.5	—	1.7	—	2.0	—	ns
t_{SB}	Byte Write Enable ($\overline{BW}$x) Setup Time	1.5	—	1.7	—	2.0	—	ns
Hold Times								
t_{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Read/Write (R/$\overline{W}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HADV}	Advance/Load (ADV/$\overline{LD}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HB}	Byte Write Enable ($\overline{BW}$x) Hold Time	0.5	—	0.5	—	0.5	—	ns

5294 tbl 24

NOTES:

1. $t_F = 1/t_{CYC}$.
2. Measured as HIGH above 0.6V_{DDQ} and LOW below 0.4V_{DDQ}.
3. Transition is measured ±200mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).

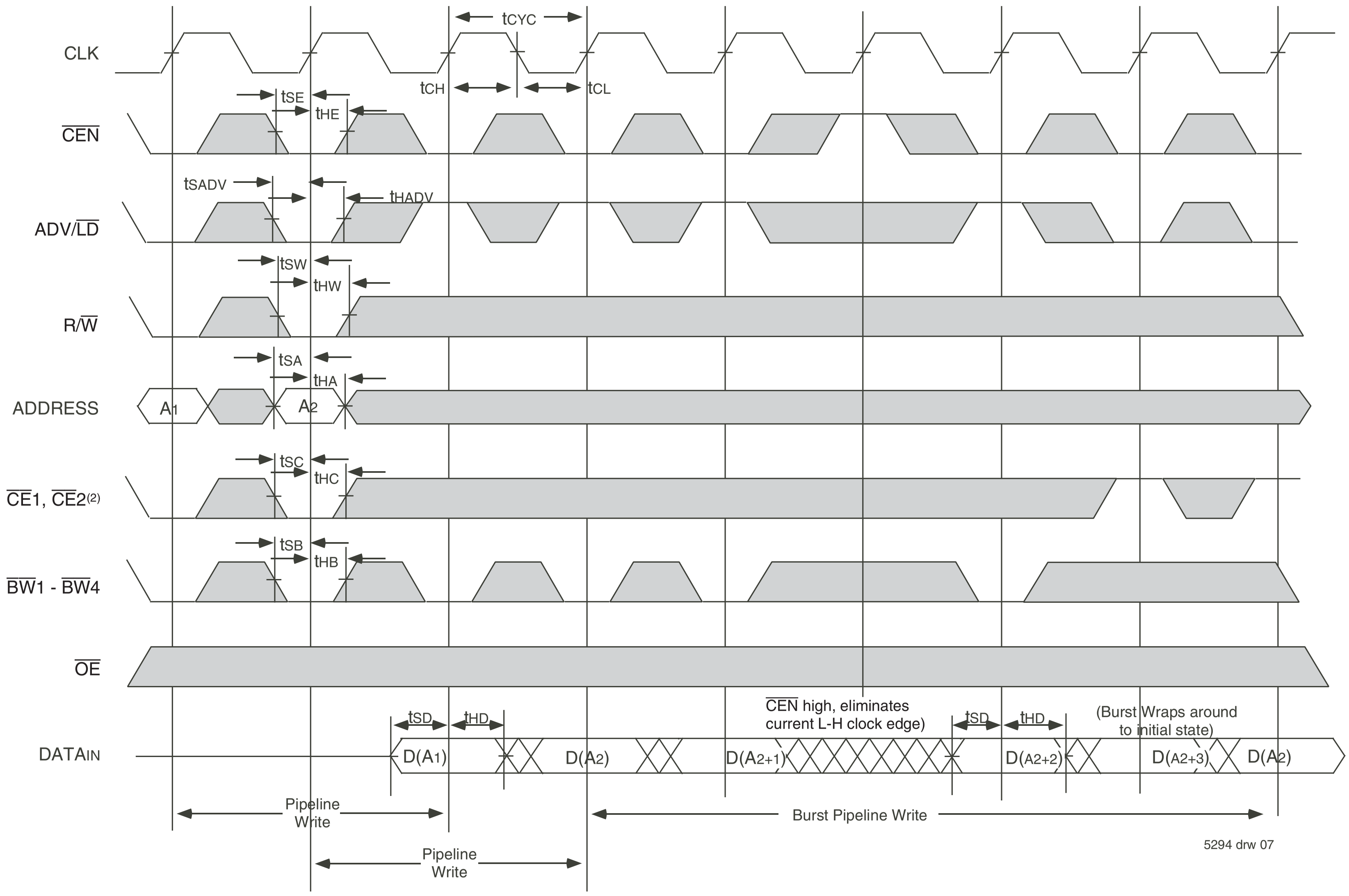
Timing Waveform of Read Cycle(1,2,3,4)



NOTES:

1. Q (A_1) represents the first output from the external address A_1. Q (A_2) represents the first output from the external address A_2; Q (A_{2+1}) represents the next output data in the burst sequence of the base address A_2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{\text{LBO}}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{\text{LD}}$ LOW.
4. R/$\overline{\text{W}}$ is don't care when the SRAM is bursting (ADV/$\overline{\text{LD}}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{\text{W}}$ signal when new address and control are loaded into the SRAM.

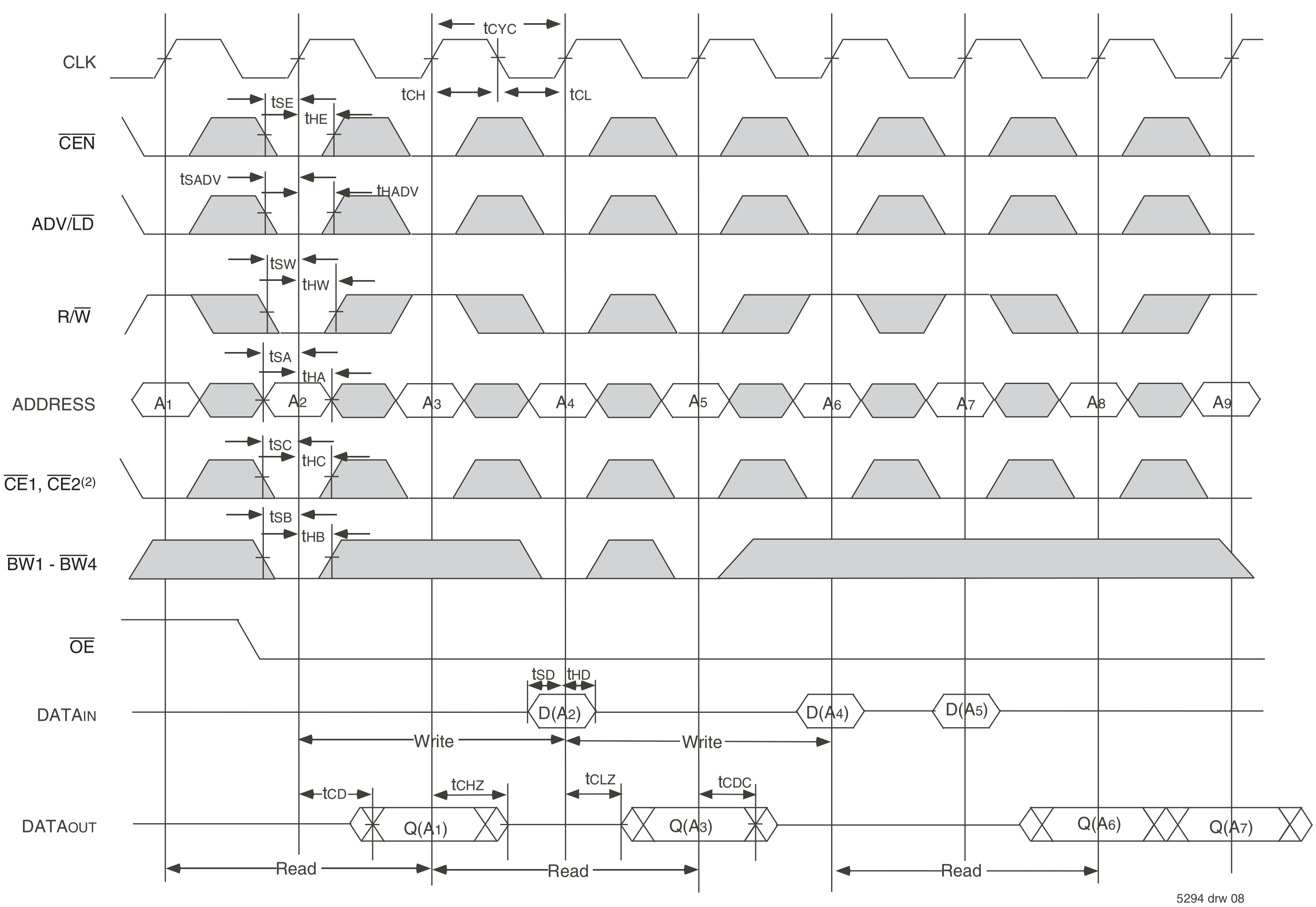
Timing Waveform of Write Cycles(1,2,3,4,5)



NOTES:

1. D (A_1) represents the first input to the external address A_1. D (A_2) represents the first input to the external address A_2; D (A_{2+1}) represents the next input data in the burst sequence of the base address A_2, etc. where address bits A_0 and A_1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
4. R/$\overline{W}$ is don't care when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals ($\overline{BW}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

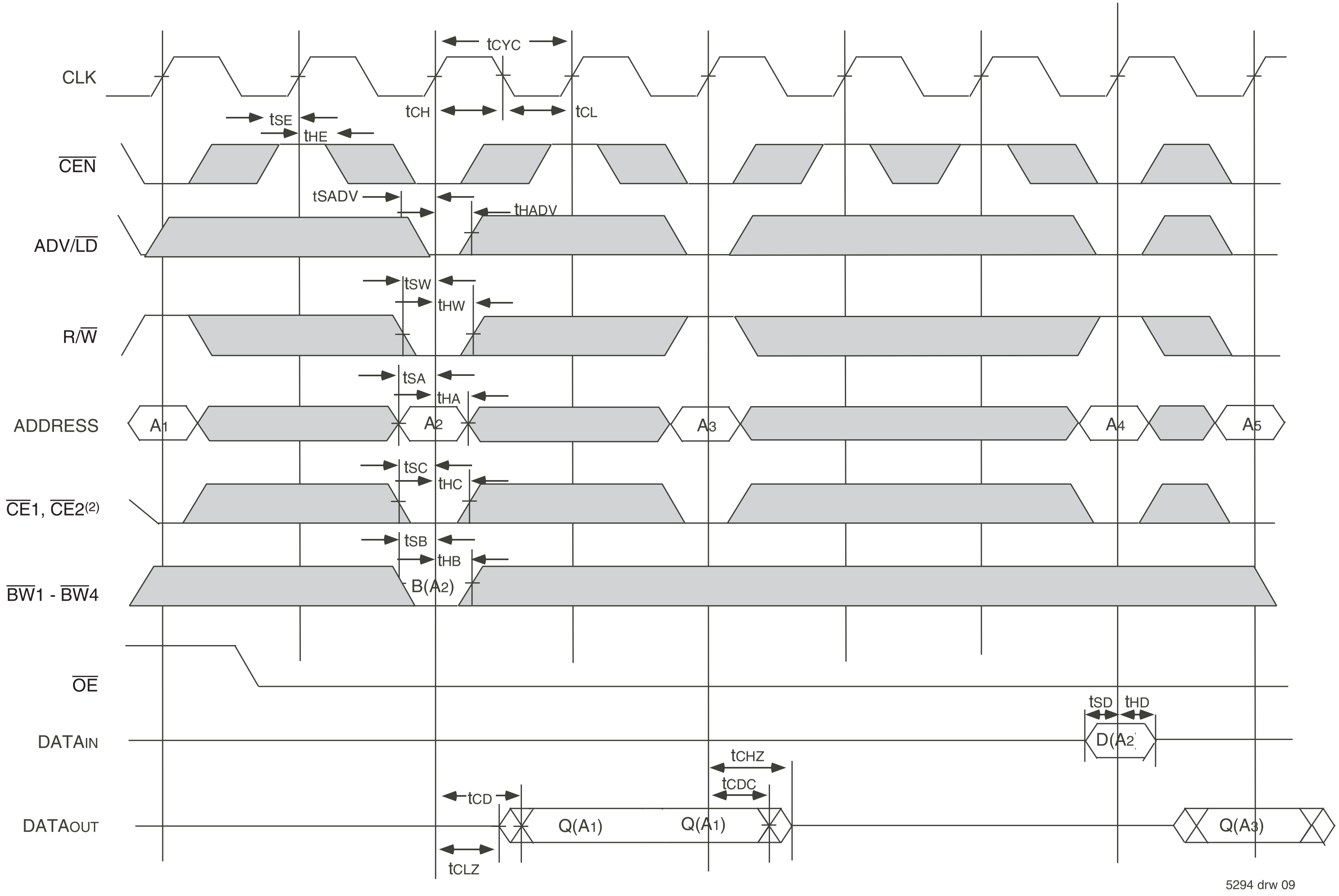
Timing Waveform of Combined Read and Write Cycles (1,2,3)



NOTES:

1. Q (A_1) represents the first output from the external address A_1. D (A_2) represents the input data to the SRAM corresponding to address A_2.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. Individual Byte Write signals ($\overline{BW}x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $R/\overline{W}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

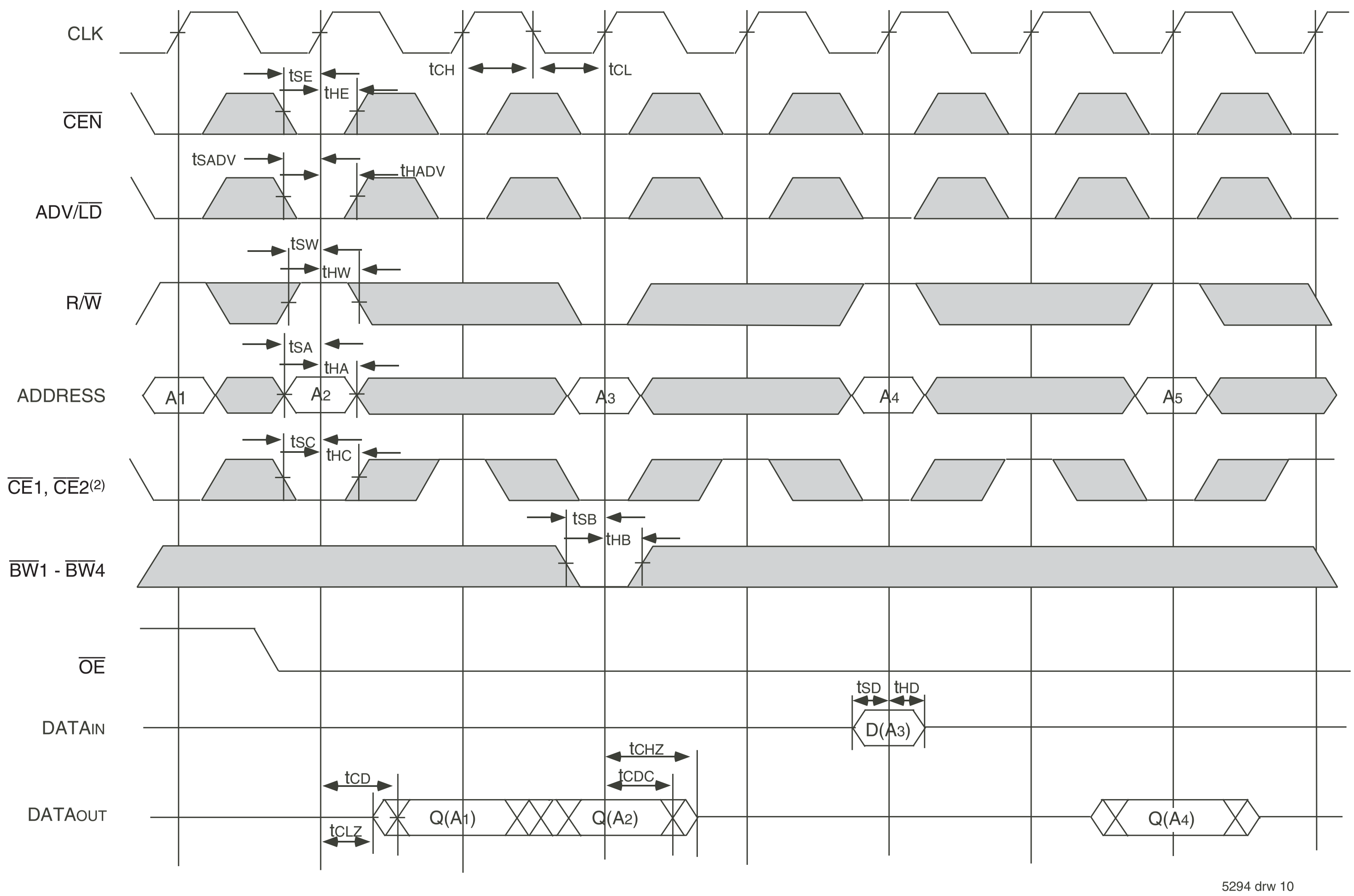
Timing Waveform of $\overline{\text{CEN}}$ Operation(1,2,3,4)



NOTES:

1. Q (A_1) represents the first output from the external address A_1. D (A_2) represents the input data to the SRAM corresponding to address A_2.
2. CE_2 timing transitions are identical but inverted to the $\overline{CE}_1$ and $\overline{CE}_2$ signals. For example, when $\overline{CE}_1$ and $\overline{CE}_2$ are LOW on this waveform, CE_2 is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BW}}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{\text{W}}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

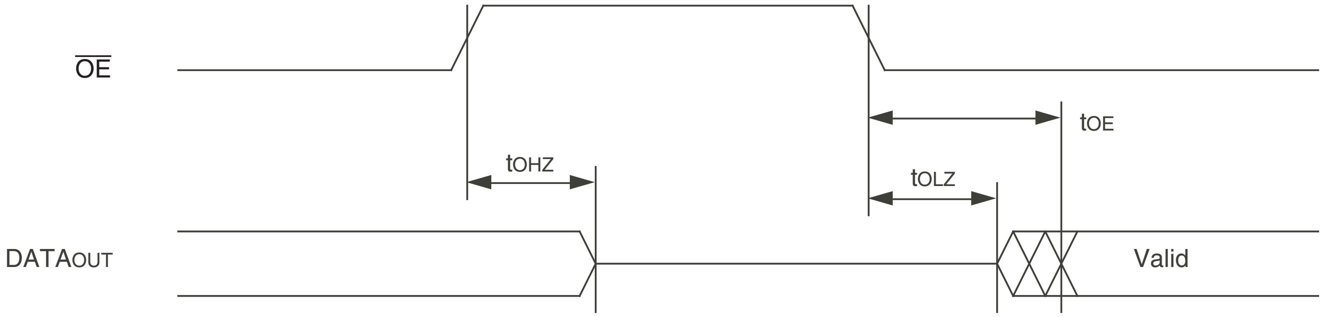
Timing Waveform of $\overline{\text{CS}}$ Operation(1,2,3,4)



NOTES:

1. Q (A1) represents the first output from the external address A1. D (A3) represents the input data to the SRAM corresponding to address A3.
2. CE2 timing transitions are identical but inverted to the $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ signals. For example, when $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$ are LOW on this waveform, CE2 is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BW}}$x) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{\text{W}}$ signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{OE}}$ Operation(1)

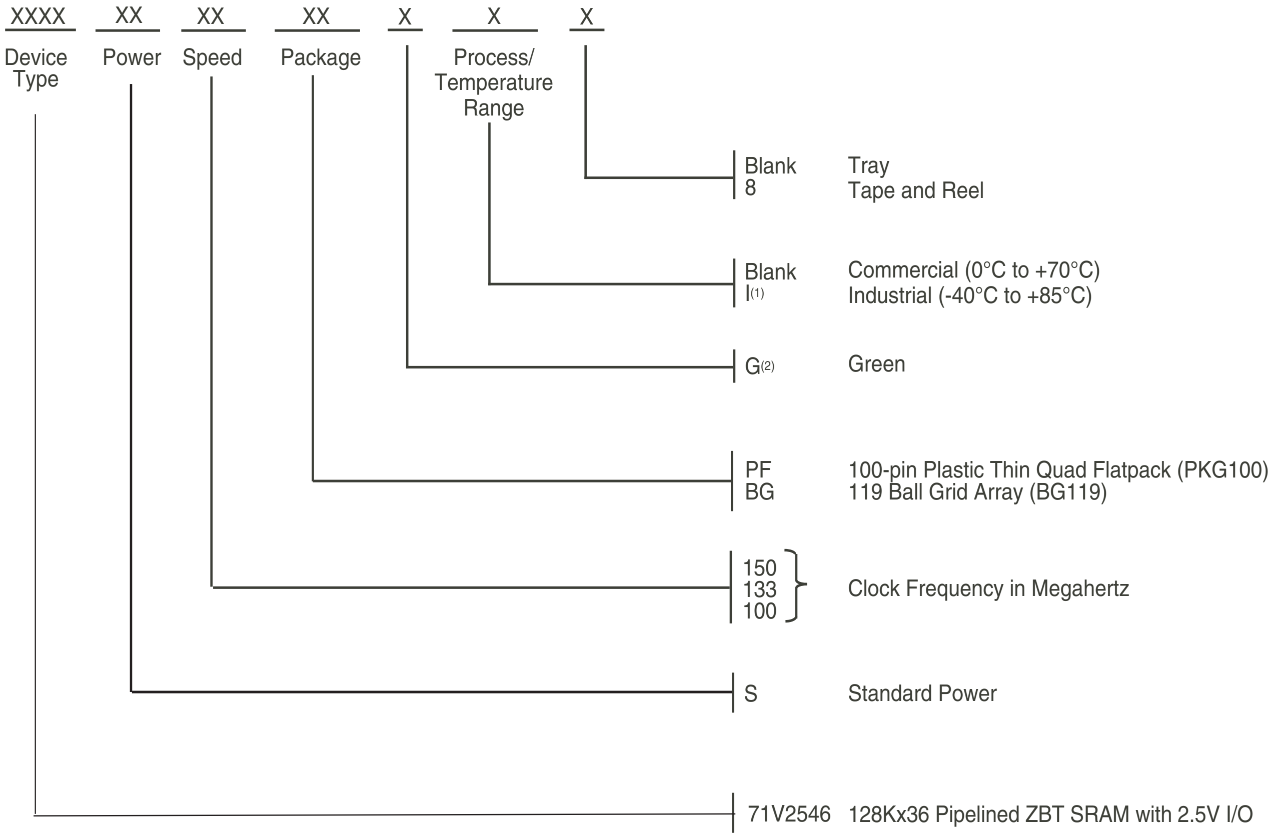


5294 drw 11

NOTE:

1. A read operation is assumed to be in progress.

Ordering Information



5294 drw 12

NOTES:

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Orderable Part Information

Speed (MHz)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
100	71V2546S100BG	BG119	PBGA	C
	71V2546S100BG8	BG119	PBGA	C
	71V2546S100BGI	BG119	PBGA	I
	71V2546S100BGI8	BG119	PBGA	I
	71V2546S100PFG	PKG100	TQFP	C
	71V2546S100PFG8	PKG100	TQFP	C
133	71V2546S133BG	BG119	PBGA	C
	71V2546S133BG8	BG119	PBGA	C
	71V2546S133BGI	BG119	PBGA	I
	71V2546S133BGI8	BG119	PBGA	I
	71V2546S133PFG	PKG100	TQFP	C
	71V2546S133PFG8	PKG100	TQFP	C
150	71V2546S150BG	BG119	PBGA	C
	71V2546S150BG8	BG119	PBGA	C
	71V2546S150PFG	PKG100	TQFP	C
	71V2546S150PFG8	PKG100	TQFP	C

Datasheet Document History

12/31/99		Created preliminary datasheet from 71V2556 and 71V2558 datasheets. Changed t_{CDC}, t_{CLZ}, and t_{CHZ} minimums from 1.0ns to 1.5ns.
03/04/00	Pg. 1,14,15,22	Add 150 MHz speed grade offering
05/02/00	Pg. 5,6	Insert clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 5,6,7	Clarify note on TQFP and BGA pin configurations; corrected typo in pinout
	Pg. 6	Add BGA capacitance table
	Pg. 21	Add 100 pin TQFP Package Diagram Outline
05/26/00	Pg. 23	Add new package offering, 13 x 15mm 165 fBGA
		Correct 119 BGA Package Diagram Outline
07/26/00	Pg. 5-8	Add ZZ, sleep mode reference note to BG119, PK100 and BQ165 pinouts
	Pg. 8	Update BQ165 pinout
	Pg. 23	Update BG119 Package Diagram Outline dimensions
10/25/00		Remove Preliminary status from datasheet
	Pg. 8	Add reference note to pin N5 on BQ165, reserved for JTAG pin $\overline{TRST}$
05/20/02	Pg. 1-8,15,22,23,27	Added JTAG "SA" version functionality and updated ZZ pin descriptions and notes
09/30/04	Pg. 7	Updated pin configuration for the 119 BGA-reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).
02/23/07	Pg. 27	Added X step die generation to data sheet ordering information.
05/27/10	Pg. 24	Added "Restricted hazardous substance device" to the ordering information.
04/11/11	Pg. 1-21	Removed 71V2548 (EOL), fBGA 165 pin, and JTAG information.
	Pg. 13	Added 150MHz data for Industrial information.
	Pg. 20	Added Tape and Reel to Ordering information and updated description of Restricted hazardous substance device to Green.
08/12/20	Pg. 1 - 22	Rebranded as Renesas datasheet
	Pg. 1 & 20	Updated Industrial temp range and green availability
	Pg. 4 - 5	Updated package codes
	Pg. 20	Removed X generation die stepping from Ordering Information
	Pg. 21	Added Orderable Part Information table

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