

HIGH SPEED 4K X 8 DUAL-PORT STATIC RAM WITH SEMAPHORE

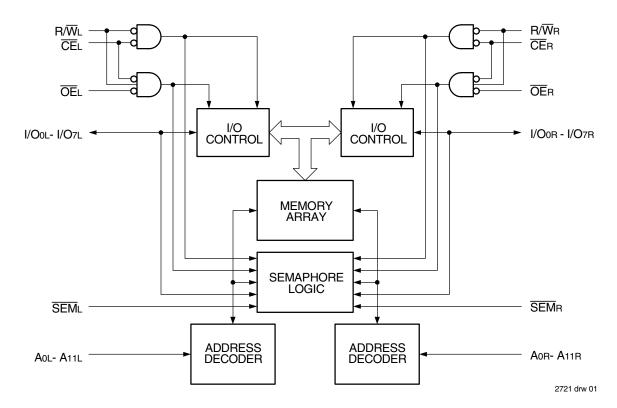
71342SA/LA

Features

- High-speed access
 - Commercial: 20ns(max.)
 - Industrial: 25ns (max.)
- Low-power operation
 - IDT71342LA Active: 700mW (typ.) Standby: 1mW (typ.)
- Fully asynchronous operation from either port

- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention (LA only)
- TTL-compatible; single 5V (±10%) power supply
- Available in plastic packages
- Industrial temperature range (-40°C to +85°C) is available for selected speeds

Functional Block Diagram



JULY 2019

Description

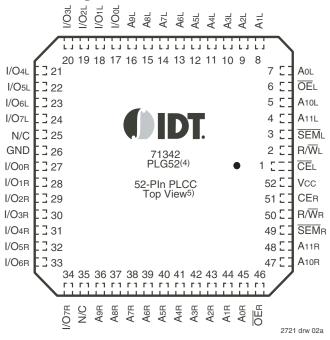
The IDT71342 is a high-speed 4K \times 8 Dual-Port Static RAM with full on-chip hardware support of semaphore signalling between the two ports.

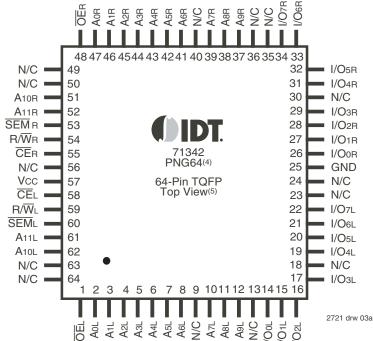
The IDT71342 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any

time. An automatic power down feature, controlled by $\overline{\text{CE}}$ and $\overline{\text{SEM}}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ HIGH).

Fabricated using CMOS high-performance technology, this device typically operates on only 700mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery. The device is packaged in either a 64-pin TQFP or a 52-pin PLCC.

Pin Configurations(1,2,3)





- 1. All Vcc pins must be connected to power supply.
- All GND pins must be connected to ground supply.
- PLG52 package body is approximately .79 in x .79 in x .17 in.
 PNG64 package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	°C
Tstg	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.5	W
Іоит	DC Output Current	50	mA

NOTES

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may
 cause permanent damage to the device. This is a stress rating only and functional
 operation of the device at these or any other conditions above those indicated in the
 operational sections of this specification is not implied. Exposure to absolute
 maximum rating conditions for extended periods may affect reliability.
- 2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc +10%.

Capacitance⁽¹⁾ (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
Соит	Output Capacitance	Vout = 3dV	10	pF
				2721 tbl 02

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

Maximum Operating

Temperature and Supply Voltage (1,2)

		1 J	3
Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES:

2721 tbl 01

2721 thl 03

1. This is the parameter Ta. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	٧
VIH	Input High Voltage	2.2	_	6.0(2)	٧
VIL	Input Low Voltage	-0.5 ⁽¹⁾	_	0.8	V

2721 tbl 04

NOTES:

- 1. V_{IL} (min.) \geq -1.5V for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage (Vcc = 5V ± 10%)

			71342SA		7134		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
Iu	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, $Vin = 0V$ to Vcc	_	10	-	5	μΑ
ILO	Output Leakage Current	$\overline{CE} = VIH$, VOUT = 0V to VCC	_	10	_	5	μΑ
Vol	Output Low Voltage	IoL = 6mA	_	0.4	_	0.4	V
		IoL = 8mA	_	0.5	_	0.5	V
Voh	Output High Voltage	IOH = -4mA	2.4	_	2.4	_	V

NOTE:

1. At Vcc ≤ 2.0V input leakages are undefined.

2721 tbl 05

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ (Vcc = 5.0V ± 10%)

		Tapping vertage italis			71342 Com'l		71342 Com'l		7134: Com'l		
Symbol	Parameter	Test Condition	Versi	on	Typ. ⁽²⁾	Max.	Тур.(2)	Max.	Typ. ⁽²⁾	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CE = VIL, Outputs Disabled	COM'L	SA LA	170 170	280 240	160 160	280 240	150 150	260 200	mA
		SEM = Don't Care f = fmax ⁽³⁾	IND	SA LA			160 160	310 260	150 150	300 250	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{\text{CEL}}$ and $\overline{\text{CER}} = \text{VIH}$ $\overline{\text{SEML}} = \overline{\text{SEMR}} \ge \text{VIH}$ $f = f_{MAX}(3)$	COM'L	SA LA	25 25	80 80	25 25	80 50	25 25	75 45	mA
	Level inputs)	† = 1MAX ⁽³⁾	IND	SA LA			25 25	100 80	25 25	75 55	
ISB2	Standby Current (One Port - TTL Level Inputs)	\overline{CE} " = VIL and \overline{CE} " = VIH Active Port Outputs Disabled, $f=f_{MAX}^{(3)}$	COM'L	SA LA	105 105	180 150	95 95	180 150	85 85	170 140	mA
	Level inputs)	I=IMAX**/	IND	SA LA	-		95 95	210 170	85 85	200 160	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports CEL and CER ≥ Vcc - 0.2V, Vin ≥ Vcc - 0.2V or Vin ≤ 0.2V	COM'L	SA LA	1.0 0.2	15 4.5	1.0 0.2	15 4.0	1.0 0.2	15 4.0	mA
	Civios Level ilipuis)	$\frac{VIN \ge VCC - 0.2V}{SEML} = \frac{SEMR}{SEMR} \ge VCC - 0.2V$ $f = 0^{(3)}$	IND	SA LA			1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	One Port CE"A" or CE"B" > VCC - 0.2V	COM'L	SA LA	105 105	170 130	95 95	170 120	85 85	150 110	mA
	Tolvios Level Ilipus)	$ \begin{array}{l} \underline{\text{VIN}} > \text{VCC} - \underline{0}.2\text{V or VIN} \leq 0.2\text{V} \\ \overline{\text{SEML}} = \overline{\text{SEMR}} \geq \text{VCC} - 0.2\text{V} \\ \text{Active Port Outputs Disabled,} \\ f = f_{\text{MAX}^{(3)}} \end{array} $	IND	SA LA			95 95	210 190	85 85	190 130	

					71342 Com'l		7134: Com'l		71342 Com'l		
Symbol	Parameter	Test Condition	Versi	on	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CE = VIL, Outputs Disabled	COM'L	SA LA	140 140	240 200	140 140	240 200	140 140	240 200	mA
		$ \overline{SEM} = Don't Care f = fMax(3) $	IND	SA LA	_		140 140	270 220			
ISB1	Standby Current (Both Ports - TTL Level Inputs)		COM'L	SA LA	25 25	70 40	25 25	70 40	25 25	70 40	mA
	Lever inputs)		IND	SA LA			25 25	70 50			
ISB2	Standby Current (One Port - TTL	$\overline{CE}^*A^* = V_{IL}$ and $\overline{CE}^*B^* = V_{IH}$ Active Port Outputs Disabled,	COM'L	SA LA	75 75	160 130	75 75	160 130	75 75	160 130	mA
	Level Inputs)	f=fmax ⁽³⁾	IND	SA LA			75 75	180 150			
ISB3	Full Standby Current (Both Ports -	Both Ports CEL and CER ≥ Vcc - 0.2V,	COM'L	SA LA	1.0 0.2	15 4.0	1.0 0.2	15 4.0	1.0 0.2	15 4.0	mA
	CMOS Level Inputs)		IND	SA LA	_	_	1.0 2.0	30 10		_	
ISB4	Full Standby Current (One Port -	One Port CE"A" or CE"B" > Vcc - 0.2V	COM'L	SA LA	75 75	150 100	75 75	150 100	75 75	150 100	mA
	CMOS Level Inputs)		IND	SA LA	_	_	75 75	170 120	_	_	

- 1. 'X' in part number indicates power rating (SA or LA).
- 2. Vcc = 5V, TA = +25°C for typical, and parameters are not production tested.
- 3. fmax = 1/trc = All inputs cycling at f = 1/trc (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby IsB3.



Data Retention Characteristics

(LA Version Only) VLC = 0.2V, VHC = VCC - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. ⁽¹⁾	Max.	Unit
VDR	Vcc for Data Retention	_		2.0		_	V
ICCDR	Data Retention Current	$VCC = 2V, \overline{CE} \ge VHC$	COM'L. & IND.	_	100	1500	μΑ
tcdr ⁽³⁾	Chip Deselect to Data Retention Time	SEM ≥ VHC		0	1	-	ns
tR ⁽³⁾	Operation Recovery Time	VIN > VHC or < VLC		trc ⁽²⁾		_	ns

NOTES: 2721 tbl 07

- 1. Vcc = 2V, TA = +25°C, and are not production tested.
- 2. trc = Read Cycle Time.
- 3. This parameter is guaranteed by device characterization, but is not production tested.

AC Test Conditions

710 TOST OUTBITTOTIS	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2721 tbl 08

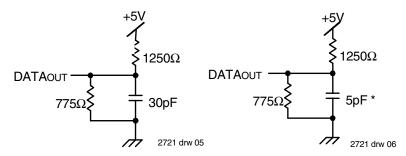


Figure 1. AC Output Test Load

Figure 2. Output Test Load (for tLZ, tHz, twz, tow) *Including scope and jig



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

			2X20 I Only	71342X25 Com'l & Ind		71342X35 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
trc	Read Cycle Time	20	_	25	_	35	_	ns
taa	Address Access Time	_	20	_	25	_	35	ns
tace	Chip Enable Access Time ⁽³⁾	_	20	_	25	_	35	ns
taoe	Output Enable Access Time	_	15	_	15	_	20	ns
tон	Output Hold from Address Change	0	_	0	_	0	_	ns
tLZ	Output Low-Z Time ^(1,2)	0	_	0	_	0	_	ns
thz	Output High-Z Time ^(1,2)		15	_	15	_	20	ns
tpu	Chip Enable to Power Up Time ⁽²⁾	0	_	0	_	0	_	ns
tpd	Chip Disable to Power Down Time ⁽²⁾	_	50	_	50	_	50	ns
tsop	SEM Flag Update Pulse (OE or SEM)	10	_	10	_	15	_	ns
twdd	Write Pulse to Data Delay ⁽⁴⁾	_	40		50		60	ns
todo	Write Data Valid to Read Data Delay ⁽⁴⁾	_	30		30		35	ns
tsaa	Semaphore Address Access Time	_	_		25		35	ns

2721 tbl 09a

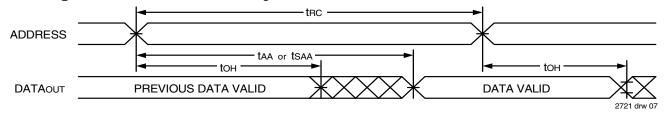
			71342X45 71342X55 Com'l Only Com'l Only		71342X70 Com'l Only			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
trc	Read Cycle Time	45	_	55	_	70	_	ns
taa	Address Access Time	_	45	_	55	_	70	ns
tace	Chip Enable Access Time (3)	_	45		55	_	70	ns
taoe	Output Enable Access Time	_	25	_	30	_	40	ns
tон	Output Hold from Address Change	0	_	0	_	0	_	ns
tLZ	Output Low-Z Time ^(1,2)	5	_	5	_	5	_	ns
tHZ	Output High-Z Time ^(1,2)	_	20	_	25	_	30	ns
tpu	Chip Enable to Power Up Time ⁽²⁾	0	_	0		0	_	ns
tpD	Chip Disable to Power Down Time (2)		50	_	50	_	50	ns
tsop	SEM Flag Update Pulse (OE or SEM)	15	_	20		20	_	ns
twdd	Write Pulse to Data Delay ⁽⁴⁾		70	_	80	_	90	ns
todo	Write Data Valid to Read Data Delay ⁽⁴⁾		45	_	55	_	70	ns
tsaa	Semaphore Address Access Time		45		55		70	ns

2721 tbl 09b

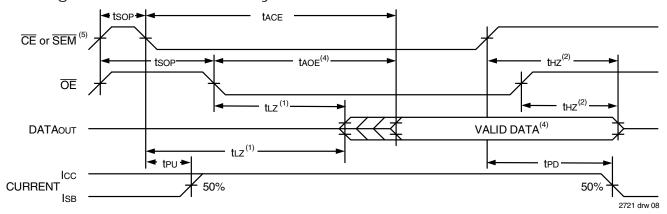
- 1. Transition is measured 0mV from Low or High-impedance voltage with the Ouput Test Load (Figure 2).
- This parameter is guaranteed by device characterization, but is not production tested.
 To access SRAM, CE = VIL, SEM = VIH. To access semaphore, CE = VIH, and SEM = VIL.
 'X' in part number indicates power rating (SA or LA).
- 5. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".



Timing Waveform of Read Cycle No. 1, Either Side(1,2,4)



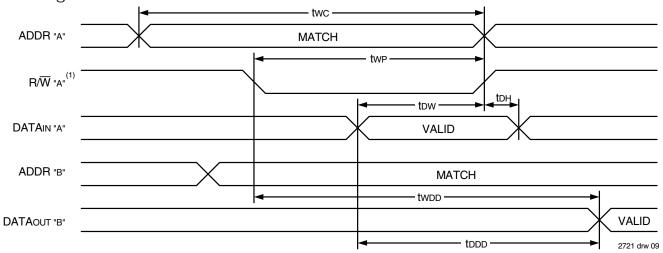
Timing Waveform of Read Cycle No. 2, Either Side(1,3)



NOTES:

- 1. Timing depends on which signal is asserted last, $\overline{\text{OE}}$ or $\overline{\text{CE}}$.
- 2. Timing depends on which signal is de-asserted first, $\overline{\sf OE}$ or $\overline{\sf CE}$.
- 3. $R/\overline{W} = VIH$ and $\overline{OE} = VIL$, unless otherwise noted.
- 4. Start of valid data depends on which timing becomes effective last; taoe, tace, or taa
- 5. To access SRAM, $\overline{CE} = VIL$ and $\overline{SEM} = VIH$. To access semaphore, $\overline{CE} = VIH$ and $\overline{SEM} = VIL$. tax is for SRAM Address Access and tsxx is for Semaphore Address Access.

Timing Waveform of Write with Port-to-Port Read(2,3)



- 1. Write cycle parameters should be adhered to, in order to ensure proper writing.
- 2. $\overline{CE}L = \overline{CE}R = VIL$. $\overline{CE}"B" = VIL$.
- 3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".



AC Electrical Characteristics Over the Operating Temperature Supply Voltage⁽⁵⁾

			2X20 I Only		2X25 & Ind	71342X35 Com'l Only		
Symbol	Parameter	Min.	Мах.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time	20	_	25		35	_	ns
tew	Chip Enable to End-of-Write ⁽³⁾	15	_	20		30	_	ns
taw	Address Valid to End-of-Write	15	_	20	_	30	_	ns
tas	Address Set-up Time	0	_	0	_	0	_	ns
twp	Write Pulse Width	15	_	20		25	_	ns
twr	Write Recovery Time	0	_	0		0	_	ns
tow	Data Valid to End-of-Write	15	_	15	_	20	_	ns
tHZ	Output High-Z Time ^(1,2)	_	15	_	15	_	20	ns
tон	Data Hold Time ⁽⁴⁾	0	_	0		3	_	ns
twz	Write Enable to Output in High-Z ^(1,2)		15	_	15	_	20	ns
tow	Output Active from End-of-Write ^(1,2,4)	3	_	3	_	3	_	ns
tswr	SEM Flag Write to Read Time	10	_	10		10		ns
tsps	SEM Flag Contention Window	10	_	10		10		ns

2721 tbl 10a

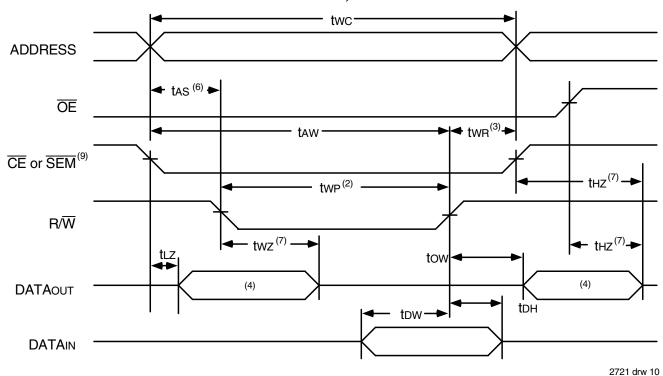
		71342X45 Com'l Only		71342X55 Com'l Only		71342X70 Com'l Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time	45	_	55	_	70	_	ns
tew	Chip Enable to End-of-Write ⁽³⁾	40	_	50	_	60	_	ns
taw	Address Valid to End-of-Write	40	_	50		60	_	ns
tas	Address Set-up Time	0	_	0	_	0	_	ns
twp	Write Pulse Width	40	_	50	_	60	_	ns
twr	Write Recovery Time	0	_	0	_	0	_	ns
tow	Data Valid to End-of-Write	20	_	25	_	30	_	ns
tHZ	Output High-Z Time ^(1,2)	_	20	_	25	_	30	ns
tDH	Data Hold Time ⁽⁴⁾	3	_	3	_	3	_	ns
twz	Write Enable to Output in High-Z ^(1,2)	_	20	_	25	_	30	ns
tow	Output Active from End-of-Write ^(1,2,4)		_	3	_	3	_	ns
tswr	SEM Flag Write to Read Time	10	_	10	_	10	_	ns
tsps	SEM Flag Contention Window	10	_	10		10	_	ns

NOTES:

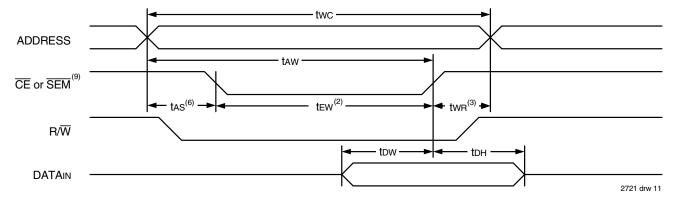
2721 tbl 10b

- Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
 This parameter is guaranteed by device characterization but is not production tested.
- 3. To access SRAM, \overline{CE} = VIL and \overline{SEM} = VIH. To access semaphore, \overline{CE} = VIH and \overline{SEM} = VIL. Either condition must be valid for the entire tew time.
- The specification for toh must be met by the device supplying write data to the SRAM under all operating conditions. Although toh and tow values will vary over voltage and temperature, the actual toh will always be smaller than the actual tow.
- 5. 'X' in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/w CONTROLLED TIMING(1,5,8)



Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing^(1, 5)

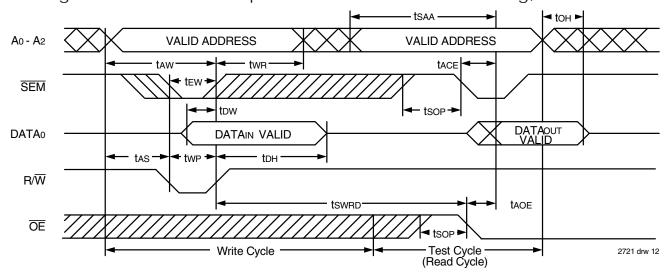


- 1. R/W or CE must be HIGH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of either \overline{CE} or $\overline{SEM} = V_{IL}$ and $R/\overline{W} = V_{IL}$.
- 3. two is measured from the earlier of $\overline{\text{CE}}$ or R/\overline{W} going HIGH to the end-of-write cycle.
- 4. During this period, the I/O pins are in the output state, and input signals must not be applied.
- 5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal ($\overline{\text{CE}}$ or R/\overline{W}) is asserted last.
- 7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
- 8. If $\widetilde{\mathsf{OE}}$ is LOW during a $\mathsf{R}/\overline{\mathsf{W}}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If $\widetilde{\mathsf{OE}}$ is HIGH during an $\mathsf{R}/\overline{\mathsf{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 9. To access SRAM, $\overline{\text{CE}} = \text{V}_{\text{IL}}$ and $\overline{\text{SEM}} = \text{V}_{\text{IH}}$. To access semaphore, $\overline{\text{CE}} = \text{V}_{\text{IH}}$ and SEM = V_{IL}. Either condition must be valid for the entire tew time.



Industrial and Commercial Temperature Ranges

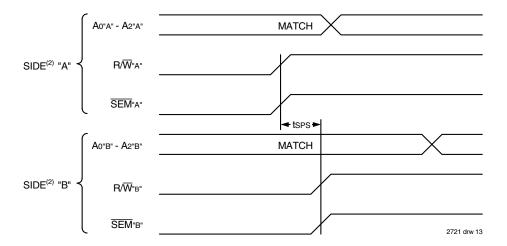
Timing Waveform of Semaphore Read After Write Timing, Either Side(1)



NOTE

1. $\overline{CE} = VIH$ for the duration of the above timing (both write and read cycle).

Timing Waveform of Semaphore Condition^(1,3,4)



- 1. Dor = Dol = Vil., $\overline{\text{CE}}$ R = $\overline{\text{CEL}}$ = ViH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
- 2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 3. This parameter is measured from the point where $R\overline{W}$ "A" or \overline{SEM} "A" goes HIGH until $R\overline{W}$ "B" or \overline{SEM} "B" goes HIGH.
- 4. If tsps is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

Functional Description

The IDT71342 is an extremely fast Dual-Port 4K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAMs and can be read from or written to at the same time, with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port SRAM. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$, the Dual-Port SRAM enable, and $\overline{\text{SEM}}$, the semaphore enable. The $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ are both HIGH.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and

test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the $\overline{\text{SEM}}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{\text{OE}}$, and $\overline{\text{R/W}}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through the address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Truth Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (\overline{SEM}) and output enable (\overline{OE}) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal (\overline{SEM}) or \overline{OE} to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Truth Table II). As an example, assume a processor writes a zero in the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore

request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all

Truth Table I — Non-Contention Read/Write Control(2)

Left or Right Port ⁽¹⁾			t Port ⁽¹⁾		
R/W	CE	SEM	ŌĒ	D0-7	Function
Х	Н	Н	Х	Z	Port Disabled and in Power Down Mode
Н	Н	L	L	DATAout	Data in Semaphore Flag Output on Port
Х	Х	Х	Н	Z	Output Disabled
1	Н	L	Χ	DATAIN	Port Data Bit Do Written Into Semaphore Flag
Н	L	Н	L	DATAOUT	Data in Memory Output on Port
L	L	Н	Χ	DATAIN	Data on Port Written Into Memory
Х	L	L	Χ	_	Not Allowed

NOTE: 2721 tbl 11

- 1. AOL A11L ≠ AOR A11R.
- 2. "H" = VIH, "L" = VIL, "X" = Don't Care, "Z" = High-Impedance.

Truth Table II — Example Semaphore Procurement Sequence(1,2,3)

Functions	Do - D15 Left	Do - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:

2721 tbl 12

- 1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.
- 2. There are eight semaphore flags written to via I/Oo and read from all I/O's. These eight semaphores are addressed by Ao-A2.
- 3. CE = VIH, SEM = VIL to access the semaphores. Refer to the semaphore Read/Write Control Truth Table.

semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores-Some examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's Dual-Port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of the memory.

To take a resource, in this example the lower 2K of Dual-Port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the

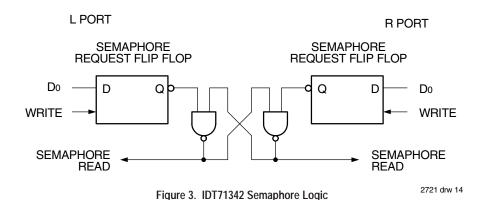
two processors to swap 2K blocks of Dual-Port RAM with each other.

The blocks do not have to by any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

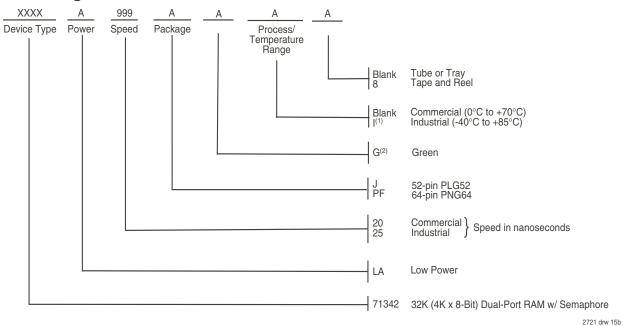
Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.





Ordering Information



NOTES

- 1. Contact your local sales office for industrial temprange for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office.
 LEAD FINISH (containing SnPb) are obsolete excluding BGA and Hermetic packages. Product Discontinuation Notice PDN# SP-17-02 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	71342LA20JG	PLG52	PLCC	С
	71342LA20JG8	PLG52	PLCC	С
	71342LA20PFG	PNG64	TQFP	С
	71342LA20PFG8	PNG64	TQFP	С
25	71342LA25JGI	PLG52	PLCC	Ī
	71342LA25JGI8	PLG52	PLCC	Ī
	71342LA25PFGI	PNG64	TQFP	Ī
	71342LA25PFGl8	PNG64	TQFP	Ī



Datasheet Document History

Page 14

01/12/99:		Initiated datasheet document history
		Converted to newformat
		Cosmetic and typographical corrections
		Added additional notes to pin configurations
06/09/99:		Changed drawing format
10/01/99:		Added Industrial Temperature Ranges and removed corresponding notes
11/10/99:		Replaced IDT Logo
12/22/99:	Page 1	Made corrections to drawing
06/26/00:	Page 3	Increased storage temperature parameters
	3	Clarified Taparameter
	Page 4	DC Electrical parameters-changed wording from "open" to "disabled"
	3	Changed ±500mV to 0mV in notes
01/12/00:	Pages 1 & 2	Moved "Description" to page 2 and adjusted page layouts
	Page 1	Added "(LA only)" to paragraph
	Page 2	Fixed J52 package description in notes
	Page 8	Replaced bottom table with correct 10b table
01/29/09:	Page 14	Removed "IDT" from orderable part number
09/26/12:	Page 1	Industrial speed access update for 35 & 55
	Page 2	Removed "IDT's" from description text
	Page 3	Removed footnote notation from PT in Absolute Maximum Ratings table 01
	Page 4, 6 & 8	Replaced "& Ind" with Com'l only for speed grades 35 & 55 in the DC Chars, AC Chars Read & Write tables
	· ·	06a, 06b, 09a, 09b, 10a & 10b
	Page 12	Added the word "system" to How the Semaphore Flags Work paragraph
	Page 12	Corrected equation for footnote 1 . Changed symbol "=" to - and "1" to not equal (≠)
	Page 14	Added T&R and Green indicators to the ordering information as well as updated the "commercial only"
	_	offering for speed grades 35 & 55
03/15/19:	Page 2	The package codes J52-1 & PN64-1 changed to PLG52 & PNG64
	ŭ	Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
07/12/19:	Page 2	Rotated PLG52 PLCC and PNG64 TQFP pin configurations to accurately reflect pin 1 orientation
	5 44	

Added Orderable Part Information

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