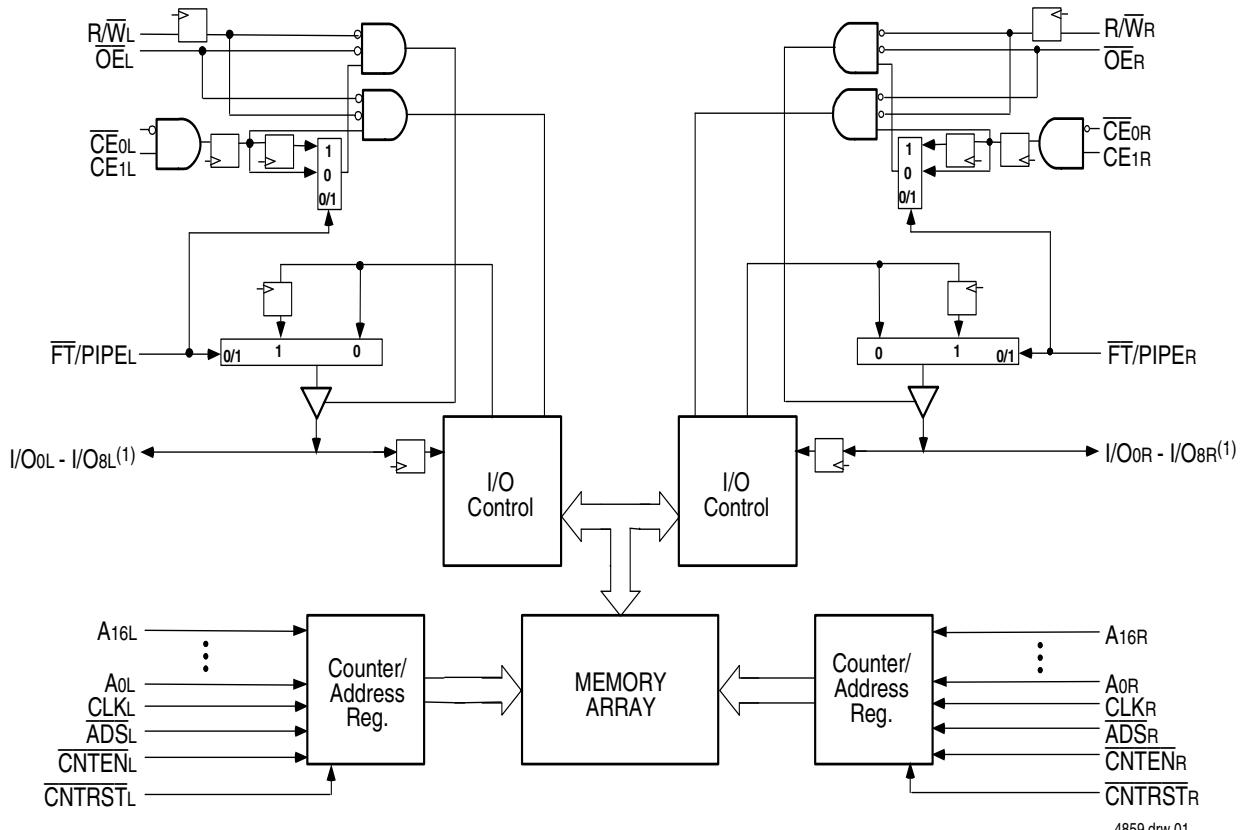


### Features:

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
  - Commercial: 9ns (max.)
  - Industrial: 9ns (max.)
- ◆ Low-power operation
  - IDT70V9199/099L
  - Active: 500mW (typ.)
  - Standby: 1.5mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either port via the **FT/PIPE** pins
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Counter enable and reset features
- ◆ Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 9 ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 15ns cycle time, 66 MHz operation in Pipelined output mode
- ◆ LVTTL- compatible, single 3.3V ( $\pm 0.3V$ ) power supply
- ◆ Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available for selected speeds
- ◆ Available in a 100-pin Thin Quad Flatpack (TQFP)
- ◆ Green parts available, see ordering information

### Functional Block Diagram



**NOTE:**

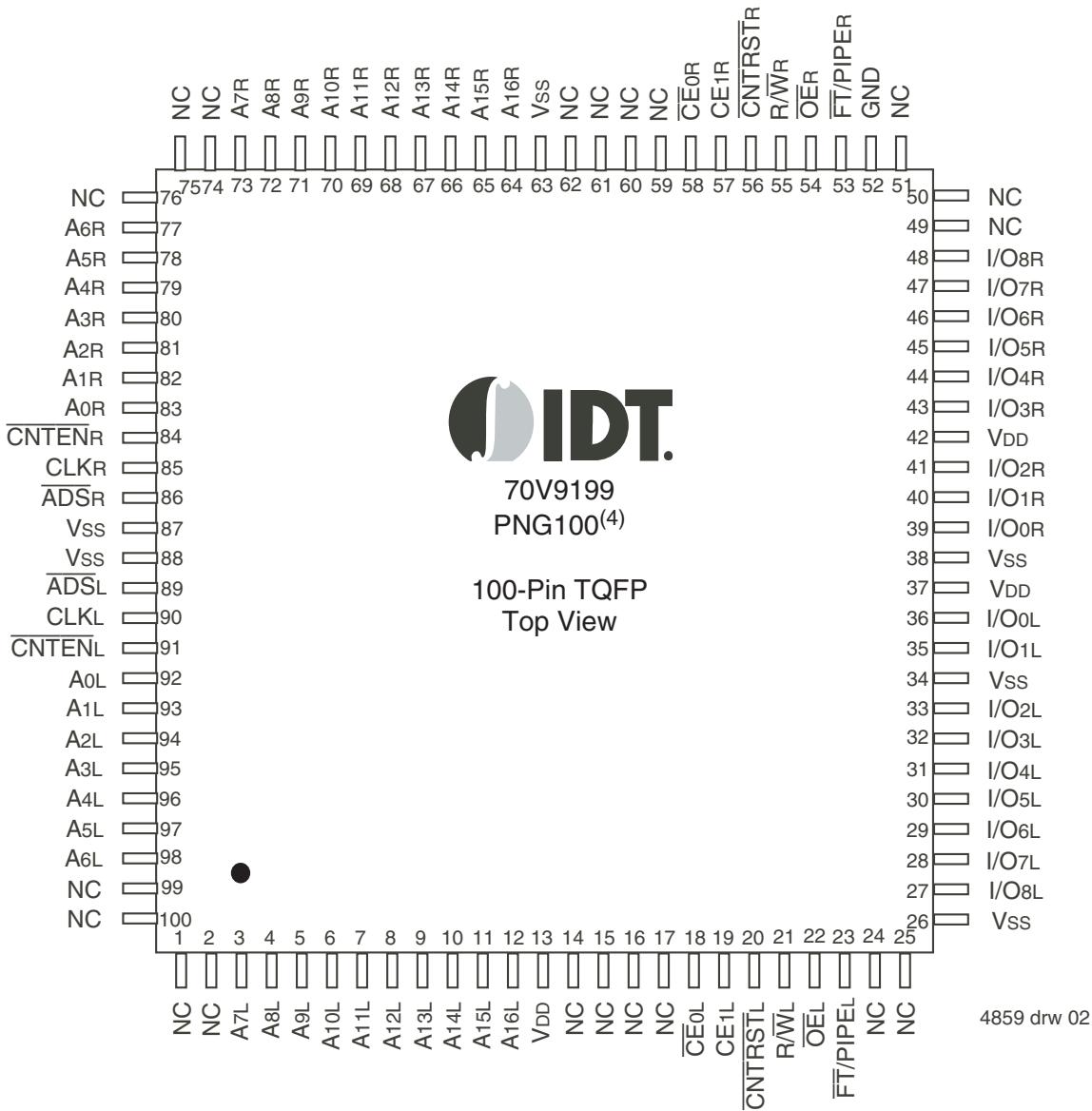
1. I/O0x - I/O7x for IDT70V9099.

## Description:

The IDT70V9199/099 is a high-speed 128K x9/x8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9199/099 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by  $\overline{CE}_0$  and  $CE_1$ , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 500mW of power.

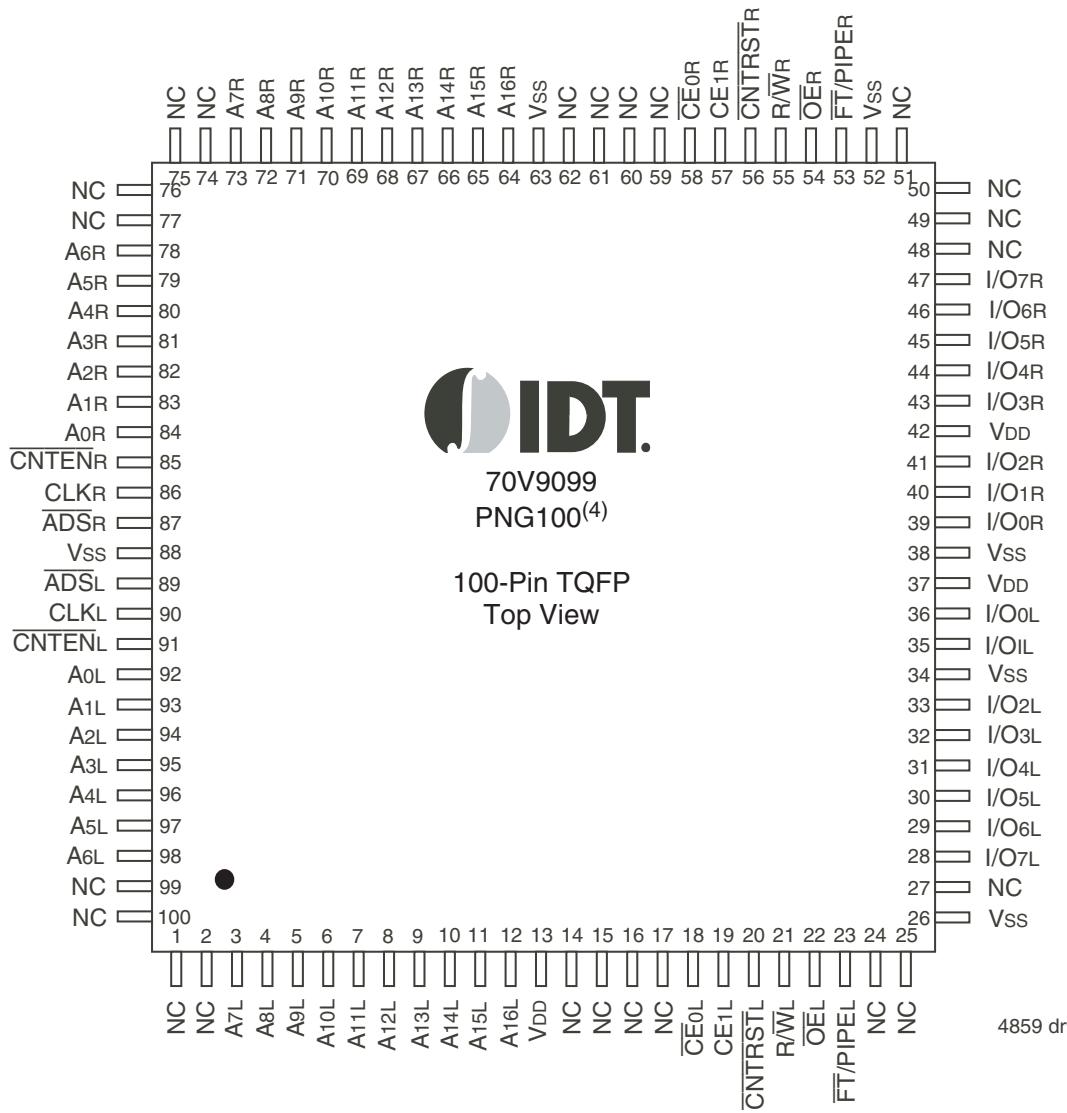
## Pin Configuration<sup>(1,2,3)</sup>



### NOTES:

1. All  $V_{DD}$  pins must be connected to power supply.
2. All  $V_{SS}$  pins must be connected to ground supply.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

## Pin Configuration<sup>(1,2,3)</sup>(con't.)



859 drw 02a

## NOTES:

NOTES:

1. All Vdd pins must be connected to power supply.
2. All Vss pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

## Pin Names

Left Port	Right Port	Names
$\overline{CE0L}$ , $CE1L$	$\overline{CE0R}$ , $CE1R$	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A0L - A16L$	$A0R - A16R$	Address
$I/O0L - I/O8L^{(1)}$	$I/O0R - I/O8R^{(1)}$	Data Input/Output
CLKL	CLKR	Clock
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter Reset
$\overline{FT}/PIPEL$	$\overline{FT}/PIPER$	Flow-Through / Pipeline
VDD		Power (3.3V)
VSS		Ground (0V)

4859 tbl 01

## NOTE:

1.  $I/O_0 - I/O_7$  for IDT70V9099.

Truth Table I—Read/Write and Enable Control<sup>(1,2,3)</sup>

$\overline{OE}$	CLK	$\overline{CE}_0$	CE1	$R/\overline{W}$	$I/O_{0-8}^{(4)}$	MODE
X	$\uparrow$	H	X	X	High-Z	Deselected—Power Down
X	$\uparrow$	X	L	X	High-Z	Deselected—Power Down
X	$\uparrow$	L	H	L	DATA <sub>IN</sub>	Write
L	$\uparrow$	L	H	H	DATA <sub>OUT</sub>	Read
H	X	L	H	X	High-Z	Outputs Disabled

4859 tbl 02

## NOTES:

1. "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
2.  $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{CNTRST}$  = X.
3.  $\overline{OE}$  is an asynchronous input signal.
4.  $I/O_0 - I/O_7$  for IDT70V9099.

Truth Table II—Address Counter Control<sup>(1,2)</sup>

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	$I/O^{(3)}$	MODE
X	X	0	$\uparrow$	X	X	L <sup>(4)</sup>	D <sub>0</sub> (0)	Counter Reset to Address 0
An	X	An	$\uparrow$	L <sup>(4)</sup>	X	H	D <sub>0</sub> (n)	External Address Loaded into Counter
An	Ap	Ap	$\uparrow$	H	H	H	D <sub>0</sub> (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	$\uparrow$	H	L <sup>(5)</sup>	H	D <sub>0</sub> (p+1)	Counter Enabled—Internal Address generation

4859 tbl 03

## NOTES:

1. "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
2.  $\overline{CE}_0$  and  $\overline{OE}$  =  $V_{IL}$ ;  $CE1$  and  $R/\overline{W}$  =  $V_{IH}$ .
3. Outputs configured in Flow-Through Output mode; if outputs are in Pipelined mode the data out will be delayed by one cycle.
4.  $\overline{ADS}$  and  $\overline{CNTRST}$  are independent of all other signals including  $\overline{CE}_0$  and  $CE1$ .
5. The address counter advances if  $\overline{CNTEN} = V_{IL}$  on the rising edge of CLK, regardless of all other signals including  $\overline{CE}_0$  and  $CE1$ .

70V9199/099L

High-Speed 3.3V 128K x9/x8 Dual-Port Synchronous Pipelined Static RAM

Industrial and Commercial Temperature Ranges

Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature <sup>(2)</sup>	GND	VDD
Commercial	0°C to +70°C	0V	3.3V $\pm$ 0.3V
Industrial	-40°C to +85°C	0V	3.3V $\pm$ 0.3V

4859 tbl 04

## NOTES:

1. This is the parameter  $T_A$ . This is the "instant on" case temperature.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.0	—	V <sub>DD</sub> +0.3V <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

4859 tbl 05

## NOTES:

1.  $V_{IL} \geq -1.5V$  for pulse width less than 10 ns.
2.  $V_{TERM}$  must not exceed  $V_{DD} + 0.3V$ .

Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIA</sub> <sup>(3)</sup>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub>	Junction Temperature	+150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

4859 tbl 06

## NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2.  $V_{TERM}$  must not exceed  $V_{DD} + 0.3V$  for more than 25% of the cycle time or 10ns maximum, and is limited to  $\leq 20mA$  for the period of  $V_{TERM} \geq V_{DD} + 0.3V$ .
3. Ambient Temperature Under DC Bias. No AC Conditions. Chip deselect.

Capacitance<sup>(1)</sup>

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

4859 tbl 07

## NOTES:

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C<sub>OUT</sub> also references C<sub>IO</sub>.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V  $\pm$  0.3V)

Symbol	Parameter	Test Conditions	70V9199/099L		Unit
			Min.	Max.	
I <sub>U</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DD</sub> = 3.6V, V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	5	µA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $CE_1 = V_{IL}$ , V <sub>OUT</sub> = 0V to V <sub>DD</sub>	—	5	µA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +4mA	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	V

4859 tbl 08

## NOTE:

1. At  $V_{DD} \leq 2.0V$  input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(3)</sup> (V<sub>DD</sub> = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version	70V9199/099L9 Com'l & Ind		70V9199/099L12 Com'l Only		Unit	
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.		
I <sub>DD</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L = \overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	L	175	230	150	200	mA
			IND	L	180	240	—	—	
I <sub>SB1</sub>	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	L	40	65	30	50	mA
			IND	L	50	70	—	—	
I <sub>SB2</sub>	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f=f_{MAX}^{(1)}$	COM'L	L	110	145	95	130	mA
			IND	L	110	155	—	—	
I <sub>SB3</sub>	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	L	0.4	2	0.4	2	mA
			IND	L	0.4	2	—	—	
I <sub>SB4</sub>	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq V_{DD} - 0.2V^{(5)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	L	100	140	90	125	mA
			IND	L	100	155	—	—	

4859tbl09

## NOTES:

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^{\circ}C$  for Typ, and are not production tested.  $I_{DD DC}(f=0) = 90mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $CE_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DD} - 0.2V$   
 $\overline{CE}_X \geq V_{DD} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DD} - 0.2V$  or  $CE_{1X} \leq 0.2V$
- "X" represents "L" for left port or "R" for right port.

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2, and 3

4859 tbl 10

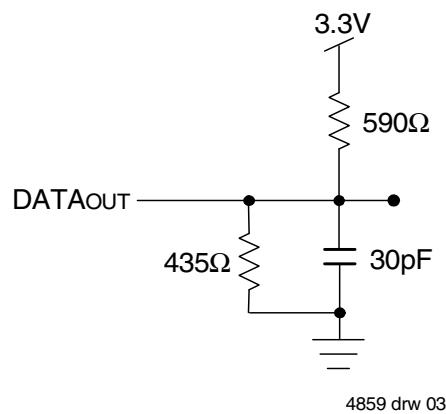


Figure 1. AC Output Test load.

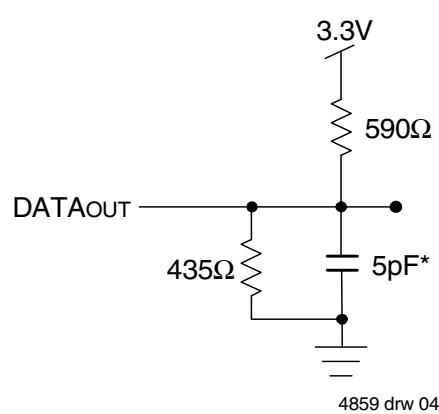


Figure 2. Output Test Load  
(For tcklz, tckhz, tolz, and tohz).  
\*Including scope and jig.

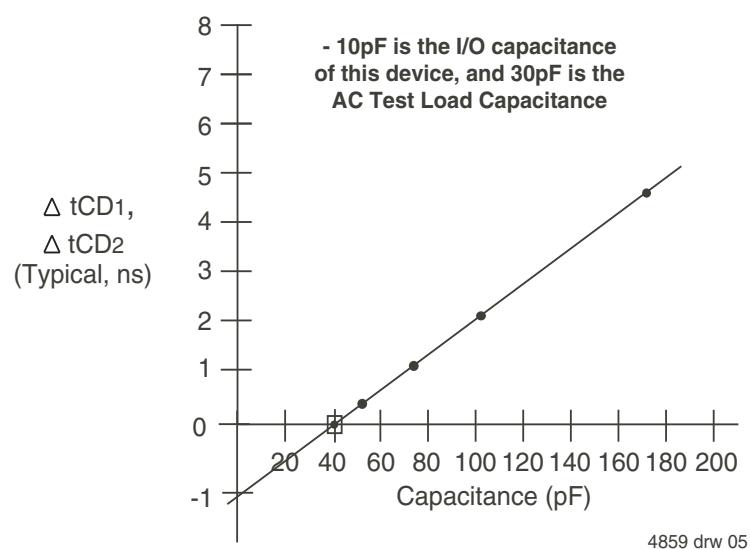


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range  
(Read and Write Cycle Timing)<sup>(3)</sup> (VDD = 3.3V ± 0.3V)

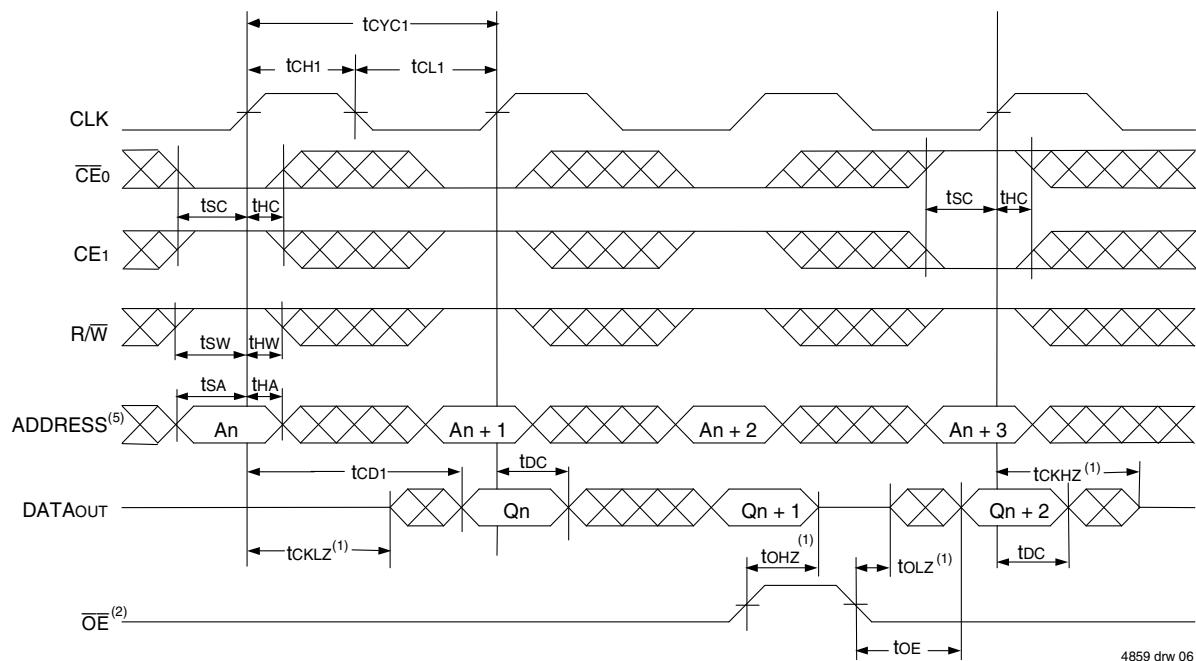
		70V9199/099L9 Com'l & Ind	70V9199/099L12 Com'l Only			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tCYC1	Clock Cycle Time (Flow-Through) <sup>(2)</sup>	25	—	30	—	ns
tCYC2	Clock Cycle Time (Pipelined) <sup>(2)</sup>	15	—	20	—	ns
tCH1	Clock High Time (Flow-Through) <sup>(2)</sup>	12	—	12	—	ns
tCL1	Clock Low Time (Flow-Through) <sup>(2)</sup>	12	—	12	—	ns
tCH2	Clock High Time (Pipelined) <sup>(2)</sup>	6	—	8	—	ns
tCL2	Clock Low Time (Pipelined) <sup>(2)</sup>	6	—	8	—	ns
tR	Clock Rise Time	—	3	—	3	ns
tF	Clock Fall Time	—	3	—	3	ns
tSA	Address Setup Time	4	—	4	—	ns
tHA	Address Hold Time	1	—	1	—	ns
tSC	Chip Enable Setup Time	4	—	4	—	ns
tHC	Chip Enable Hold Time	1	—	1	—	ns
tSW	R/W Setup Time	4	—	4	—	ns
tHW	R/W Hold Time	1	—	1	—	ns
tSD	Input Data Setup Time	4	—	4	—	ns
tHD	Input Data Hold Time	1	—	1	—	ns
tSAD	ADS Setup Time	4	—	4	—	ns
tHAD	ADS Hold Time	1	—	1	—	ns
tSCN	CNTEN Setup Time	4	—	4	—	ns
tHCN	CNTEN Hold Time	1	—	1	—	ns
tSRST	CNTRST Setup Time	4	—	4	—	ns
tHRST	CNTRST Hold Time	1	—	1	—	ns
toE	Output Enable to Data Valid	—	9	—	12	ns
tOLZ	Output Enable to Output Low-Z <sup>(1)</sup>	2	—	2	—	ns
tOHZ	Output Enable to Output High-Z <sup>(1)</sup>	1	7	1	7	ns
tCD1	Clock to Data Valid (Flow-Through) <sup>(2)</sup>	—	20	—	25	ns
tCD2	Clock to Data Valid (Pipelined) <sup>(2)</sup>	—	9	—	12	ns
tDC	Data Output Hold After Clock High	2	—	2	—	ns
tCKHZ	Clock High to Output High-Z <sup>(1)</sup>	2	9	2	9	ns
tCKLZ	Clock High to Output Low-Z <sup>(1)</sup>	2	—	2	—	ns
<b>Port-to-Port Delay</b>						
tCWDD	Write Port Clock High to Read Data Delay	—	35	—	40	ns
tCCS	Clock-to-Clock Setup Time	—	15	—	15	ns

4859 tbl 11

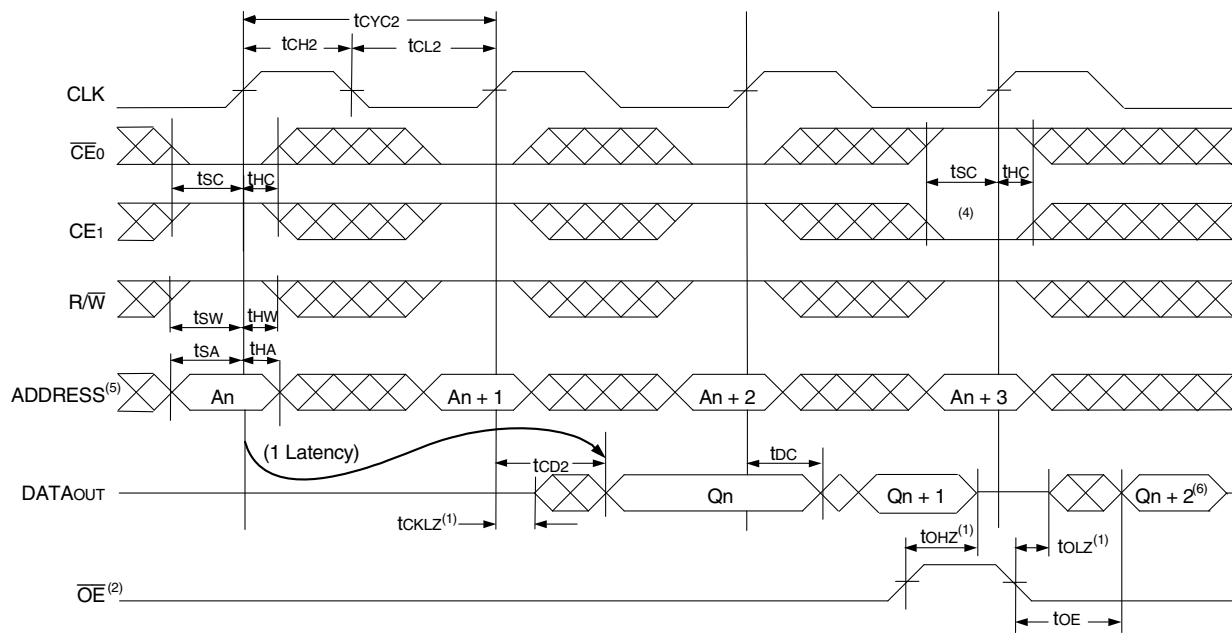
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (tCYC2, tCD2) apply to either or both the Left and Right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (tCYC1, tCD1) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (OE),  $\overline{FT}/PIPE_R$ , and  $\overline{FT}/PIPE_L$ .

## Timing Waveform of Read Cycle for Flow-Through Output ( $\overline{\text{FT}}/\text{PIPE}^{\text{"X"}}$ = $V_{IL}$ )<sup>(3,6)</sup>



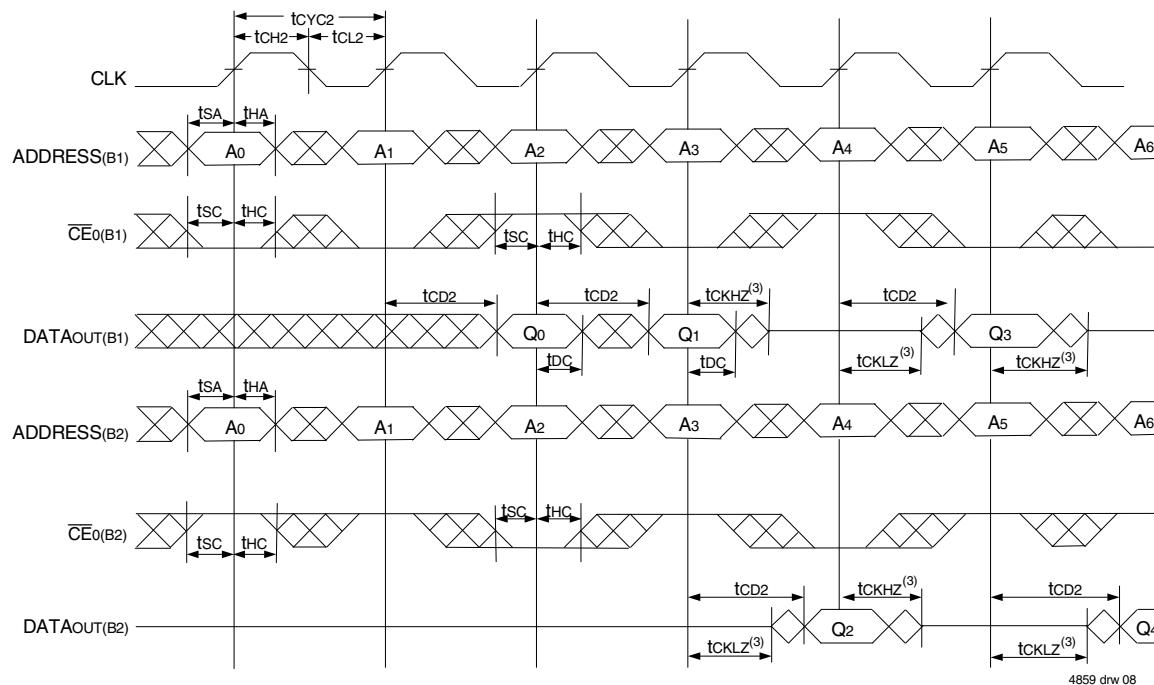
## Timing Waveform of Read Cycle for Pipelined Operation ( $\overline{\text{FT}}/\text{PIPE}^{\text{"X"}}$ = $V_{IH}$ )<sup>(3,6)</sup>



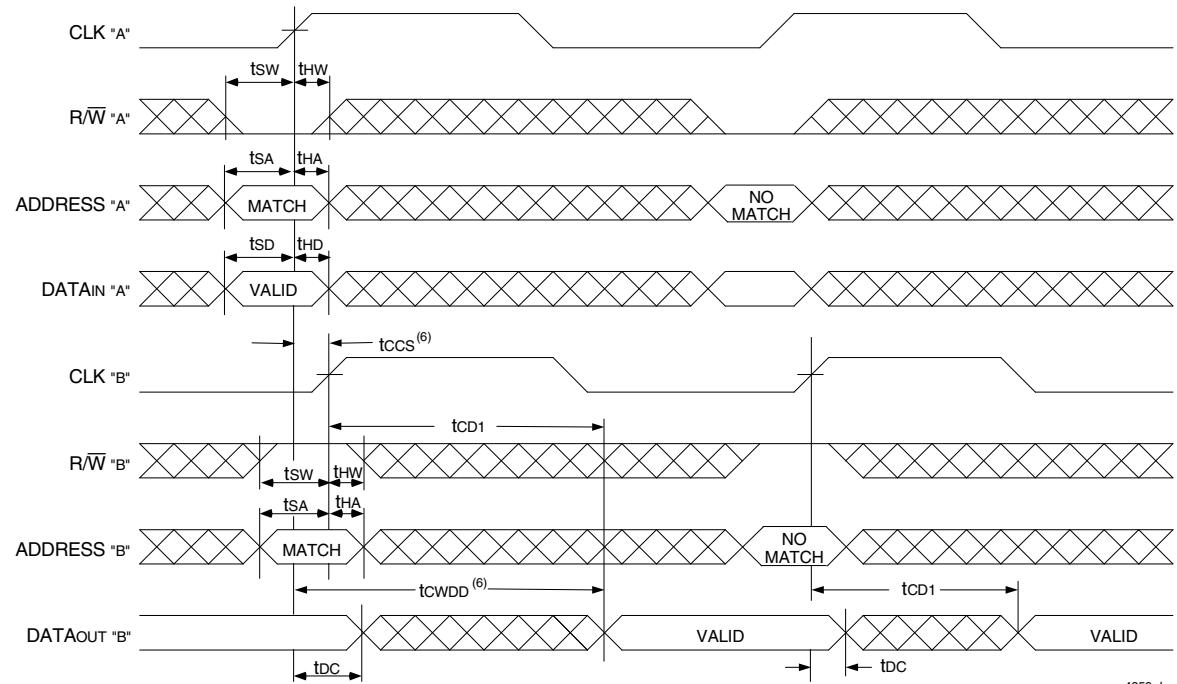
### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{\text{OE}}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3.  $\overline{\text{ADS}} = V_{IL}$  and  $\overline{\text{CNTRST}} = V_{IH}$ .
4. The output is disabled (High-Impedance state) by  $\overline{\text{CE0}} = V_{IH}$  or  $\text{CE1} = V_{IL}$  following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since  $\overline{\text{ADS}} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. 'X' here denotes Left or Right port. The diagram is with respect to that port.

## Timing Waveform of a Bank Select Pipelined Read<sup>(1,2)</sup>

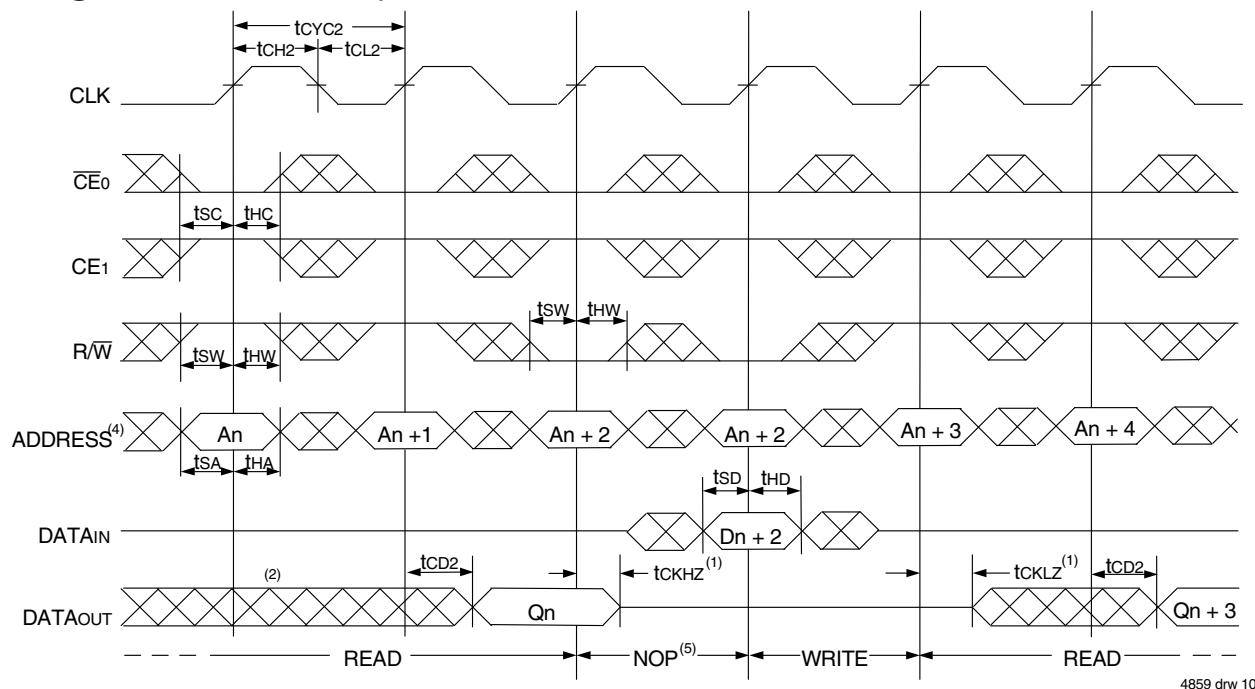
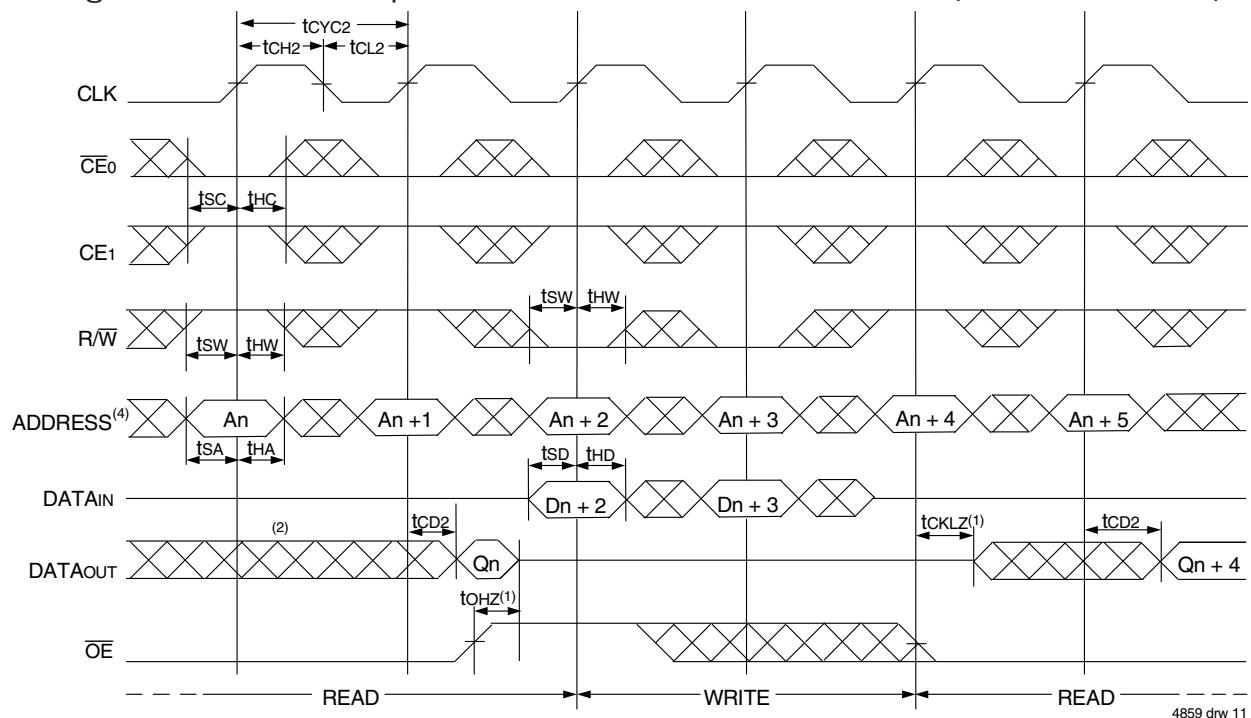


## Timing Waveform with Port-to-Port Flow-Through Read<sup>(4,5,7)</sup>



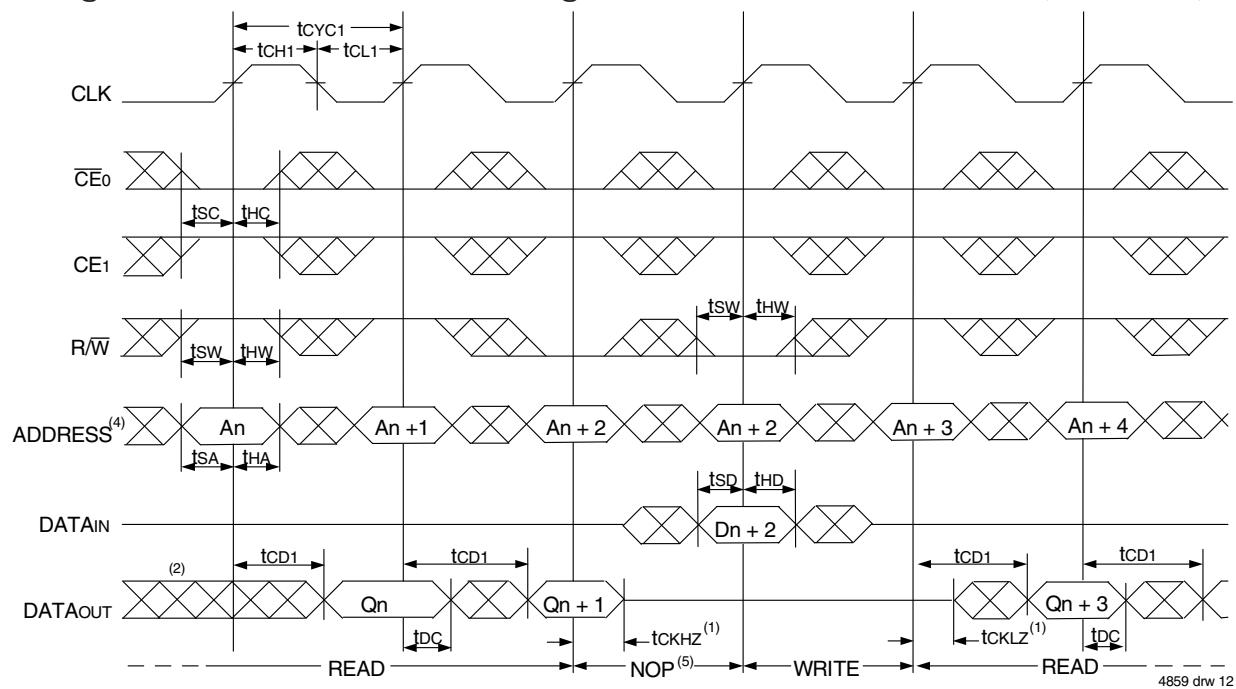
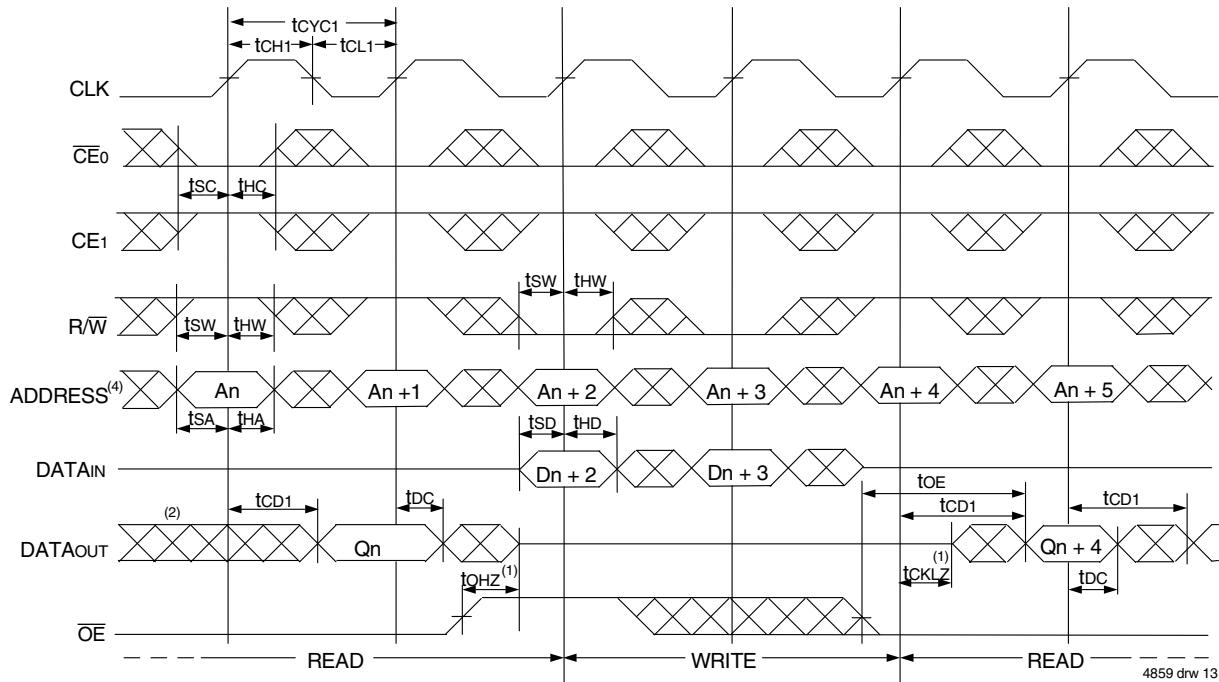
## NOTES:

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9199/099 for this waveform, and are setup for depth expansion in this example.  $ADDRESS_{(B1)} = ADDRESS_{(B2)}$  in this situation.
2.  $\overline{OE}$  and  $\overline{ADS} = VIL$ ;  $CE1_{(B1)}$ ,  $CE1_{(B2)}$ ,  $R/W$  and  $\overline{CNTRST} = VIH$ .
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4.  $\overline{CE}_0$  and  $\overline{ADS} = VIL$ ;  $CE1$  and  $\overline{CNTRST} = VIH$ .
5.  $\overline{OE} = VIL$  for the Right Port, which is being read from.  $\overline{OE} = VIH$  for the Left Port, which is being written to.
6. If  $tccs \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $t_{CWDD}$ .  
If  $tccs >$  maximum specified, then data from right port READ is not valid until  $tccs + t_{CD1}$ .  $t_{CWDD}$  does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(3)</sup>

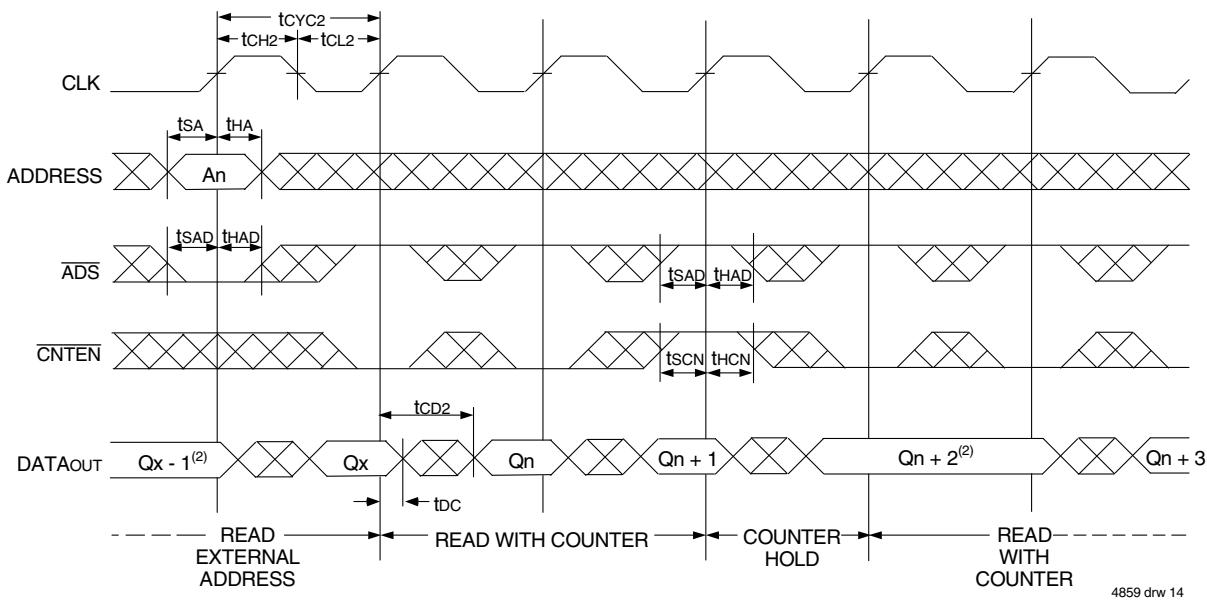
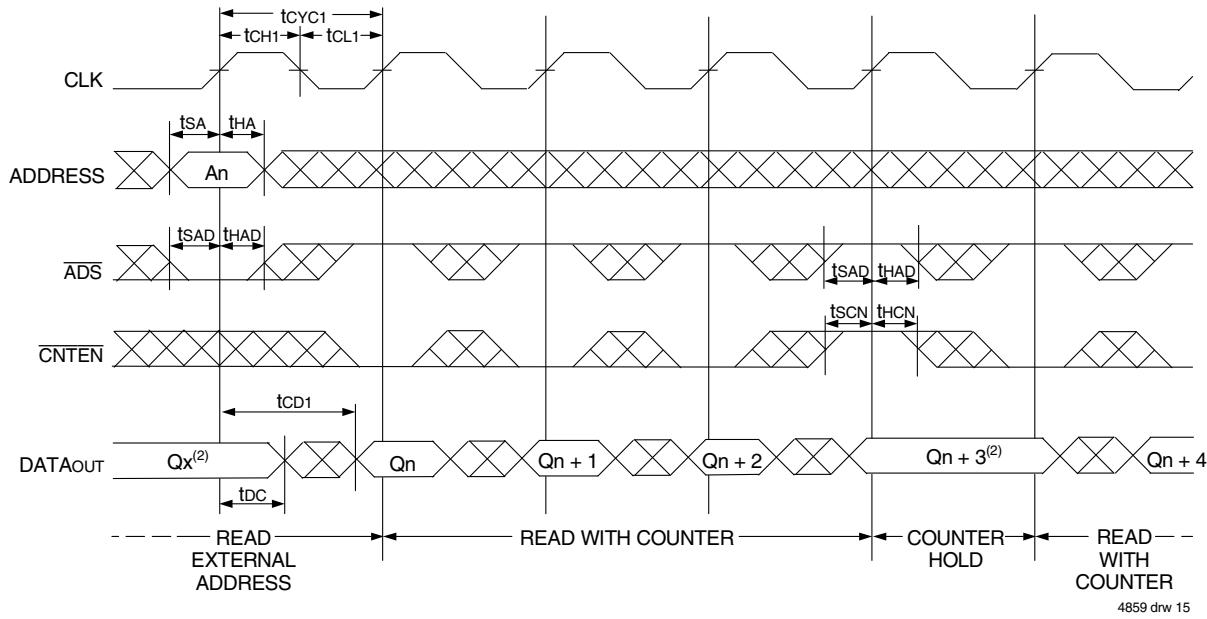
## NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$  and  $ADS = V_{IL}$ ;  $CE_1$  and  $CNTRST = V_{IH}$ . "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since  $ADS = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(3)</sup>

## NOTES:

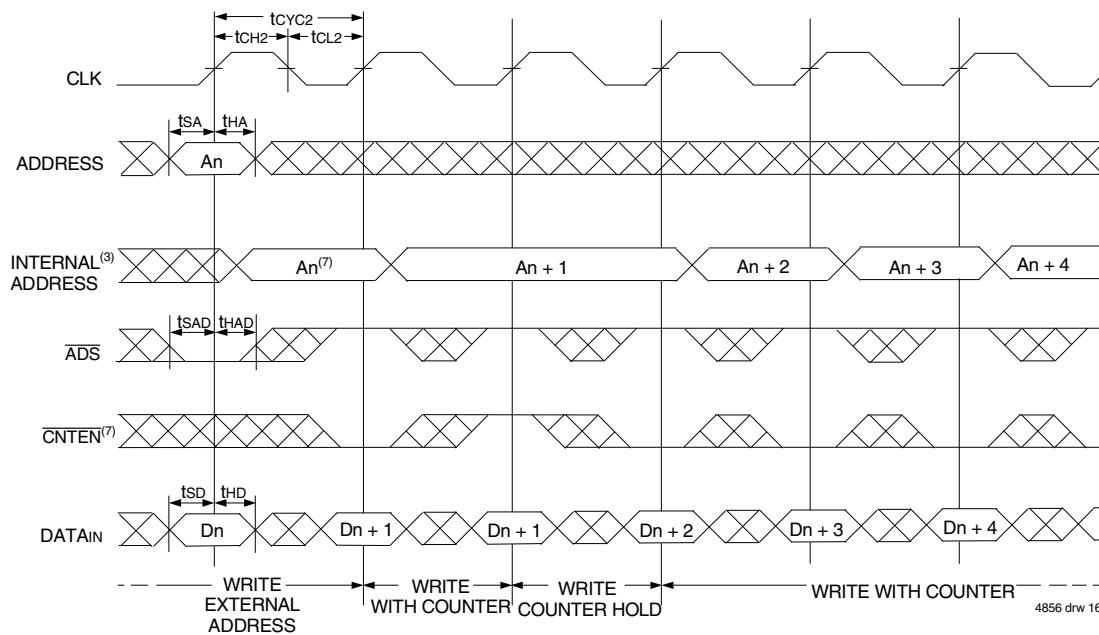
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$  and  $\overline{ADS} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST} = V_{IH}$ . "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>

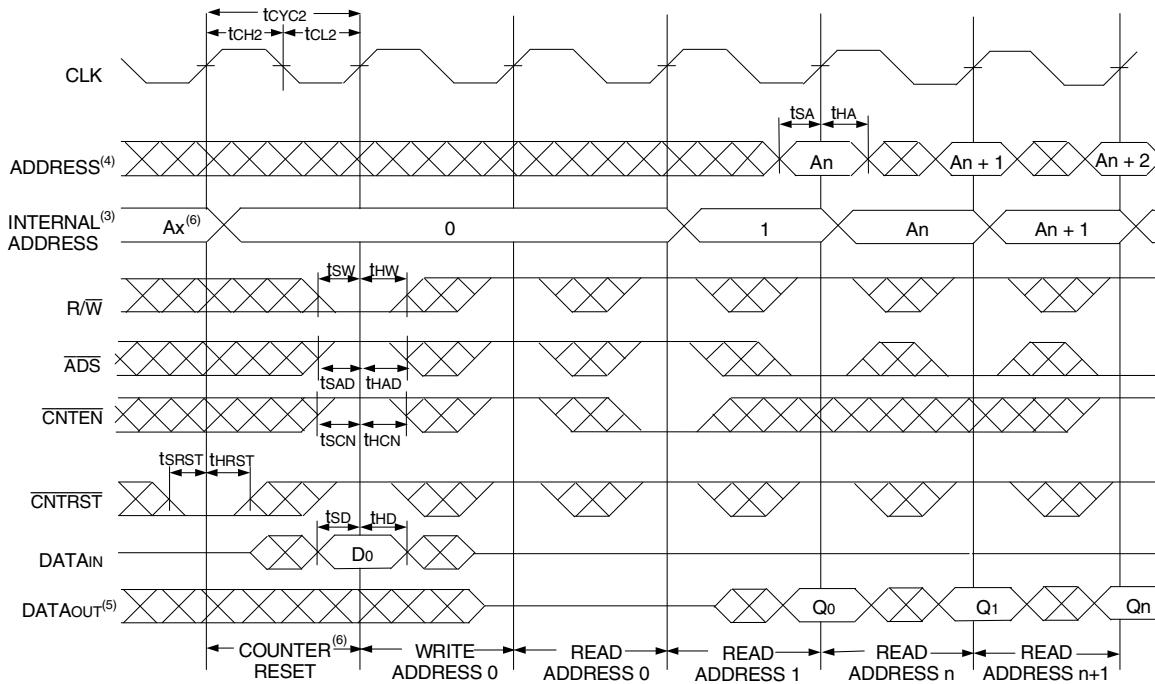
## NOTES:

1.  $\overline{CE}_0$  and  $\overline{OE}$  =  $V_{IL}$ ;  $CE_1$ ,  $R/W$ , and  $\overline{CNTRST}$  =  $V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)<sup>(1)</sup>



## Timing Waveform of Counter Reset (Pipelined Outputs)<sup>(2)</sup>



### NOTES:

1.  $\overline{CE}_0$  and  $\overline{R/W} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST} = V_{IH}$ .
2.  $\overline{CE}_0 = V_{IL}$ ;  $CE_1 = V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $ADS = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDRo will be accessed. Extra cycles are shown here simply for clarification.
7.  $CNTEN = V_{IL}$  advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

## Functional Description

The IDT70V9199/099 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to staff the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IL}$  and  $CE_1 = V_{IH}$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9199/099's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with  $\overline{CE}_0 = V_{IH}$  or  $CE_1 = V_{IL}$  to reactivate the outputs.

## Depth and Width Expansion

The IDT70V9199/099 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9199/099 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 18/16-bit or wider applications.

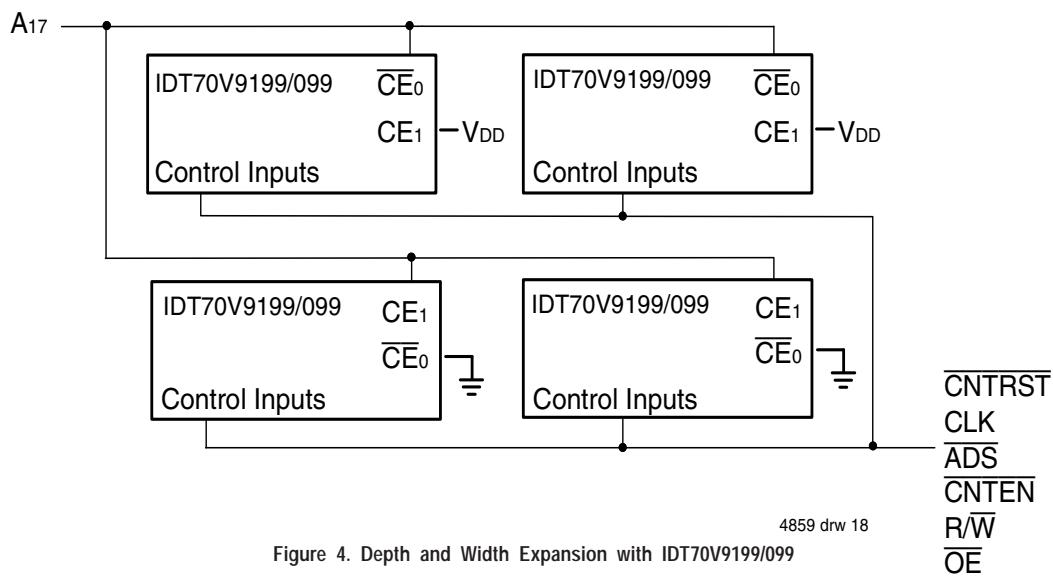
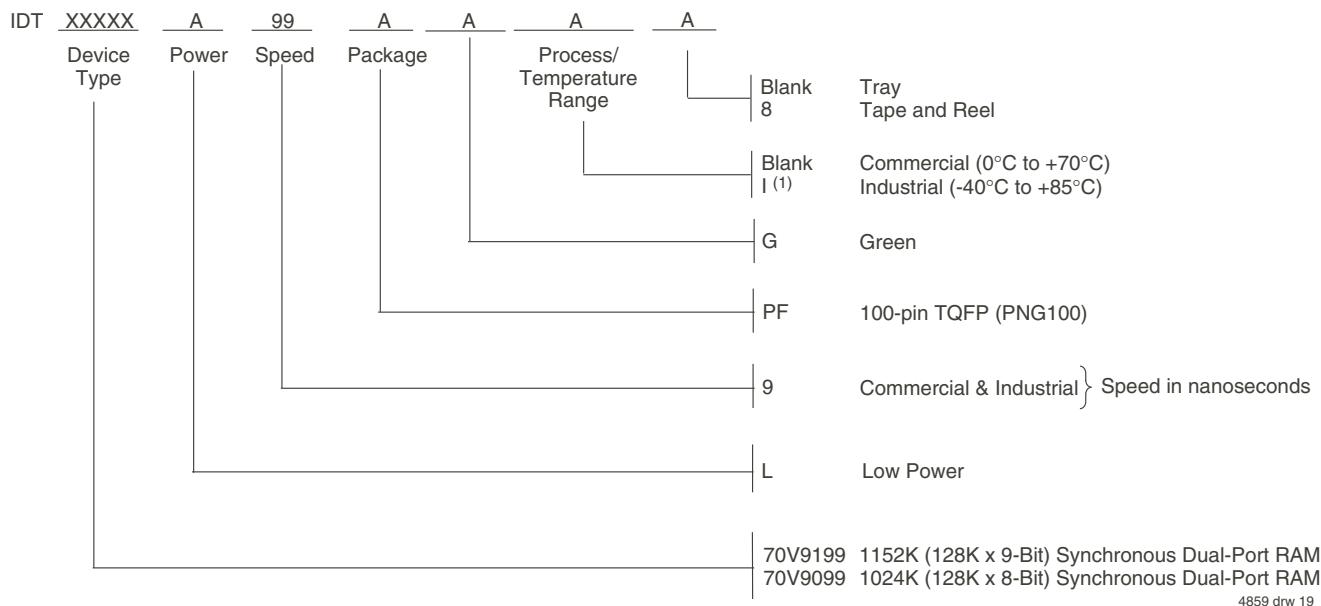


Figure 4. Depth and Width Expansion with IDT70V9199/099

## Ordering Information



## NOTES:

- Industrial temperature range is available. For specific speeds, packages and powers contact your sales office.

**LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02**  
Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

## IDT Clock Solution for IDT70V9199/099 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Dual-Port Clock Specifications			IDT PLL Clock Devices	IDT Non-PLL Clock Devices	
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency			
70V9199/099	3.3	LVTTL	9pF	40%	100	150ps	IDT2305 IDT2308 IDT2309	FCT3805 FCT3805D/E FCT3807 FCT3807D/E

4859tbl12

## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
9	70V9199L9PFGI	PNG100	TQFP	I
	70V9199L9PFGI8	PNG100	TQFP	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
9	70V9099L9PFG	PNG100	TQFP	C
	70V9099L9PFG8	PNG100	TQFP	C

## Datasheet Document History

09/30/99:		Initial Public Release
11/12/99:		Replaced IDT logo
01/10/01:	Page 3	Changed information in Truth Table II
	Page 4	Increased storage temperature parameters
	Page 5	Clarified TA parameter DC Electrical parameters—changed wording from "open" to "disabled" Changed $\pm 200\text{mV}$ to $0\text{mV}$ in notes Removed Preliminary status
04/09/03:		Consolidate multiple devices into one datasheet Changed naming conventions from V <sub>CC</sub> to V <sub>DD</sub> and from GND to V <sub>SS</sub>
	Pages 2 & 3	Added date revision to pin configurations
	Page 5	Added junction temperature to Absolute Maximum Ratings Table Added Ambient Temperature footnote
	Pages 1, 6 & 16	Added 6ns speed grade Added updated DC power numbers to the DC Electrical Characteristics Table Added 6ns speed AC timing numbers and changed t <sub>OE</sub> to be equal to t <sub>CD2</sub> in the AC Electrical Characteristics Table
	Page 16	Added IDT Clock Solution Table
01/10/06:	Page 1	Added green availability to features
	Page 16	Added green indicator to ordering information
02/22/07:	Page 1	Removed 6ns & 7ns speed grades from features
	Page 6	Removed 6ns & 7ns speed grade values from the DC Electrical Characteristics Table
	Page 8	Removed 6ns & 7ns speed grade values from the AC Electrical Characteristics Table
	Page 16	Removed 6ns & 7ns speed grades from ordering information
01/19/09:	Page 16	Removed "IDT" from orderable part number
07/26/10:	Page 8	In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial TA header note has been removed
	Pages 9-12	In order to correct the footnotes of timing diagrams, <u>CNTEN</u> has been removed to reconcile the footnotes with the <u>CNTEN</u> logic definition found in Truth Table II - Address Counter Control
03/01/18:		Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018
07/25/19:	Page 1 & 16	Deleted obsolete Commercial speed grade 12ns in Features and Ordering Information
	Page 2 & 3	Rotated PNG100 TQFP pin configurations to accurately reflect pin 1 orientation
	Page 2 & 3	Updated package code PN100-1 to PNG100
	Page 16	Added Orderable Part Information

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