

HIGH-SPEED 3.3V 16/8K X 9 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

IDT70V9169/59L

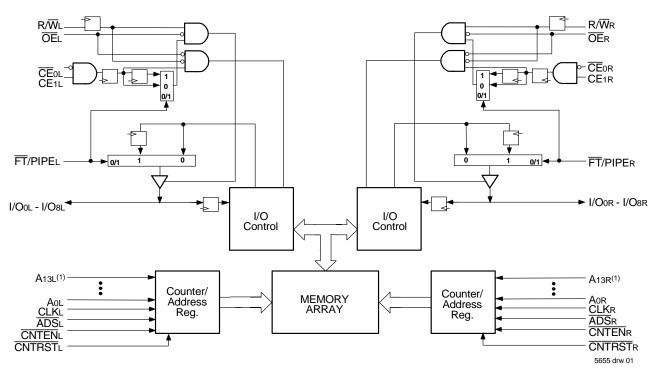
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
 - Commercial: 6.5/7.5/9ns (max.)
 - Industrial: 7.5ns (max.)
- Low-power operation
 - IDT70V916/59L/59L
 Active: 450mW (typ.)
 Standby: 1.5mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either port via the FT/PIPE pins
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic

- Full synchronous operation on both ports
 - 3.5ns setup to clock and Ons hold on all control, data, and address inputs
 - Data input, address, and control registers
 - Fast 6.5ns clock to data out in the Pipelined output mode
 - Self-timed write allows fast cycle time
 - 10ns cycle time, 100MHz operation in Pipelined output mode
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL- compatible, single 3.3V (±0.3V) power supply
- Industrial temperature range (-40°C to +85°C) is available for 83 MHz
- Available in a 100-pin Thin Quad Flatpack (TQFP) and 100pin fine pitch Ball Grid Array (fpBGA) packages.

Functional Block Diagram



NOTE:

1. A₁₃ is a NC for IDT70V9159.

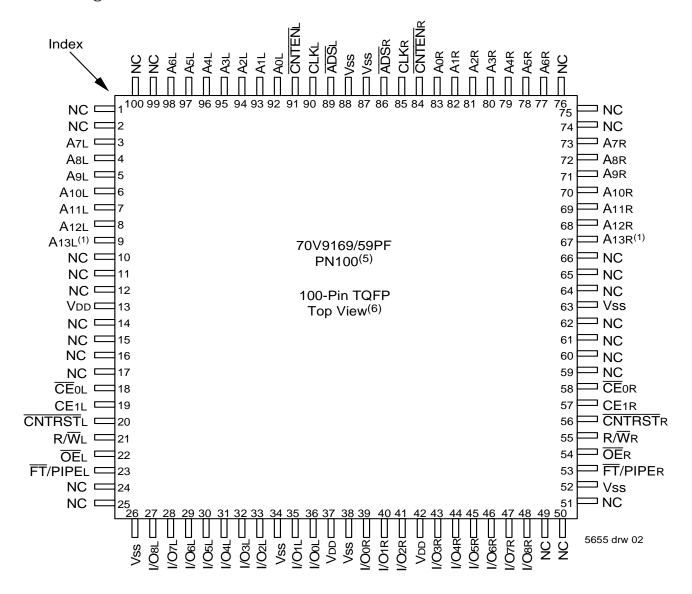
FEBRUARY 2018

Description:

The IDT70V9169/59 is a high-speed 16/8K x 9 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9169/59 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{\text{CE}}$ 0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 450mW of power.

Pin Configurations (1,2,3,4)



- 1. A₁₃ is a NC for IDT70V9159.
- 2. All VDD pins must be connected to power supply.
- 3. All Vss pins must be connected to ground supply.
- 4. Package body is approximately 14mm x 14mm x 1.4mm.
- 5. This package code is used to reference the package diagram.
- 6. This text does not indicate orientation of the actual part-marking.

Pin Configurations (cont'd) (1,2,3,4)

70V9169/59PF BF100⁽⁵⁾

100-Pin fpBGA Top View⁽⁶⁾

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
A6R	A 9R	A12R	NC	Vss	Vss	NC	R/WR	Vss	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
A4R	A5R	A8R	A 10R	NC	NC	NC	OEr	NC	I/O6R
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
A3R	NC	NC	A 7R	NC	CEOR	CE1R	PL/FTR	I/ O 7R	I/O3R
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
Aor	CLKR	A1R	A 2R	A 11R	A13R ⁽¹⁾	CNTRST _R	I/O8R	I/O5R	I/O1R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
Vss	ADSR	CNTENR	A1L	ADSL	Vss	I/O4R	I/O2R	I/Oor	VDD
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
Vss	CLKL	Aol	A3L	Vdd	Vss	Vdd	I/O2L	I/O1L	I/OoL
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
CNTENL	NC	A5L	A12L	NC	R/WL	NC	I/O4L	Vss	I/O3L
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
A2L	A4L	A9L	A13L ⁽¹⁾	NC	CE1L	NC	I/O7L	I/O6L	I/O5L
J1	J2	J3	J4	J5	J6	J7	^{J8}	^{J9}	J10
NC	A7L	A10L	NC	NC	NC	OEL	Vss	Vss	I/O8L
K1	K2	K3	K4	K5	K6	K7	K8		K10
A6L	A8L	A11L	NC	Vdd	Vdd	CE0L	CNTRST∟		NC

5655 drw 03

- 1. A₁₃ is a NC for IDT70V9159.
- 2. All V_{DD} pins must be connected to power supply.
- 3. All Vss pins must be connected to ground supply.
- 4. Package body is approximately 10mm x 10mm x 1.4mm with 0.8mm ball pitch.
- 5. This package code is used to reference the package diagram.
- 6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names		
Œ0L, CE1L	CEOR, CE1R	Chip Enables		
R/WL	R/W̄R	Read/Write Enable		
ŌĒL	OE R	Output Enable		
A0L - A13L ⁽¹⁾	Aor - A13R ⁽¹⁾	Address		
1/Ool - 1/O8L	1/Oor - 1/O8R	Data Input/Output		
CLKL	CLKR	Clock		
ADS L	AD S _R	Address Strobe		
CNTENL	<u>CNTEN</u> R	Counter Enable		
CNTRSTL	<u>CNTRST</u> R	Counter Reset		
FT/PIPEL	FT/PIPER	Flow-Through/Pipeline		
V	DD	Power (3.3V)		
V	SS	Ground (0V)		

NOTE:

1. A₁₃ is a NC for IDT70V9159.

Truth Table I—Read/Write and Enable Control^(1,2,3)

5655 tbl 01

ŌĒ	CLK	Œ₀	CE1	R/W	I/O ₀₋₈	Mode
Х	1	Н	Х	Χ	High-Z	Deselected—Power Down
Х	1	Χ	L	Χ	High-Z	Deselected—Power Down
Х	1	L	Н	L	DATAIN	Write
L	1	L	Н	Н	DATAout	Read
Н	Χ	L	Н	Χ	High-Z	Outputs Disabled

5655 tbl 02

- 1. "H" = VIH, "L" = VIL, "X" = Don't Care. 2. ADS, CNTEN, CNTRST = X.
- 3. $\overline{\text{OE}}$ is an asynchronous input signal.

Truth Table II—Address Counter Control (1,2)

External Address	Previous Internal Address	Internal Address Used	CLK	ĀDS	CNTEN	CNTRST	I/O ⁽³⁾	MODE
An	Х	An	↑	L ⁽⁴⁾	Х	Н	Dvo (n)	External Address Used
Х	An	An + 1	1	Н	L ⁽⁵⁾	Н	Dvo(n+1)	Counter Enabled—Internal Address generation
Х	An + 1	An + 1	1	Н	Н	Н	Dvo(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
Х	Х	A0	1	Χ	Х	L ⁽⁴⁾	Dvo(0)	Counter Reset to Address 0

NOTES:

5655 tbl 03

- 1. "H" = VIH, "L" = VIL, "X" = Don't Care. 2. $\overline{\text{CE}}_0$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, and $\overline{\text{OE}}$ = VIL; CE1 and R/ $\overline{\text{W}}$ = VIH.
- 3. Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- 4. ADS and CNTRST are independent of all other signals including CEo, CE1, UB and LB.
- 5. The address counter advances if CNTEN = VIL on the rising edge of CLK, regardless of all other signals including CE₀, CE₁, UB and LB.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature ⁽¹⁾	GND	V DD
Commercial	0°C to +70°C	0V	3.3V <u>+</u> 0.3V
Industrial	-40°C to +85°C	0V	3.3V <u>+</u> 0.3V

NOTES:

5655 tbl 04

1. This is the parameter Ta. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.3	3.6	V
Vss	Ground	0	0	0	V
VIH	Input High Voltage	2.0	_	V _{DD} +0.3V ⁽²⁾	V
VIL	Input Low Voltage	-0.3 ⁽¹⁾	_	0.8	V

5655 tbl 05

NOTES:

- 1. VIL > -1.5V for pulse width less than 10 ns.
- 2. VTERM must not exceed VDD+0.3V.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	-55 to +125	°C
Tstg	Storage Temperature	-65 to +150	°C
Іоит	DC Output Current	50	mA

NOTES:

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. VTERM must not exceed VDD +0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20 mA for the period of VTERM $\geq VDD + 0.3$ V.

Capacitance⁽¹⁾

 $(TA = +25^{\circ}C, f = 1.0MHz)$

	Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
	CIN	Input Capacitance	VIN = 3dV	9	pF
ĺ	Соит ⁽³⁾	Output Capacitance	Vout = 3dV	10	pF

NOTES:

5655 tbl 07

- 1. These parameters are determined by device characterization, but are not production tested.
- 2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- 3. Cout also references Ci/o.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (VDD= 3.3V ± 0.3V)

			70V91		
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Iu	Input Leakage Current ⁽¹⁾	$V_{DD} = 3.6V$, $V_{IN} = 0V$ to V_{DD}	-	5	μΑ
luo	Output Leakage Current	\overline{CE} = ViH or CE1 = ViL, Vout = 0V to VDD	_	5	μΑ
Vol	Output Low Voltage	IoL = +4mA	_	0.4	V
Vон	Output High Voltage	IOH = -4mA	2.4	_	V

NOTE:

5655 tbl 08

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range $^{(3)}$ (VDD = 3.3V ± 0.3V)

						70V9169/5 Com'l O					70V9169/59L9 Com'l Only		
Symbol	Parameter	Test Condition	Versio	n	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Мах.	Typ. ⁽⁴⁾	Max.	Unit		
ldd	Dynamic Operating	CEL and CER= VIL,	COM'L	Г	175	330	155	280	135	230	mA		
	Current (Both Ports Active)	Outputs Disabled, f = fMAX ⁽¹⁾	IND	L		_	155	330	_	_			
ISB1	Standby Current	$\overline{CE}L = \overline{CE}R = VIH$	COM'L	L	50	80	40	70	30	60	mA		
	(Both Ports - TTL Level Inputs)	$f = fMAX^{(1)}$	IND	L		_	40	80	_	_			
ISB2	Standby	CE*A" = VIL and CE*B" = VIH ⁽⁵⁾ Active Port Outputs Disabled, f=fMAX ⁽¹⁾	COM'L	L	115	185	105	170	95	155	mA		
	Current (One Port - TTL Level Inputs)		IND	L	_	_	105	180	_	_			
ISB3	Full Standby	Both Ports CEL and	COM'L	L	0.5	3.0	0.5	3.0	0.5	3.0	mA		
	Current (Both Ports - CMOS Level Inputs)	$\overline{CE}R \ge V_{DD} - 0.2V$, $V_{IN} \ge V_{DD} - 0.2V$ or $V_{IN} \le 0.2V$, $f = 0^{(2)}$	IND	L		_	0.5	3.0	_				
ISB4	Full Standby	\overline{CE} "A" $\leq 0.2V$ and	COM'L	L	105	175	95	160	85	145	mA		
	Current (One Port - CMOS Level Inputs)	$\begin{array}{ll} \overline{\text{CE}}\text{'B"} & \stackrel{>}{\geq} \text{V}_{DD} \text{ - } 0.2 \text{V}^{(5)} \\ \text{VIN} & \geq \text{ V}_{DD}\text{- } 0.2 \text{V or} \\ \text{VIN} & \leq 0.2 \text{V, Active Port,} \\ \text{Outputs Disabled, } f = \text{fmax}^{(1)} \end{array}$	IND	L			95	175		_			

5655 tbl 09

- 1. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tcvc, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- 2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- 3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 4. $V_{DD} = 3.3V$, $T_A = 25$ °C for Typ, and are not production tested. $I_{CCDC}(f=0) = 90$ mA (Typ).
- 5. $\overline{\text{CE}}\text{x} = \text{V}\text{IL} \text{ means } \overline{\text{CE}}\text{ox} = \text{V}\text{IL} \text{ and } \text{CE}\text{1x} = \text{V}\text{IH}$
 - $\overline{\text{CE}}\text{x} = \text{Vih means } \overline{\text{CE}}\text{ox} = \text{Vih or CE}\text{1x} = \text{Vil}$
 - $\overline{\text{CE}}\text{x} \leq 0.2 \text{V}$ means $\overline{\text{CE}}\text{ox} \leq 0.2 \text{V}$ and $\text{CE}\text{1x} \geq \text{V}\text{dd}$ 0.2 V
 - $\overline{\text{CE}}\text{x} \geq \text{ V}\text{DD} \text{ } 0.2 \text{V} \text{ means } \overline{\text{CE}}\text{ox} \geq \text{ V}\text{DD} \text{ } 0.2 \text{V} \text{ or } \text{CE}\text{1x} \leq 0.2 \text{V}$
 - "X" represents "L" for left port or "R" for right port.

^{1.} At $VDD \le 2.0V$ input leakages are undefined.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	2ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2 & 3

5655 tbl 10

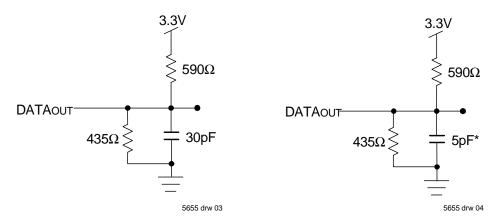


Figure 1. AC Output Test load.

Figure 2. Output Test Load (For tcklz, tckHz, tolz, and toHz). *Including scope and jig.

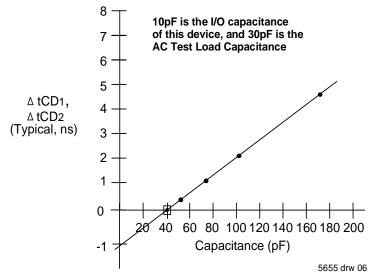


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) $^{(3)}$ ($V_{DD}=3.3V\pm0.3V$, $T_{A}=0^{\circ}C$ to +70°C)

	did write byele rilling) (VIII		69/59L6 I Only		69/59L7 & Ind			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tcyc1	Clock Cycle Time (Flow-Through) ⁽²⁾	19	_	22	_	25	_	ns
tcyc2	Clock Cycle Time (Pipelined) ⁽²⁾	10	_	12	_	15	_	ns
tcн1	Clock High Time (Flow-Through) ⁽²⁾	6.5		7.5	_	12	_	ns
ta_1	Clock Low Time (Flow-Through) ⁽²⁾	6.5	_	7.5	_	12	_	ns
tCH2	Clock High Time (Pipelined) ⁽²⁾	4	_	5	_	6	_	ns
ta_2	Clock Low Time (Pipelined) ⁽²⁾	4	_	5	_	6	_	ns
tr	Clock Rise Time	_	3	_	3	_	3	ns
tr	Clock Fall Time		3	_	3	_	3	ns
tsa	Address Setup Time	3.5		4		4	_	ns
tha	Address Hold Time	0		0	_	1	_	ns
tsc	Chip Enable Setup Time	3.5		4	_	4	_	ns
thc	Chip Enable Hold Time	0		0		1	_	ns
tsB	Byte Enable Setup Time	3.5		4	_	4	_	ns
tнв	Byte Enable Hold Time	0		0		1	_	ns
tsw	R/W Setup Time	3.5		4		4	_	ns
thw	R/W Hold Time	0		0	_	1	_	ns
tsd	Input Data Setup Time	3.5		4	_	4	_	ns
thD	Input Data Hold Time	0		0		1	_	ns
tsad	ADS Setup Time	3.5		4		4	_	ns
thad	ADS Hold Time	0	_	0	_	1	_	ns
tscn	CNTEN Setup Time	3.5		4		4	_	ns
thon	CNTEN Hold Time	0		0	_	1	_	ns
tsrst	CNTRST Setup Time	3.5		4		4	_	ns
thrst	CNTRST Hold Time	0		0	_	1	_	ns
toe	Output Enable to Data Valid	_	6.5	_	7.5	_	9	ns
tolz	Output Enable to Output Low-Z ⁽¹⁾	2		2	_	2	_	ns
tонz	Output Enable to Output High-Z ⁽¹⁾	1	7	1	7	1	7	ns
tcd1	Clock to Data Valid (Flow-Through) ⁽²⁾	_	15	_	18	_	20	ns
tCD2	Clock to Data Valid (Pipelined) ⁽²⁾		6.5	_	7.5		9	ns
toc	Data Output Hold After Clock High	2		2		2	_	ns
tckhz	Clock High to Output High-Z ⁽¹⁾	2	9	2	9	2	9	ns
tcklz	Clock High to Output Low-Z ⁽¹⁾	2	_	2	_	2	_	ns
Port-to-Port I	Delay	•	<u> </u>	-	-	-	-	-
tcwdd	Write Port Clock High to Read Data Delay	_	24	_	28	_	35	ns
tccs	Clock-to-Clock Setup Time		9	_	10	_	15	ns

NOTES:

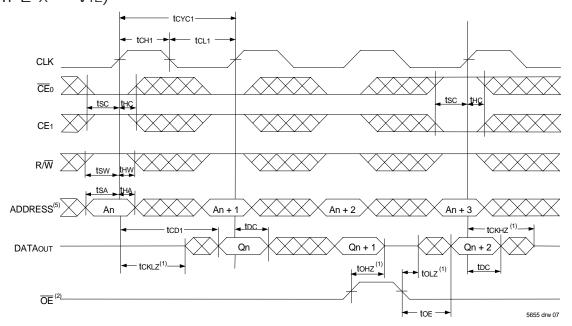
5655 tbl 11

^{1.} Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.

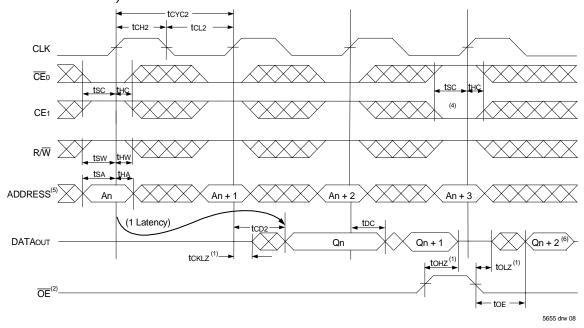
^{2.} The Pipelined output parameters (tcyc2, tcb2) apply to either or both the Left and Right ports when FT/PIPE = VIH. Flow-through parameters (tcyc1, tcb1) apply when FT/PIPE = VIL for that port.

^{3.} All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (OE), FT/PIPER, and FT/PIPEL.

Timing Waveform of Read Cycle for Flow-Through Output $(\overline{FT}/PIPE"x" = VIL)^{(3,6)}$

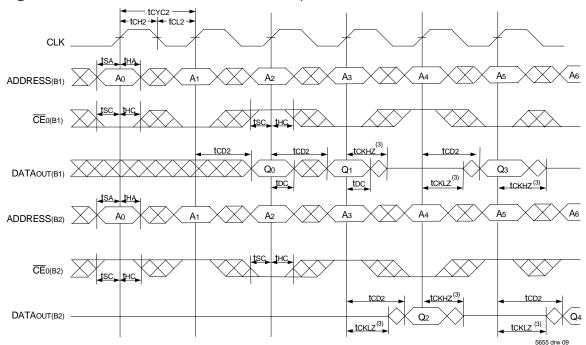


Timing Waveform of Read Cycle for Pipelined Operation $(\overline{FT}/PIPE"x" = VIH)^{(3,6)}$

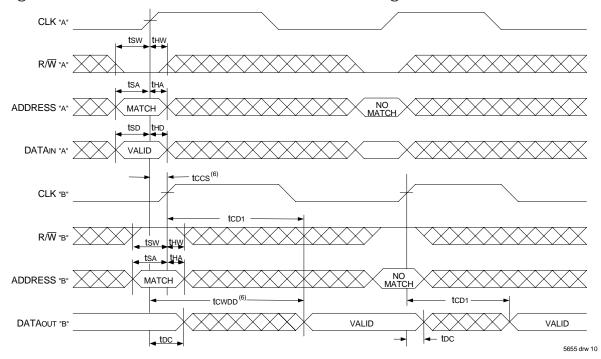


- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
- 3. $\overline{ADS} = VIL$, \overline{CNTEN} and $\overline{CNTRST} = VIH$.
- 4. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = \text{V}_{\text{IH}}$, CE1 = VIL following the next rising edge of the clock. Refer to Truth Table 1.
- 5. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- 6. "X' here denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Bank Select Pipelined Read (1,2)



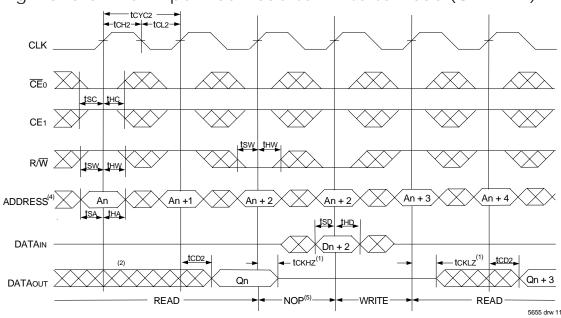
Timing Waveform with Port-to-Port Flow-Through Read^(4,5,7)



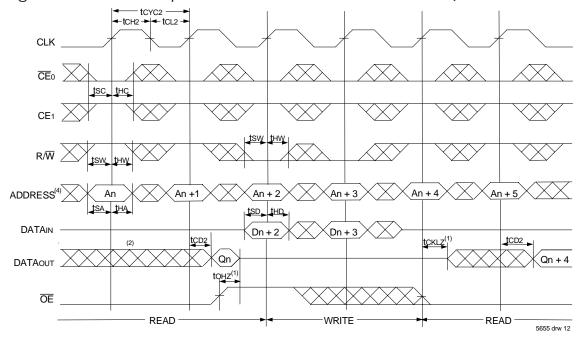
- 1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V916/59L for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
- 2. \overline{OE} and \overline{ADS} = VIL; CE1(B1), CE1(B2), R/W, \overline{CNTEN} , and \overline{CNTRST} = VIH.
- 3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 4. $\overline{\text{CE}}_0$ and $\overline{\text{ADS}} = \text{Vil.}$; CE1, $\overline{\text{CNTEN}}$, and $\overline{\text{CNTRST}} = \text{Vih.}$
- 5. \overline{OE} = VIL for the Right Port, which is being read from. \overline{OE} = VIH for the Left Port, which is being written to.
- 6. If tccs ≤ maximum specified, then data from right port READ is not valid until the maximum specified for tcwpb.

 If tccs > maximum specified, then data from right port READ is not valid until tccs + tcp1. tcwpb does not apply in this case.
- 7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read (**OE** = VIL)(3)

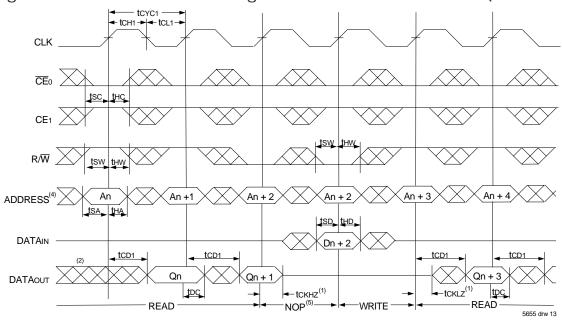


Timing Waveform of Pipelined Read-to-Write-to-Read (**OE** Controlled)(3)

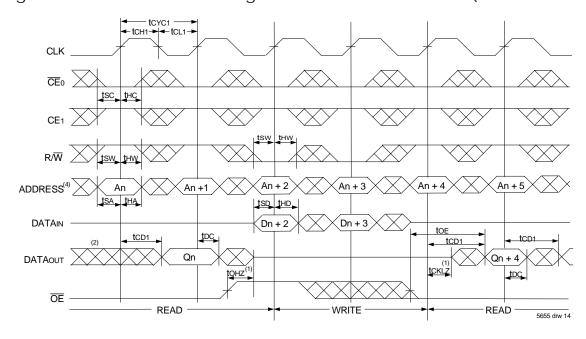


- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- 3. $\overline{\text{CE}}_0$ and $\overline{\text{ADS}}$ = VIL; CE1, $\overline{\text{CNTEN}}$, and $\overline{\text{CNTRST}}$ = VIH. "NOP" is "No Operation".
- 4. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- 5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read (**OE** = VIL)(3)

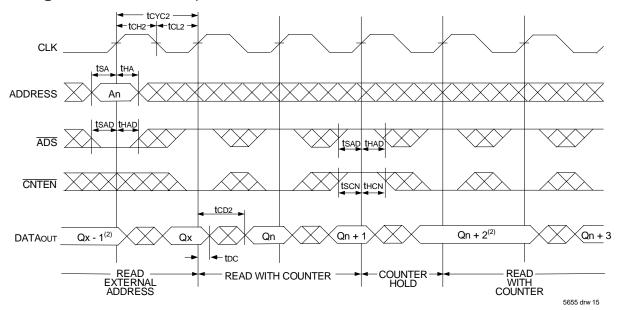


Timing Waveform of Flow-Through Read-to-Write-to-Read (**OE** Controlled)(3)

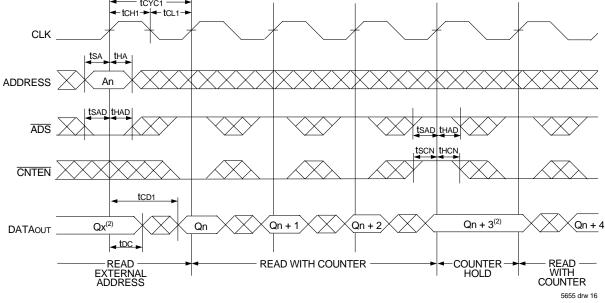


- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- CEo and ADS = VIL; CE1, CNTEN, and CNTRST = VIH. "NOP" is "No Operation".
 Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- 5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾

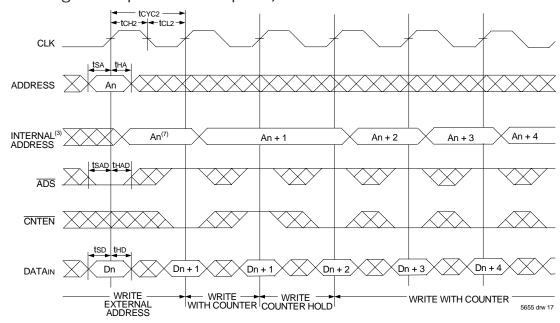


Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

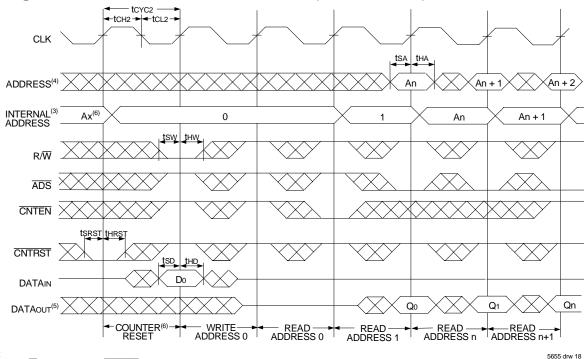


- 1. $\overline{\text{CE}}_0$ and $\overline{\text{OE}}$ = V_{IL}; CE₁, R/ $\overline{\text{W}}$, and $\overline{\text{CNTRST}}$ = V_{IH}.
- 2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)



Timing Waveform of Counter Reset (Pipelined Outputs)(2)



- NOTES: 1. $\overline{\text{CE}}_0$ and $\overline{\text{R/W}} = \text{VIL}$; CE1 and $\overline{\text{CNTRST}} = \text{VIH}$.
- 2. $\overline{CE}_0 = V_{IL}$; CE1 = V_{IH}.
- 3. The "Internal Address" is equal to the "External Address" when ADS = V_{IL} and equals the counter output when ADS = V_{IL}
- 4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- 5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- 6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. ADDRo will be accessed. Extra cycles are shown here simply for clarification.
- 7. CNTEN = VIL advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V9169/59 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

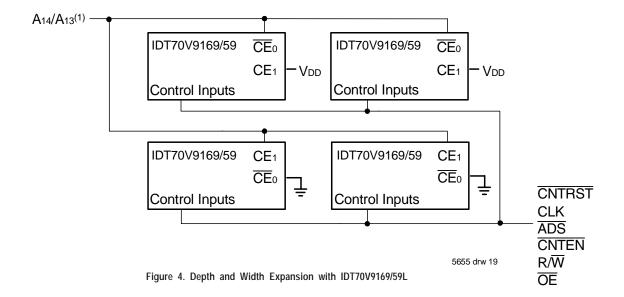
An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

 $\overline{\text{CE}}\text{O} = \text{VIL}$ and CE1 = VIH for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9169/59's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{\text{CE}}\text{O} = \text{VIL}$ and CE1 = VIH to re-activate the outputs.

Depth and Width Expansion

The IDT70V9169/59 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

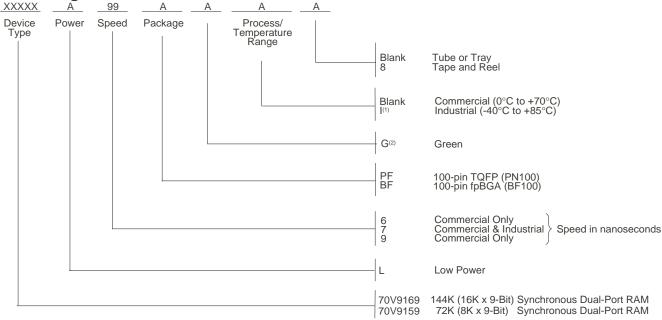
The IDT70V9169/59 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.



NOTE:

1. A14 is for IDT70V9169, A₁₃ is for IDT70V9159.





NOTES:

- 1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers see your sales office.
 LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice PDN# SP-17-02

IDT Clock Solution for IDT70V9169/59 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specitications		Clock Specifications				IDT	IDT
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance	PLL Clock Device	Non-PLL Clock Device
70V9169/59	3.3	LVTTL	9pF	40%	100	150ps	IDT2305 IDT2308 IDT2309	FCT3805 FCT3805D/E FCT3807 FCT3807D/E

5638 tbl 12

Datasheet Document History

07/08/02: Initial Public Release 08/15/03: Removed Preliminary status

Page 16 Added IDT Clock Solution Table

01/29/09: Page 16 Removed "IDT" from orderable part number 06/18/15: Page 2 Removed IDT with reference to fabrication

Page 2 Removed date from 100-pin TQFP configuration

Page 2 & 16 The package code PN100-1 changed to PN100 to match standard package codes

Page 3 Removed date from 100-pin fpBGA configuration Page 6 Corrected typo in the Typical Output Derating drawing

Page 16 Added Tape and Reel and Green indicators and updated the footnotes to the Ordering Information

02/21/18: Product Discontinuation Notice - PDN# SP-17-02

Last time buy expires June 15, 2018

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