

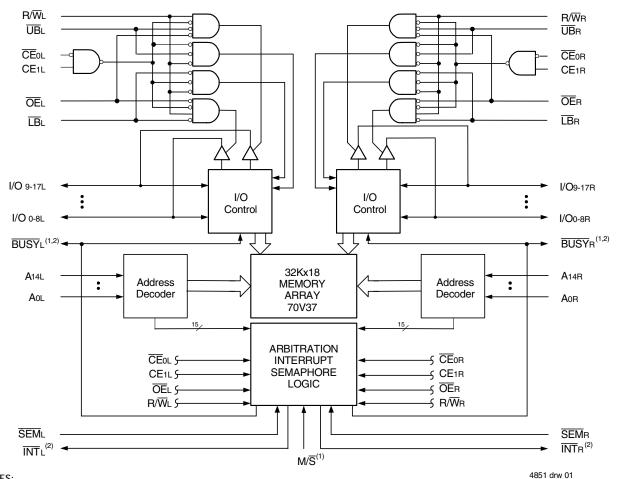
HIGH-SPEED 3.3V 32K x 18 DUAL-PORT STATIC RAM

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
 - Commercial: 15ns (max.)
 - Industrial: 20ns (max.)
- Low-power operation
 - IDT70V37L Active: 440mW (typ.) Standby: 660µW (typ.)
- Dual chip enables allow for depth expansion without external logic
- IDT70V37 easily expands data bus width to 36 bits or more using the Master/Slave select when cascading more than one device

- M/S = VIH for BUSY output flag on Master, M/S = VIL for BUSY input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTL-compatible, single 3.3V (±0.3V) power supply
- Available in a 100-pin TQFP
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

Functional Block Diagram



NOTES:

- 1. \overline{BUSY} is an input as a Slave (M/ \overline{S} =VIL) and an output when it is a Master (M/ \overline{S} =VIH).
- 2. BUSY and INT are non-tri-state totem-pole outputs (push-pull).

JUNE 2019



Description

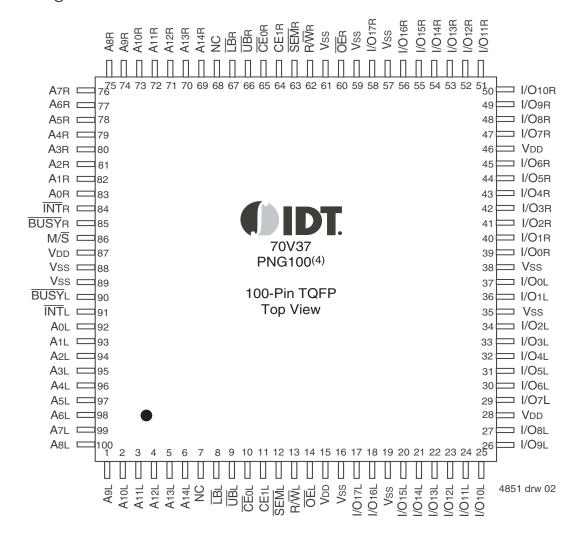
The IDT70V37 is a high-speed 32K x 18 Dual-Port Static RAM. The IDT70V37 is designed to be used as a stand-alone 576K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 36-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 36-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for

reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{\text{CE}}$ 0 or CE1) permit the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 440mW of power. The IDT70V37 is packaged in a 100-pin Thin Quad Flatpack (TQFP).

Pin Configurations (1,2,3)



NOTES:

- 1. All VDD pins must be connected to power supply.
- 2. All Vss pins must be connected to ground.
- 3. Package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names		
CEOL, CE1L	CEOR, CE1R	Chip Enables		
R/WL	R/W̄R	Read/Write Enable		
ŌĒL	OE R	Output Enable		
Aol - A14L	A0R - A14R	Address		
I/O0L - I/O17L	I/O0R - I/O17R	Data Input/Output		
SEML	<u>SEM</u> R	Semaphore Enable		
<u>ŪB</u> ∟	UB R	Upper Byte Select		
<u>TB</u> ∟	∐ B _R	Lower Byte Select		
ĪNTL	ĪNT _R	Interrupt Flag		
BUSYL	BUSY R	Busy Flag		
M/S		Master or Slave Select		
V	DD	Power (3.3V)		
V	SS	Ground (0V)		

4851 tbl 01

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	-55 to +125	°C
Tstg	Storage Temperature	-65 to +150	°C
Іоит	DC Output Current	50	mA

NOTES: 4851 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS
 may cause permanent damage to the device. This is a stress rating only and
 functional operation of the device at these or any other conditions above those
 indicated in the operational sections of this specification is not implied. Exposure
 to absolute maximum rating conditions for extended periods may affect
 reliability.
- 2. VTERM must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20 mA for the period of VTERM $\geq V$ DD + 0.3V.

Maximum Operating Temperature and Supply Voltage (1)

апасары	yvortago				
Grade	Ambient Temperature ⁽¹⁾	GND	Vdd		
Commercial	0°C to +70°C	0V	3.3V <u>+</u> 0.3V		
Industrial	-40°C to +85°C	0V	3.3V <u>+</u> 0.3V		

NOTE:

1. This is the parameter Ta. This is the "instant on" case temperature.

Recommended DC Operating Conditions

COLIG	110113				
Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.3	3.6	٧
Vss	Ground	0	0	0	V
VIH	Input High Voltage	2.0		V _{DD} +0.3 ⁽²⁾	V
VIL	Input Low Voltage	-0.3 ⁽¹⁾	_	0.8	V

4851 tbl 04

NOTES:

1. $V_{IL} \ge -1.5V$ for pulse width less than 10ns.

2. VTERM must not exceed VDD + 0.3V.

Capacitance⁽¹⁾ (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	9	pF
Cout ⁽²⁾	Output Capacitance	Vout = 0V	10	pF

NOTES

1. This parameter is determined by device characterization but is not production tested.

2. Cout also references C_Vo.



Industrial and Commercial Temperature Ranges

Truth Table I – Chip Enable^(1,2)

CE	Œ0	CE1	Mode		
	V⊩	VIH	Port Selected (TTL Active)		
L	L $\leq 0.2V$ $\geq VDD - 0.2V$ Port Selected (CMOS Active)				
	VIH	X	Port Deselected (TTL Inactive)		
Н	X	VıL	Port Deselected (TTL Inactive)		
	≥VDD -0.2V	X ₍₃₎	Port Deselected (CMOS Inactive)		
	X ₍₃₎	<u><</u> 0.2V	Port Deselected (CMOS Inactive)		

NOTES: 4852 tbl 06

- 1. Chip Enable references are shown above with the actual $\overline{\text{CE}}_0$ and CE_1 levels; $\overline{\text{CE}}$ is a reference only.
- 2. 'H' = VIH and 'L' = VIL.
- 3. CMOS standby requires 'X' to be either \leq 0.2V or \geq VDD-0.2V.

Truth Table II - Non-Contention Read/Write Control

	Inputs ⁽¹⁾					Outputs		
CE(2)	R/W	ŌĒ	ŪB	<u>ГВ</u>	SEM	I/O ₉₋₁₇	I/O ₀₋₈	Mode
Н	Х	Χ	Х	Х	Н	High-Z	High-Z	Deselected: Power-Down
X	Х	Х	Н	Н	Н	High-Z	High-Z	Both Bytes Deselected
L	L	Χ	L	Н	Н	DATAIN	High-Z	Write to Upper Byte Only
L	L	Х	Н	L	Н	High-Z	DATAIN	Write to Lower Byte Only
L	L	Χ	L	L	Н	DATAIN	DATAIN	Write to Both Bytes
L	Н	L	L	Н	Н	DATAout	High-Z	Read Upper Byte Only
L	Н	L	Н	L	Н	High-Z	DATA out	Read Lower Byte Only
L	Н	L	L	L	Н	DATAout	DATAout	Read Both Bytes
Х	Х	Н	Χ	Χ	Χ	High-Z	High-Z	Outputs Disabled

NOTES: 4851 tbl 07

- 1. A0L A14L \neq A0R A14R
- 2. Refer to Truth Table I Chip Enable.

Truth Table III - Semaphore Read/Write Control(1)

	Inputs ⁽¹⁾						puts	
CE ⁽²⁾	R/W	ŌĒ	ŪB	ШB	SEM	I/O ₉₋₁₇	I/O ₀₋₈	Mode
Н	Н	L	Х	Х	L	DATAout	DATAout	Read Data in Semaphore Flag
Х	Н	L	Н	Н	L	DATAout	DATAout	Read Data in Semaphore Flag
Н	1	Χ	Х	Х	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
Х	1	Х	Н	Н	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
L	Х	Х	L	Х	L			Not Allowed
L	Х	Х	Х	L	L			Not Allowed

NOTES: 4851 tbl 08

- 1. There are eight semaphore flags written to I/Oo and read from all the I/Os (I/Oo-I/O17). These eight semaphore flags are addressed by Ao-A2.
- 2. Refer to Truth Table I Chip Enable.



Industrial and Commercial Temperature Ranges

DC Electrical Characteristics Over the Operating

Temperature and Supply Voltage Range (VDD = 3.3V ± 0.3V)

			70V37L		
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Iu	Input Leakage Current ⁽¹⁾	$V_{DD} = 3.6V$, $V_{IN} = 0V$ to V_{DD}	ı	5	μΑ
ILO	Output Leakage Current	$\overline{CE}^{(2)} = V_{IH}$, $V_{OUT} = 0V$ to V_{DD}	ı	5	μΑ
Vol	Output Low Voltage	IoL = +4mA	-	0.4	V
Vон	Output High Voltage	IOH = -4mA	2.4	_	٧

NOTES:

4851 tbl 09

- 1. At $V_{DD} \leq 2.0V$, input leakages are undefined.
- 2. Refer to Truth Table I Chip Enable.

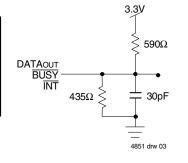
DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(5)}$ (VDD = 3.3V \pm 0.3V)

					7L15 Only	Co	7L20 m'l nd	
Symbol	Parameter	Test Condition	Version	Typ. ⁽¹⁾	Max.	Typ. ⁽¹⁾	Max.	Unit
lod	Dynamic Operating Current	<u>CE</u> = V _I L, Outputs Disabled <u>SEM</u> = V _I H	COM'L L	145	235	135	205	mA
	(Both Ports Active)	$f = f_{MAX}^{(2)}$	IND L	_		135	220	
ISB1	Standby Current (Both Ports - TTL Level	CEL = CER = VIH SEMR = SEML = VIH	COM'L L	40	70	35	55	mA
	Inputs)	$f = f_{MAX}^{(2)}$	IND L	_	_	35	65	
ISB2	Standby Current (One Port - TTL Level	CE"A" = VIL and CE"B" = VIH(4)	COM'L L	100	155	90	140	mA
	Inputs)	Active Port Outputs Disabled, f=fmax ⁽²⁾ , SEMR = SEML = VIH	IND L	_	_	90	150	
ISB3	Full Standby Current (Both Ports - All CMOS	Both Ports $\overline{CE}L$ and $\overline{CE}R \ge VDD - 0.2V$, $VIN \ge VDD - 0.2V$ or $VIN \le 0.2V$, $f = 0^{(3)}$	COM'L L	0.2	3.0	0.2	3.0	mA
	Level Inputs)	$\frac{VIN \ge VDD - 0.2V}{SEMR} = \frac{VDD - 0.2V}{SEMR} = \frac{VDD - 0.2V}{SEMR}$	IND L	_	_	0.2	3.0	
ISB4	Full Standby Current (One Port - All CMOS	\overline{CE} "A" $\leq 0.2V$ and \overline{CE} "B" $\geq V$ DD - $0.2V^{(4)}$, SEMR = $\overline{SEML} \geq V$ DD - $0.2V$,	COM'L L	95	150	90	135	mA
	Level Inputs)	SEMIR = SEMIL \geq VDD - 0.2V, VIN \geq VDD - 0.2V or VIN \leq 0.2V, Active Port Outputs Disabled, f = fmax ⁽²⁾	IND L	_		90	145	

- 1. VDD = 3.3V, TA = +25°C, and are not production tested. IDD DC = 90mA (Typ.)
- 2. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- 3. f = 0 means no address or control lines change.
- 4. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 5. Refer to Truth Table I Chip Enable.



AC Test Conditions	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2



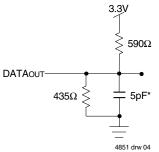
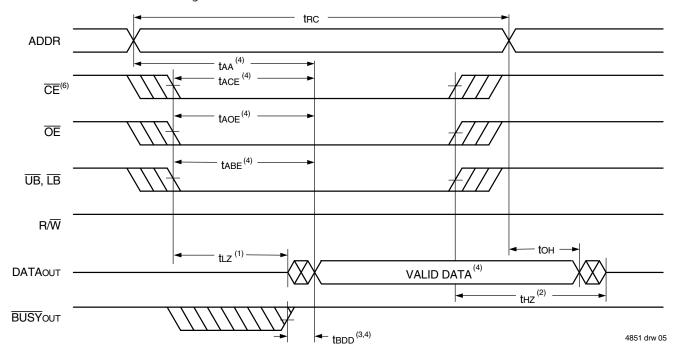


Figure 1. AC Output Load

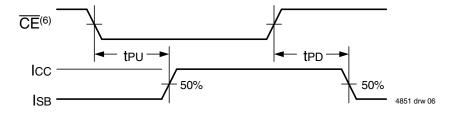
Figure 2. Output Test Load (for tLz, tHz, twz, tow) * Including scope and jig.

Waveform of Read Cycles⁽⁵⁾



4851 tbl 11

Timing of Power-Up Power-Down



NOTES:

- 1. Timing depends on which signal is asserted last, \overline{OE} , \overline{CE} , \overline{LB} or \overline{UB} .
- 2. Timing depends on which signal is de-asserted first $\overline{\sf CE}$, $\overline{\sf OE}$, $\overline{\sf LB}$ or $\overline{\sf UB}$.
- 3. tbbb delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
- 4. Start of valid data depends on which timing becomes effective last tage, tage, tage or tbdd.
- 5. SEM = VIH.
- 6. Refer toTruth Table I Chip Enable.



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

			37L15 I Only	70V37L20 Com'l & Ind			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
READ CYCLE							
trc	Read Cycle Time	15	_	20	_	ns	
taa	Address Access Time	_	15	_	20	ns	
tace	Chip Enable Access Time ⁽³⁾	_	15	_	20	ns	
tabe	Byte Enable Access Time ⁽³⁾	_	15	_	20	ns	
taoe	Output Enable Access Time	_	10	_	12	ns	
tон	Output Hold from Address Change	3	_	3	_	ns	
tLZ	Output Low-Z Time ^(1,2)	3	_	3	_	ns	
tHZ	Output High-Z Time ^(1,2)		10	_	10	ns	
tpu	Chip Enable to Power Up Time (2)	0	_	0	_	ns	
tpd	Chip Disable to Power Down Time (2)	_	15	_	20	ns	
tsop	Semaphore Flag Update Pulse (OE or SEM)	10		10	_	ns	
tsaa	Semaphore Address Access Time	_	15	_	20	ns	

4851 tbl 12

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

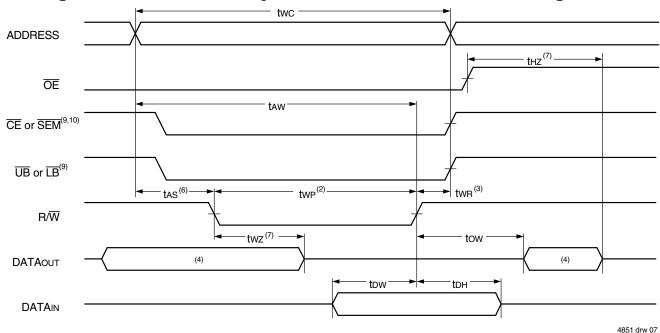
		70V37L15 Com'l Only		70V37L20 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE						
twc	Write Cycle Time	15	_	20		ns
tew	Chip Enable to End-of-Write ⁽³⁾	12	_	15	_	ns
taw	Address Valid to End-of-Write	12	_	15		ns
tas	Address Set-up Time ⁽⁵⁾	0	_	0		ns
twp	Write Pulse Width	12	_	15	_	ns
twr	Write Recovery Time	0	_	0		ns
tow	Data Valid to End-of-Write	10	_	15		ns
thz	Output High-Z Time ^(1,2)	_	10	_	10	ns
tон	Data Hold Time ⁽⁴⁾	0	_	0		ns
twz	Write Enable to Output in High-Z ^(1,2)	_	10	_	10	ns
tow	Output Active from End-of-Write ^(1,2,4)	0	_	0		ns
tswrd	SEM Flag Write to Read Time	5	_	5		ns
tsps	SEM Flag Contention Window	5	_	5		ns

NOTES:

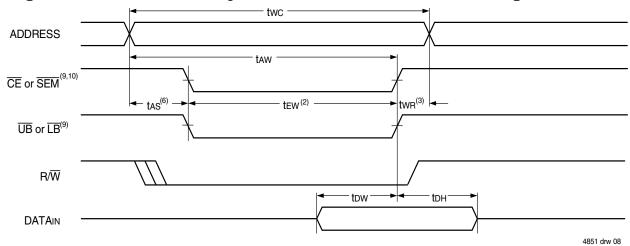
- 1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
- 2. This parameter is guaranteed by device characterization, but is not production tested.
- 3. To access RAM, $\overline{\text{CE}}$ = V_IL and $\overline{\text{SEM}}$ = V_IH. To access semaphore, $\overline{\text{CE}}$ = V_IH and $\overline{\text{SEM}}$ = V_IL. Either condition must be valid for the entire tew time.
- 4. The specification for toh must be met by the device supplying write data to the RAM under all operating conditions. Although toh and tow values will vary over voltage and temperature, the actual toh will always be smaller than the actual tow.



Timing Waveform of Write Cycle No. 1, R/W Controlled Timing (1,5,8)



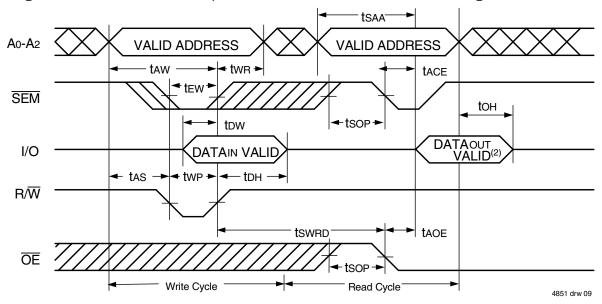
Timing Waveform of Write Cycle No. 2, **CE** Controlled Timing^(1,5)



- 1. R/\overline{W} or \overline{CE} or \overline{UB} and \overline{LB} = V_{IH} during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of a \overline{CE} = V_{IL} and a R/ \overline{W} = V_{IL} for memory array writing cycle. 3. twn is measured from the earlier of \overline{CE} or R/ \overline{W} (or \overline{SEM} or R/ \overline{W}) going HIGH to the end of write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the $\overline{\text{CE}}$ or $\overline{\text{SEM}} = \text{VIL}$ transition occurs simultaneously with or after the $\overline{\text{R/W}} = \text{VIL}$ transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal is asserted last, $\overline{\text{CE}}$ or $\overline{\text{RW}}$.
- 7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load
- 8. If $\overline{OE} = V_{IL}$ during R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If $\overline{OE} = VIH$ during an R/\overline{W} controlled write cycle, this requirement does not apply and the write pulse can be as short as the
- 9. To access RAM, $\overline{\text{CE}} = \text{VIL}$ and $\overline{\text{SEM}} = \text{VIH}$. To access semaphore, $\overline{\text{CE}} = \text{VIH}$ and $\overline{\text{SEM}} = \text{VIL}$. Lew must be met for either condition.
- 10. Refer to Truth Table I Chip Enable.



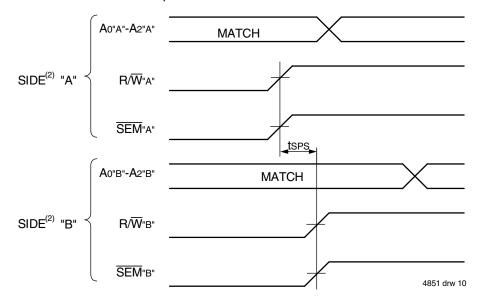
Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



NOTES:

- 1. $\overline{\text{CE}} = \text{V}_{\text{IH}}$ or $\overline{\text{UB}}$ and $\overline{\text{LB}} = \text{V}_{\text{IH}}$ for the duration of the above timing (both write and read cycle) (Refer to Truth Table I Chip Enable).
- 2. "DATAout VALID" represents all I/O's (I/Oo I/O17) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention (1,3,4)



NOTES

- 1. DOR = DOL = VIL, $\overline{CE}L = \overline{CE}R = VIH$ or both \overline{UB} and $\overline{LB} = VIH$ (Refer to Truth Table I Chip Enable).
- 2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
- 3. This parameter is measured from R/\overline{W}^*A^* or \overline{SEM}^*A^* going HIGH to R/\overline{W}^*B^* or \overline{SEM}^*B^* going HIGH.
- 4. If tsps is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

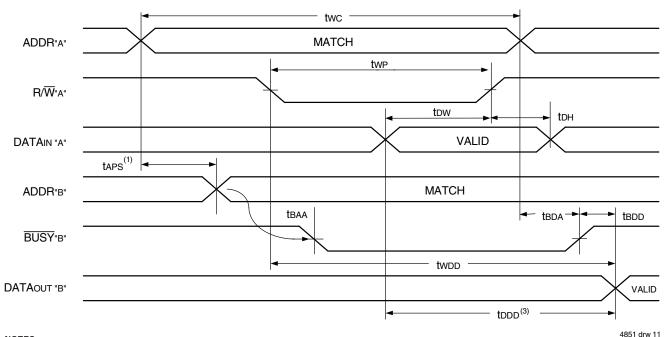
•	70V37L15 Com'l Only			70V37L20 Com'l & Ind			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	
BUSY TIMI	NG (M/S=Vih)						
tbaa	BUSY Access Time from Address Match	_	15		20	ns	
tBDA	BUSY Disable Time from Address Not Matched		15		20	ns	
t BAC	BUSY Access Time from Chip Enable Low		15		20	ns	
tBDC	BUSY Access Time from Chip Enable High	_	15	_	17	ns	
taps	Arbitration Priority Set-up Time (2)	5		5		ns	
tBDD	BUSY Disable to Valid Data ⁽³⁾		15	_	17	ns	
twн	Write Hold After BUSY ⁽⁵⁾	12		15		ns	
BUSY TIMI	NG (M/S=VIL)						
twB	BUSY Input to Write ⁽⁴⁾	0		0		ns	
twн	Write Hold After BUSY ⁽⁵⁾	12		15		ns	
PORT-TO-F	PORT DELAY TIMING						
twdd	Write Pulse to Data Delay ⁽¹⁾		30		45	ns	
todd	Write Data Valid to Read Data Delay ⁽¹⁾	_	25	_	30	ns	

NOTES:

- 1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY (M/S = VIH)".
- 2. To ensure that the earlier of the two ports wins.
- 3. tbdd is a calculated parameter and is the greater of 0, twdd twp (actual), or tddd tdw (actual).
- 4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
- 5. To ensure that a write cycle is completed on port "B" after contention on port "A".



Timing Waveform of Write with Port-to-Port Read and $\overline{\textbf{BUSY}}$ (M/ $\overline{\textbf{S}}$ = VIH) $^{(2,4,5)}$

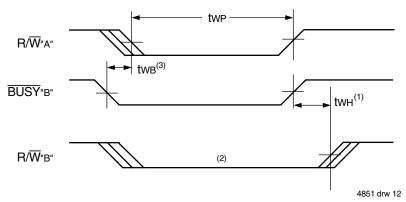


NOTES

4851 drv

- 1. To ensure that the earlier of the two ports wins. taps is ignored for $M/\overline{S} = VIL$ (SLAVE).
- 2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, refer to Truth Table I Chip Enable.
- 3. $\overline{OE} = V_{IL}$ for the reading port.
- 4. If $M/\overline{S} = V_{IL}$ (slave), \overline{BUSY} is an input. Then for this example $\overline{BUSY}^*A^* = V_{IH}$ and \overline{BUSY}^*B^* input is shown above.
- 5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

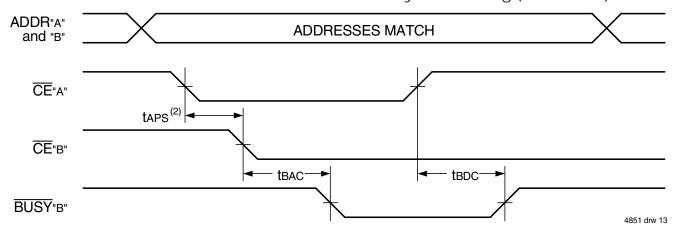
Timing Waveform of Write with **BUSY** (M/**S** = VIL)



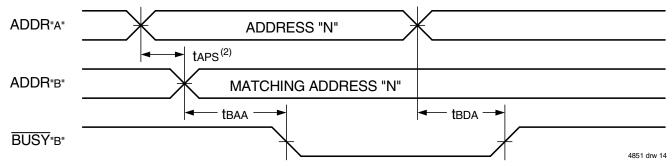
NOTES

- 1. twh must be met for both $\overline{\text{BUSY}}$ input (SLAVE) and output (MASTER).
- 2. $\overline{\text{BUSY}}$ is asserted on port "B" blocking R/ $\overline{\text{W}}$ "B", until $\overline{\text{BUSY}}$ "B" goes HIGH.
- 3. twb is only for the 'slave' version.

Waveform of **BUSY** Arbitration Controlled by **CE** Timing (M/**S** = VIH)^(1,3)



Waveform of $\overline{\textbf{BUSY}}$ Arbitration Cycle Controlled by Address Match Timing (M/ $\overline{\textbf{S}}$ = VIH)⁽¹⁾



NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
- 2. If taps is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.
- 3. Refer to Truth Table I Chip Enable .

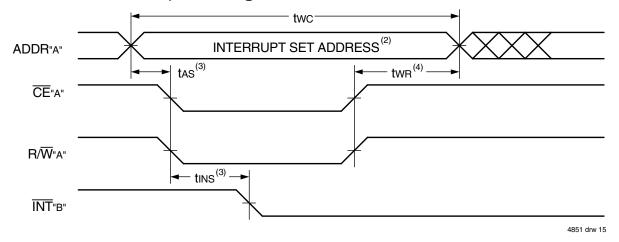
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

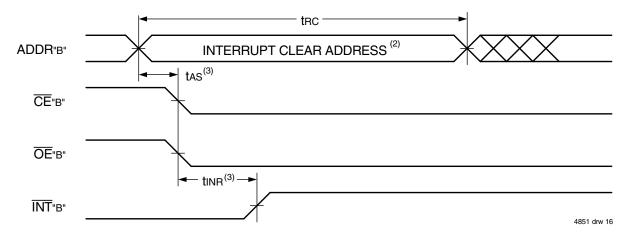
			37L15 'I Only	Co	37L20 m'l Ind	
Symbol	Parameter Min. Max.				Max.	Unit
INTERRUPT T	TIMING					
tas	Address Set-up Time	0		0	_	ns
twr	Write Recovery Time	0	_	0	_	ns
tins	Interrupt Set Time	_	15	_	20	ns
tinr	Interrupt Reset Time	_	15	_	20	ns



70V37L

Waveform of Interrupt Timing^(1,5)





NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
- 2. Refer to Interrupt Truth Table.
- 3. Timing depends on which enable signal ($\overline{\text{CE}}$ or R/\overline{W}) is asserted last.
- 4. Timing depends on which enable signal (CE or R/W) is de-asserted first.
- 5. Refer to Truth Table I Chip Enable.

Truth Table IV — Interrupt Flag^(1,4,5)

Left Port				Right Port						
R/₩L	CEL	<u>ŌE</u> L	A14L-A0L	ĪNT∟	R/ W R	CER	OE R	A14R-A0R	Ī NT R	Function
L	L	Х	7FFF	Х	Х	Х	Х	Х	L ⁽²⁾	Set Right INTR Flag
Х	Х	Х	X	Х	Х	L	L	7FFF	H ⁽³⁾	Reset Right INTR Flag
Х	Х	Х	Х	L ⁽³⁾	L	L	Х	7FFE	Х	Set Left INTL Flag
X	L	L	7FFE	H ⁽²⁾	Х	Х	Х	Х	Х	Reset Left INTL Flag

NOTES:

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.

- 2. If $\overline{BUSY}_L = V_{IL}$, then no change.
- 3. If $\overline{BUSY}R = VIL$, then no change.
- 4. $\overline{\text{INT}}_{\text{L}}$ and $\overline{\text{INT}}_{\text{R}}$ must be initialized at power-up.
- 5. Refer to Truth Table I Chip Enable.



Truth Table V —

Address **BUSY** Arbitration⁽⁴⁾

High-Speed 3.3V 32K x 18 Dual-Port Static RAM

Inputs			Out	puts	
CEL	ՇĒ r	Aol-A14L Aor-A14R	BUS YL(1)	BUS YR(1)	Function
Х	Х	NO MATCH	Н	Н	Normal
Н	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

NOTES:

4851 tbl 17

- 1. Pins BUSYL and BUSYR are both outputs when the part is configured as a master. Both are inputs when configured as a slave. BUSY outputs on the IDT70V37 are push-pull, not open drain outputs. On slaves the BUSY input internally inhibits writes.
- 2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If taps is not met, either BUSYL or BUSYR = LOW will result. BUSYL and BUSYR outputs can not be LOW simultaneously.
- 3. Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.
- 4. Refer to Truth Table I Chip Enable.

Truth Table VI — Example of Semaphore Procurement Sequence $^{(1,2,3)}$

			•
Functions	Do - D17 Left	Do - D17 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTES

4851 tbl 18

- 1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V37.
- 2. There are eight semaphore flags written to via I/Oo and read from all I/O's (I/Oo-I/O17). These eight semaphores are addressed by Ao A2.
- 3. $\overline{CE} = VIH$, $\overline{SEM} = VIL$ to access the semaphores. Refer to the Truth Table III Semaphore Read/Write Control.

Functional Description

The IDT70V37 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V37 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ 0 and CE1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ = HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag $(\overline{INT}L)$ is asserted when the right port writes to memory location 7FFE

(HEX), where a write is defined as $\overline{CE}R = R/\overline{W}R = VIL$ per the Truth Table. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}L = \overline{OE}L = VIL$, R/\overline{W} is a "don't care". Likewise, the right port interrupt flag (\overline{INTR}) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must read the memory location 7FFF. The message (18 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of \overline{BUSY} logic is not desirable, the \overline{BUSY} logic can be disabled by placing the part in slave mode with the \overline{MS} pin. Once in slave mode the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. If desired, unintended write operations can be prevented to a port by tying the \overline{BUSY} pin for that port LOW.

The BUSY outputs on the IDT 70V37 RAM in master mode, are pushpull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

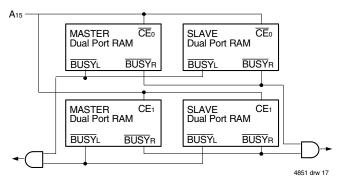


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V37 RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70V37 RAM array in width while using \overline{BUSY} logic, one master part is used to decide which side of the RAMs array will receive a \overline{BUSY} indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the \overline{BUSY} signal as a write inhibit signal. Thus on the IDT70V37 RAM the \overline{BUSY} pin is an output if the part is used as a master (M/ \overline{S} pin = VIL) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating \overline{BUSY} on one side of the array and another master indicating \overline{BUSY} on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long

enough for a $\overline{\text{BUSY}}$ flag to be output from the master before the actual write pulse can be initiated with the $R\overline{\text{W}}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V37 is an extremely fast Dual-Port 32K \times 18 CMOS Static RAMwith an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, with both ports being completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{\text{CE}}$, the Dual-Port RAM enable, and $\overline{\text{SEM}}$, the semaphore enable. The $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table III where $\overline{\text{CE}}$ and $\overline{\text{SEM}}$ are both HIGH.

Systems which can best use the IDT70V37 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V37s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V37 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the



shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V37 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the \overline{SEM} pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, \overline{CE} , and R/ \overline{W}) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins Ao – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table VI). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{\text{SEM}}$) and output enable ($\overline{\text{OE}}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{\text{SEM}}$ or $\overline{\text{OE}}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table VI). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram

of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

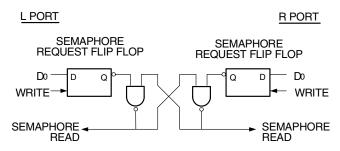


Figure 4. IDT70V37 Semaphore Logic

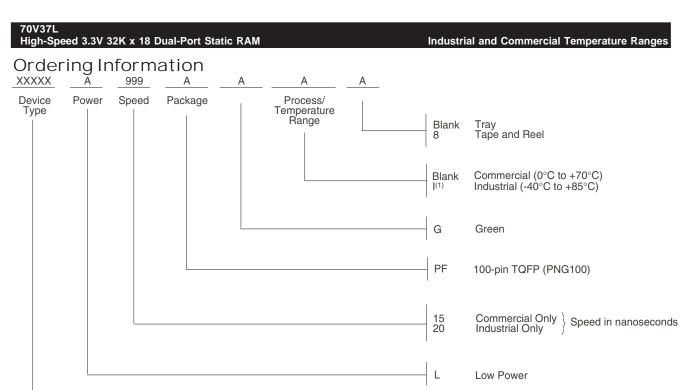
4851 drw 18

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.





576K (32K x 18) Dual-Port RAM

4851 drw 19

70V37

NOTES:

- 1. Contact your sales office for Industrial Temperature range in other speeds, packages and powers.
- LEAD FINISH (SnPb) are Obsolete Product Discontinuation Notice PDN#SP-17-02
 Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	70V37L15PFG	PNG100	TQFP	С
	70V37L15PFG8	PNG100	TQFP	С
20	70V37L20PFGI	PNG100	TQFP	I
	70V37L20PFGl8	PNG100	TQFP	Ι



Datasheet Document History

08/01/99: Initial Public Offering

Page 1 & 17 Replaced IDT logo 01/02/02:

Page 3 Increased storage temperature parameter

Clarified TA Parameter

Page 5 DC Electrical parameters-changed wording from "open" to "disabled"

Added Truth Table I - Chip Enable as note 5

Corrected ±200mV to 0mV in notes

Page 5, 7, 10 & 12 Added Industrial Temperature range for 20ns to DC & AC Electrical Characteristics

06/17/04: Removed Preliminary status

> Page 1 & 17 Replaced old ® logo with new тм logo Page 2 Added date revision to pin configuration

Page 2 - 5 Changed naming conventions from Vcc to Vpp and from GND to Vss

Page 1 Added green availability to features 08/15/08:

> Page 17 Added green indicator to ordering information Page 1 & 17 Updated old ™ logo with new ® logo

01/19/09: Page 17 Removed "IDT" from orderable part number 06/18/15: Page 2 Removed IDT in reference to fabrication

Page 2 Removed date from the 100-pin TQFP configuration

Page 2 & 17 The package code PN100-1 changed to PN100 to match standard package codes

Page 17 Added Tape & Reel indicator to the Ordering Information

Product Discontinuation Notice - PDN# SP-17-02 12/14/17:

Last time buy expires June 15, 2018

06/20/19: Page 1 & 17 Deleted obsolete Commercial 20ns speed grade in Features and Ordering Information

Page 2 Rotated PNG100 TQFP pin configuration to accurately reflect pin 1 orientation

Page 17 Added Orderable Part Information table

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.