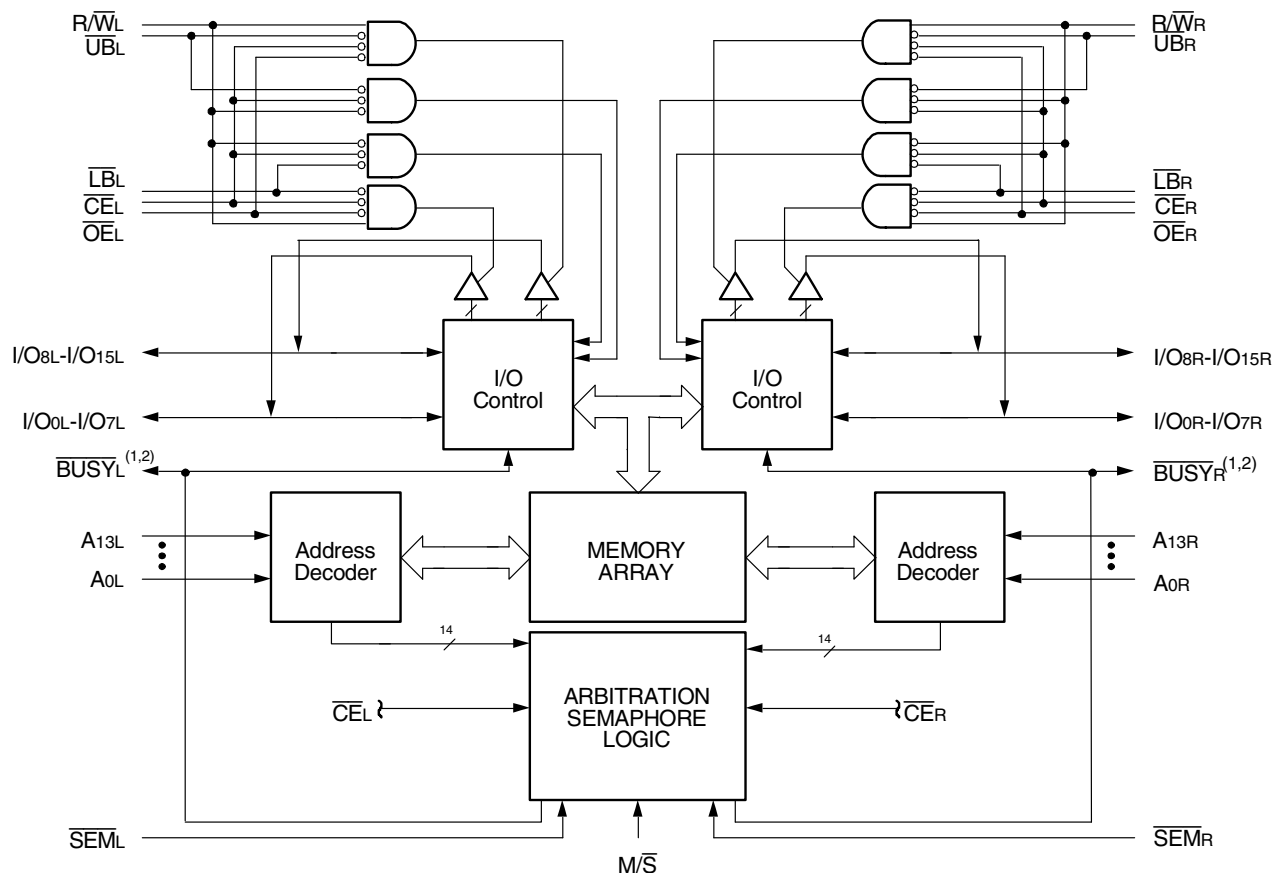


Features

- ♦ True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- ♦ High-speed access
 - Commercial: 25/35/55ns (max.)
- ♦ Low-power operation
 - IDT70V26S
Active: 300mW (typ.)
Standby: 3.3mW (typ.)
 - IDT70V26L
Active: 300mW (typ.)
Standby: 660μW (typ.)
- ♦ Separate upper-byte and lower-byte control for multiplexed bus compatibility
- ♦ IDT70V26 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- ♦ $M/\bar{S} = V_{IH}$ for \overline{BUSY} output flag on Master
 $M/\bar{S} = V_{IL}$ for \overline{BUSY} input on Slave
- ♦ On-chip port arbitration logic
- ♦ Full on-chip hardware support of semaphore signaling between ports
- ♦ Fully asynchronous operation from either port
- ♦ TTL-compatible, single 3.3V ($\pm 0.3V$) power supply
- ♦ Available in 84-pin PGA and PLCC
- ♦ Green parts available, see ordering information

Functional Block Diagram



NOTES:

1. (MASTER): \overline{BUSY} is output; (SLAVE): \overline{BUSY} is input.
2. \overline{BUSY} outputs are non-tri-stated push-pull.

2945 drw 01

Description

The IDT70V26 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT70V26 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

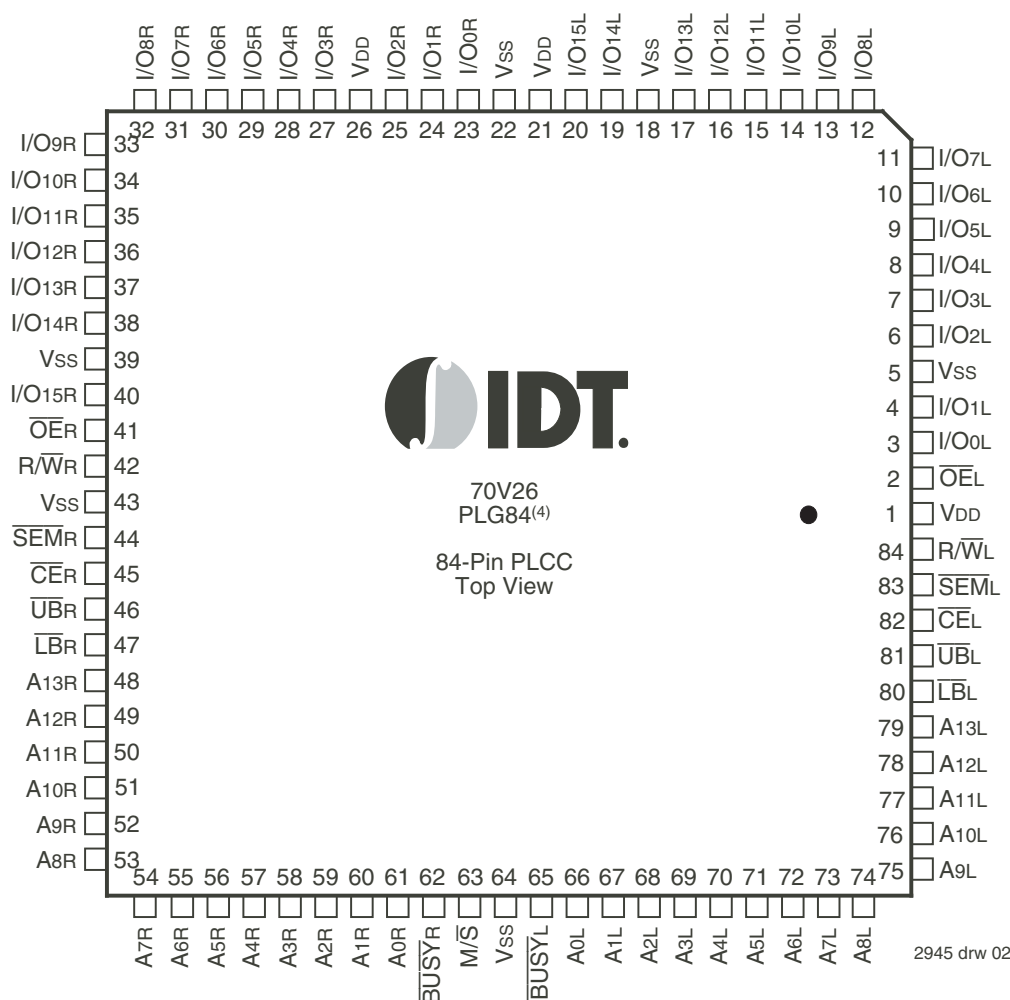
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for

reads or writes to any location in memory. An automatic power down feature controlled by \overline{CE} permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 300mW of power.

The IDT70V26 is packaged in a ceramic 84-pin PGA and 84-Pin PLCC.

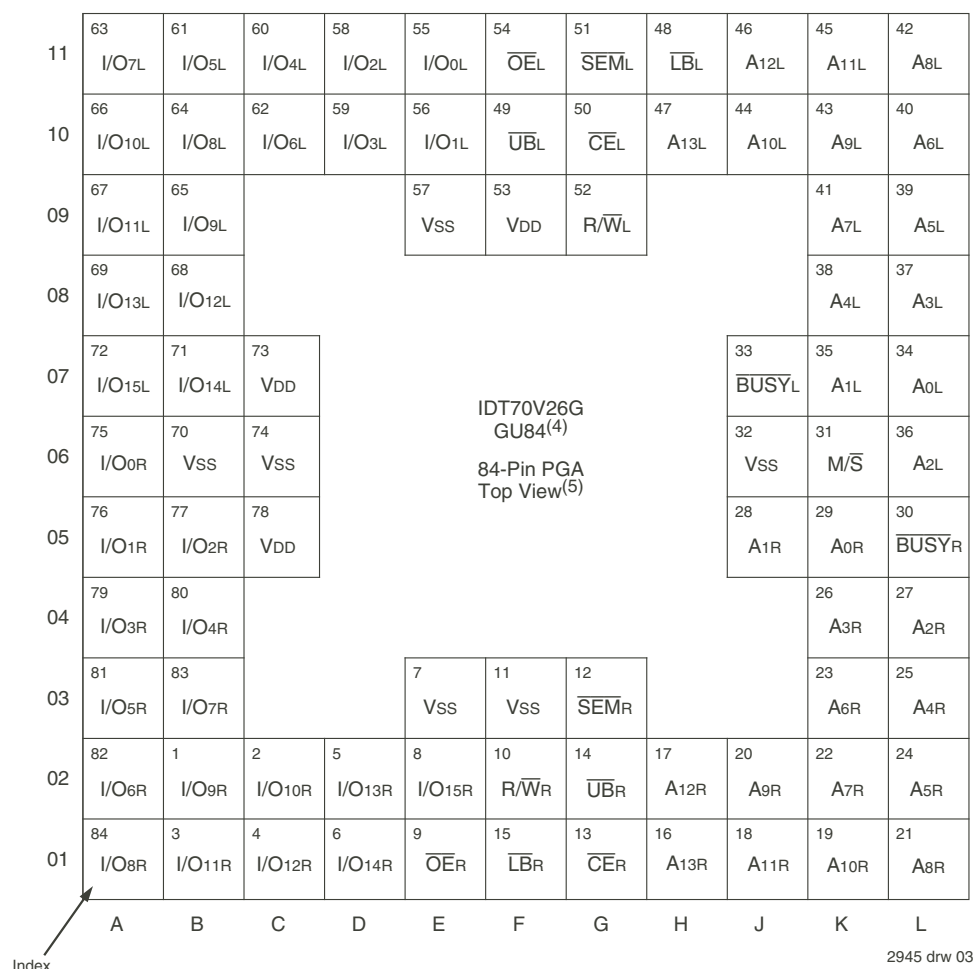
Pin Configurations^(1,2,3)



NOTES:

1. All V_{DD} pins must be connected to power supply.
2. All V_{SS} pins must be connected to ground supply.
3. Package body is approximately 1.15 in x 1.15 in x .17 in.
4. This package code is used to reference the package diagram.

Pin Configurations^(1,2,3) (con't.)



NOTES:

1. All VDD pins must be connected to power supply.
2. All VSS pins must be connected to ground supply.
3. Package body is approximately 1.12 in x 1.12 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
CEL	CEr	Chip Enable
R/WL	R/Wr	Read/Write Enable
OEL	OEr	Output Enable
A0L - A13L	A0R - A13R	Address
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output
SEML	SEMr	Semaphore Enable
UBL	UBr	Upper Byte Select
LBL	LB r	Lower Byte Select
BUSYL	BUSYr	Busy Flag
M/S		Master or Slave Select
VDD		Power (3.3V)
VSS		Ground (0V)

2945 tbl 01

Truth Table I — Non-Contention Read/Write Control

Inputs ⁽¹⁾						Outputs		Mode
\overline{CE}	R/\overline{W}	\overline{OE}	\overline{UB}	\overline{LB}	\overline{SEM}	I/O ₈₋₁₅	I/O ₀₋₇	
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected: Power-Down
L	L	X	L	H	H	DATA _{IN}	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATA _{IN}	Write to Lower Byte Only
L	L	X	L	L	H	DATA _{IN}	DATA _{IN}	Write to Both Bytes
L	H	L	L	H	H	DATA _{OUT}	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATA _{OUT}	Read Lower Byte Only
L	H	L	L	L	H	DATA _{OUT}	DATA _{OUT}	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

2945 tbl 02

NOTE:

1. A
- _{0L}
- A
- _{13L}
- ≠ A
- _{0R}
- A
- _{13R}

Truth Table II — Semaphore Read/Write Control⁽¹⁾

Inputs ⁽¹⁾						Outputs		Mode
\overline{CE}	R/\overline{W}	\overline{OE}	\overline{UB}	\overline{LB}	\overline{SEM}	I/O ₈₋₁₅	I/O ₀₋₇	
H	H	L	X	X	L	DATA _{OUT}	DATA _{OUT}	Read Data in Semaphore Flag
X	H	L	H	H	L	DATA _{OUT}	DATA _{OUT}	Read Data in Semaphore Flag
H	↑	X	X	X	L	DATA _{IN}	DATA _{IN}	Write I/O into Semaphore Flag
X	↑	X	H	H	L	DATA _{IN}	DATA _{IN}	Write I/O into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2945 tbl 03

NOTE:

1. There are eight semaphore flags written to via I/O
- ₀
- and read from all I/O's (I/O
- ₀
- I/O
- ₁₅
-). These eight semaphores are addressed by A
- ₀
- A
- ₂
- .

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT}	DC Output Current	50	mA

NOTES:

2945 tbl 04

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 0.3V.
- Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

Capacitance⁽¹⁾ (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	9	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	10	pF

2945 tbl 07

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 0.3
Industrial	-40°C to +85°C	0V	3.3V ± 0.3

2945 tbl 05

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions⁽²⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} + 0.3 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

2945 tbl 06

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{DD} + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	70V26S		70V26L		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{DD} = 3.6V, V _{IN} = 0V to V _{DD}	—	10	—	5	μA
I _{LO}	Output Leakage Current	\overline{CE} = V _{IH} , V _{OUT} = 0V to V _{DD}	—	10	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = +4mA	—	0.4	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	2.4	—	V

2945 tbl 08

NOTE:

- At V_{DD} ≤ 2.0V, input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ ($V_{DD} = 3.3V \pm 0.3V$)

Symbol	Parameter	Test Condition	Version	70V26X25 Com'l & Ind		70V26X35 Com'l Only		70V26X55 Com'l Only		Unit
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$, Outputs Disabled $SEM = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L S	100	170	90	140	90	140	mA
			L	100	140	90	120	90	120	
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R = \overline{CE}_L = V_{IH}$ $SEM_R = SEM_L = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L S	14	30	12	30	12	30	mA
			L	12	24	10	24	10	24	
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{A^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ $SEM_R = SEM_L = V_{IH}$	COM'L S	50	95	45	87	45	87	mA
			L	50	85	45	75	45	75	
I _{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} < 0.2V$, $f = 0^{(4)}$ $SEM_R = SEM_L \geq V_{DD} - 0.2V$	COM'L S	1.0	6	1.0	6	1.0	6	mA
			L	0.2	3	0.2	3	0.2	3	
I _{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{A^*} \leq 0.2V$ and $\overline{CE}_{B^*} \geq V_{DD} - 0.2V^{(5)}$ $SEM_R = SEM_L \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L S	60	90	55	85	55	85	mA
			L	60	80	55	74	55	74	
			IND S	60	125	—	—	—	—	mA
			L	60	90	—	—	—	—	

NOTES:

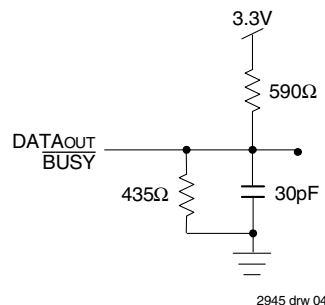
2945 tbl 09

- 'X' in part number indicates power rating (S or L)
- $V_{DD} = 3.3V$, $T_A = +25^\circ C$, and are not production tested. $I_{CCDC} = 80mA$ (Typ.)
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- $f = 0$ means no address or control lines change.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Test Conditions

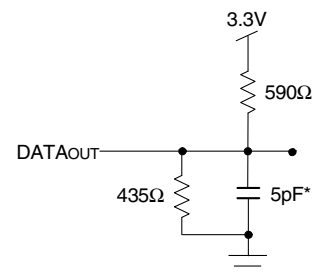
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2945 tbl 10



2945 drw 04

Figure 1. AC Output Test Load



2945 drw 05

Figure 2. Output Test Load
(for tLZ, tHZ, tWZ, tOW)
* Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁴⁾

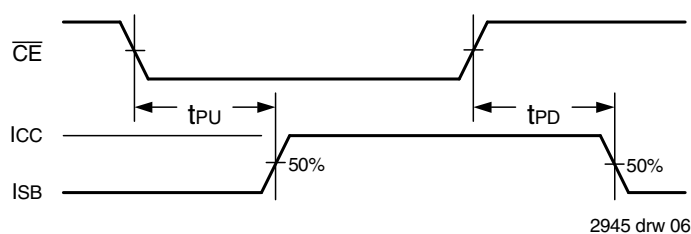
Symbol	Parameter	70V26X25 Com'l & Ind		70V26X35 Com'l Only		70V26X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time ⁽³⁾	—	25	—	35	—	55	ns
tABE	Byte Enable Access Time ⁽³⁾	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time ^(1,2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time ⁽²⁾	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time ⁽²⁾	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{\text{OE}}$ or $\overline{\text{SEM}}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

2945 tbl 11

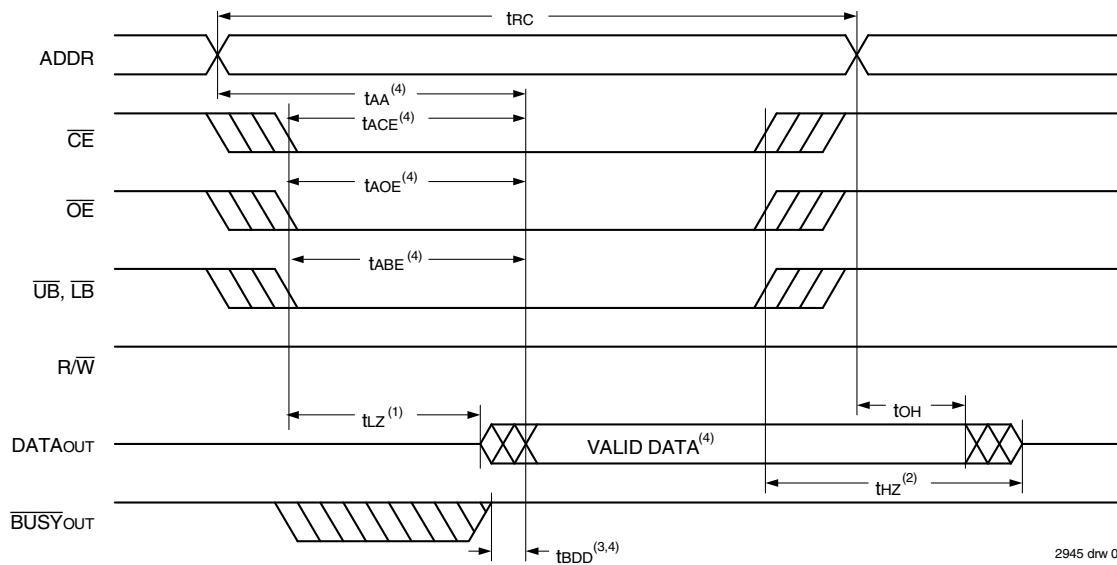
NOTES:

1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$.
4. 'X' in part number indicates power rating (S or L).

Timing of Power-Up Power-Down



Waveform of Read Cycles⁽⁵⁾



NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} , \overline{CE} , \overline{LB} , or \overline{UB} .
2. Timing depends on which signal is de-asserted first, \overline{CE} , \overline{OE} , \overline{LB} , or \overline{UB} .
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations \overline{BUSY} has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM} = V_{IH}$.

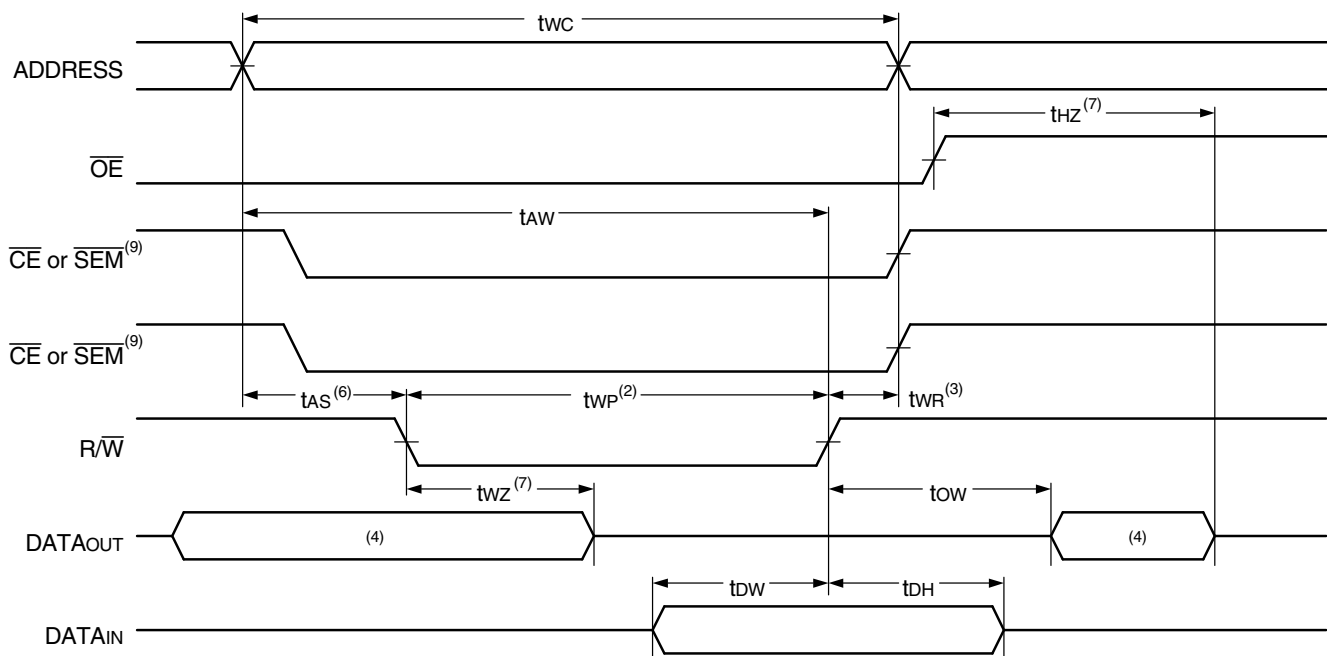
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

Symbol	Parameter	70V26X25 Com'l & Ind		70V26X35 Com'l Only		70V26X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write ⁽³⁾	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time ⁽³⁾	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time ^(1,2)	—	15	—	20	—	25	ns
tDH	Data Hold Time ⁽⁴⁾	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z ^(1,2)	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write ^(1,2,4)	0	—	0	—	0	—	ns
tSWRD	SEM Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	SEM Flag Contention Window	5	—	5	—	5	—	ns

NOTES:

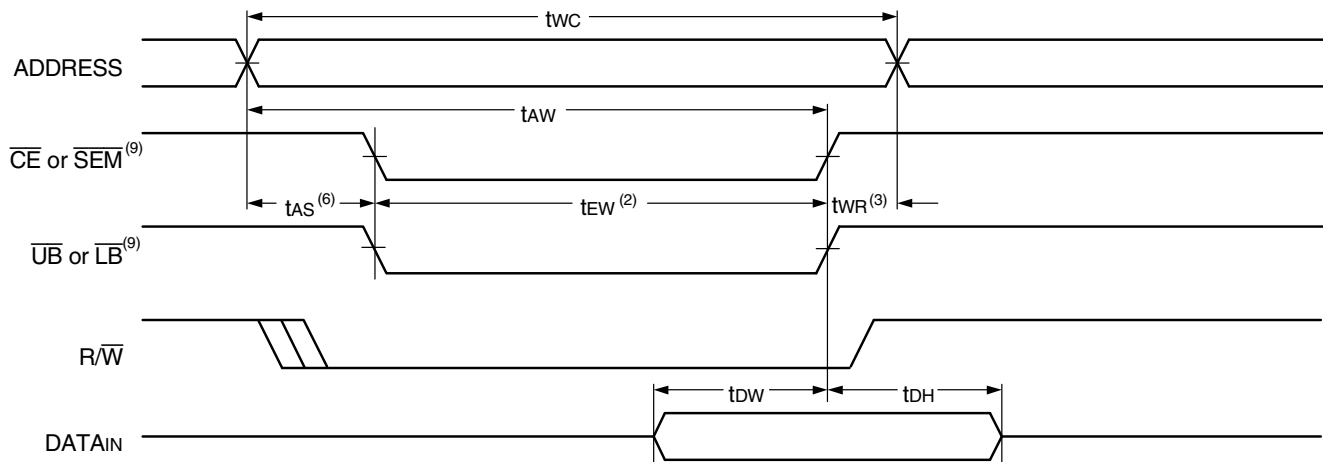
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, $\overline{R/\overline{W}}$ Controlled Timing^(1,5,8)



2945 drw 08

Timing Waveform of Write Cycle No. 2, \overline{CE} , \overline{UB} , \overline{LB} Controlled Timing^(1,5)

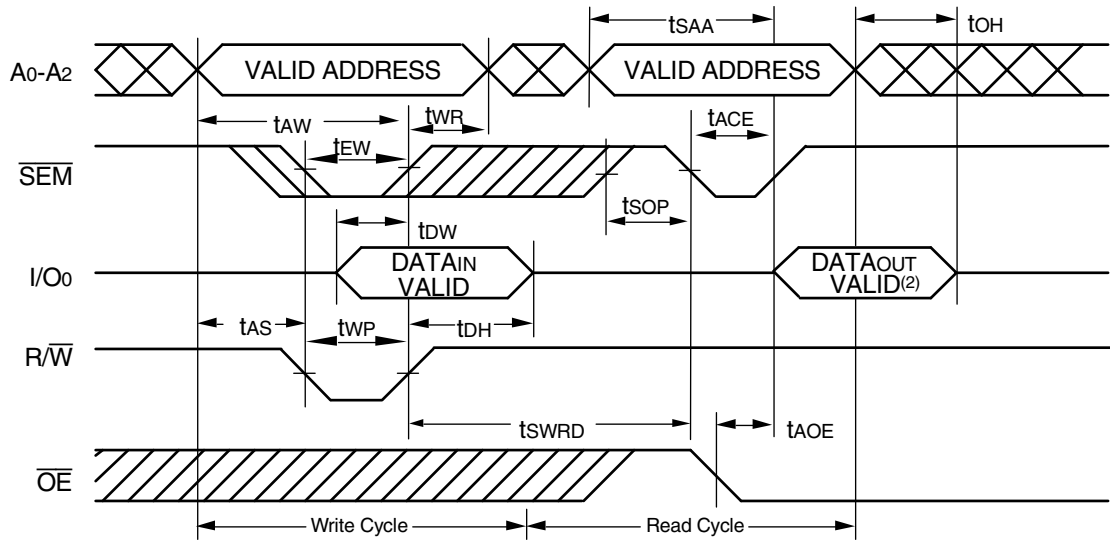


2945 drw 09

NOTES:

1. $\overline{R/\overline{W}}$ or \overline{CE} or \overline{UB} and \overline{LB} must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW \overline{CE} and a LOW $\overline{R/\overline{W}}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of \overline{CE} or $\overline{R/\overline{W}}$ (or \overline{SEM} or $\overline{R/\overline{W}}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} or \overline{SEM} LOW transition occurs simultaneously with or after the $\overline{R/\overline{W}}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \overline{CE} or $\overline{R/\overline{W}}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If \overline{OE} is LOW during $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
9. To access RAM, $\overline{CE} = V_{IL}$ and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ and $\overline{SEM} = V_{IL}$. t_{EW} must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side⁽¹⁾

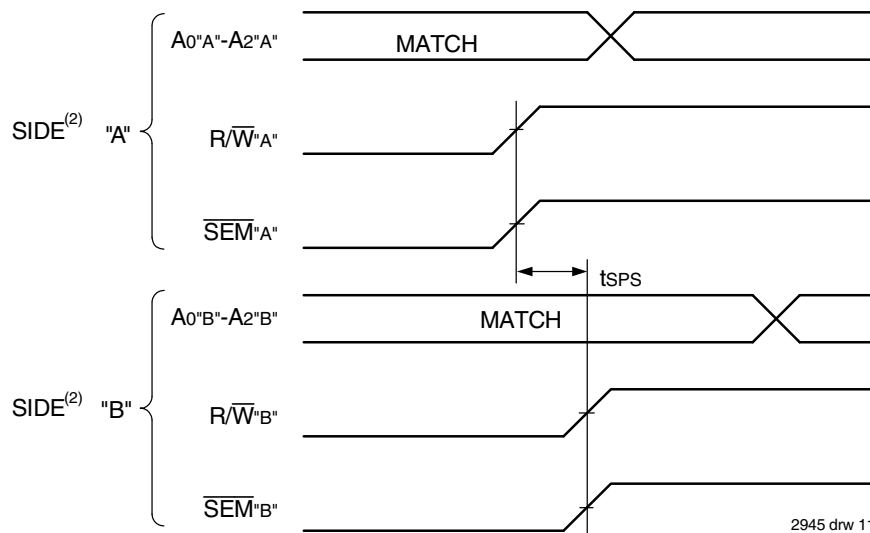


2945 drw 10

NOTES:

1. $\overline{CE} = V_{IH}$ or $\overline{UB} \& \overline{LB} = V_{IH}$ for the duration of the above timing (both write and read cycle).
2. "DATAOUT VALID" represents all I/O's (I/O₀-I/O₁₅) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention^(1,3,4)



2945 drw 11

NOTES:

1. $DOR = DOL = V_{IL}$, $\overline{CE}_R = \overline{CE}_L = V_{IH}$, or both $\overline{UB} \& \overline{LB} = V_{IH}$.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/\overline{W} "A" or \overline{SEM} "A" going HIGH to R/\overline{W} "B" or \overline{SEM} "B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁶⁾

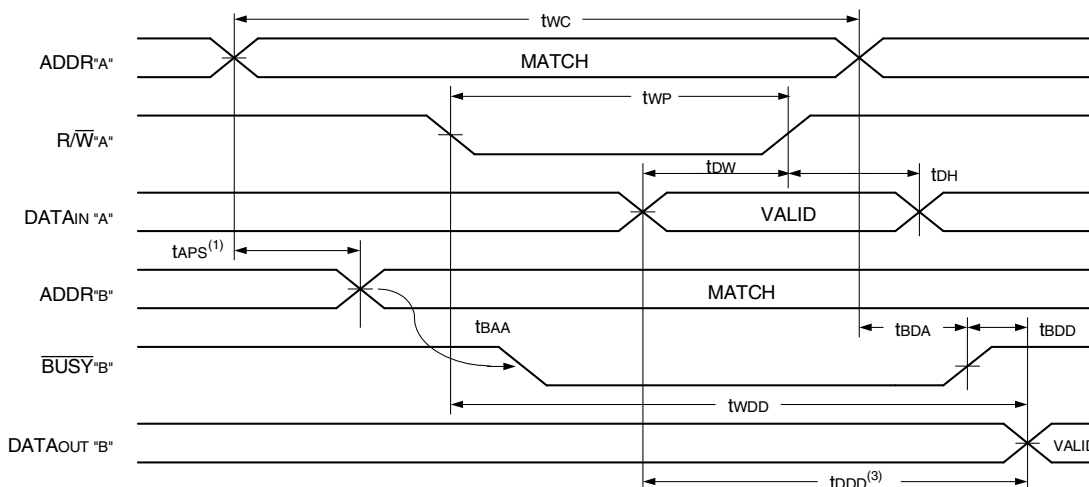
Symbol	Parameter	70V26X25 Com'l & Ind		70V26X35 Com'l Only		70V26X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S̄ = VIH)								
tBAA	BUSY Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	BUSY Disable Time from Address Not Match	—	25	—	35	—	45	ns
tBAC	BUSY Access Time from Chip Enable Low	—	25	—	35	—	45	ns
tBDC	BUSY Disable Time from Chip Enable High	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time ⁽²⁾	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data ⁽³⁾	—	35	—	40	—	50	ns
tWH	Write Hold After BUSY ⁽⁵⁾	20	—	25	—	25	—	ns
BUSY INPUT TIMING (M/S̄ = VIL)								
tWB	BUSY Input to Write ⁽⁴⁾	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY ⁽⁵⁾	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay ⁽¹⁾	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay ⁽¹⁾	—	50	—	60	—	80	ns

2945 tbl 13

NOTES:

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and \overline{BUSY} ($M/\bar{S} = V_{IH}$)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part number indicates power rating (S or L).

Timing Waveform of Write with Port-to-Port Read and \overline{BUSY} ^(2,4,5)

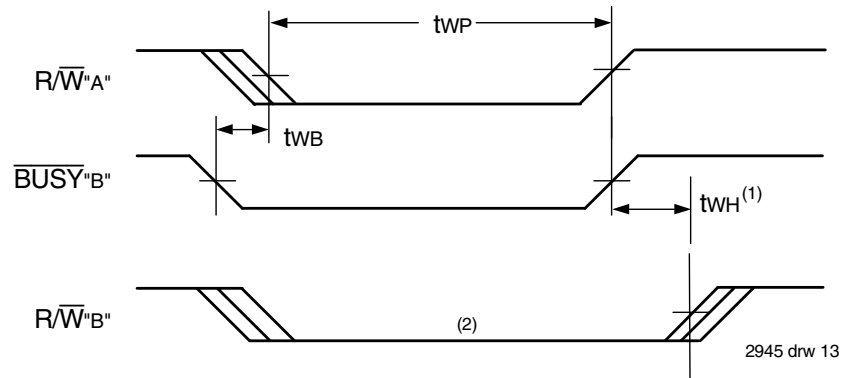


NOTES:

1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\bar{S} = V_{IL}$ (SLAVE).
2. $\overline{CE_L} = \overline{CE_R} = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. If $M/\bar{S} = V_{IL}$ (SLAVE), then \overline{BUSY} is an input ($\overline{BUSY}'A' = V_{IH}$ and $\overline{BUSY}'B' = \text{"don't care"}$, for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

2945 drw 12

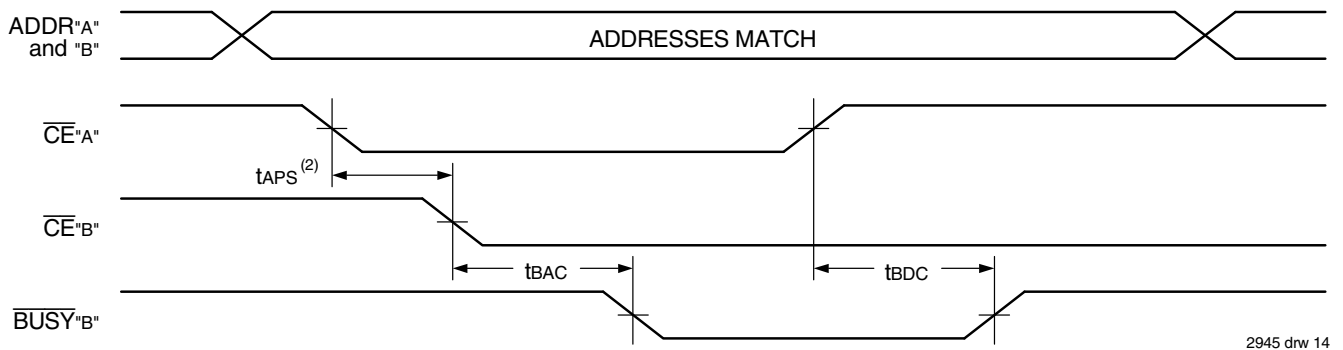
Timing Waveform of Write with **BUSY**



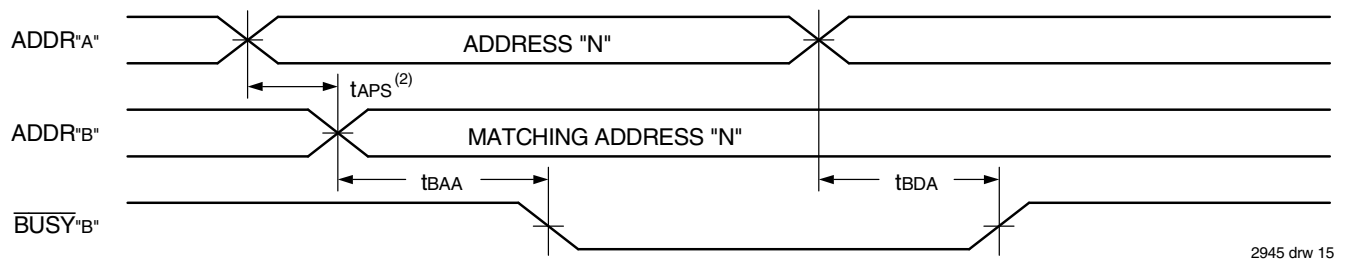
NOTES:

1. t_{WH} must be met for both \overline{BUSY} input (SLAVE) and output (MASTER).
2. \overline{BUSY} is asserted on port "B" blocking R/\overline{W} "B", until \overline{BUSY} "B" goes HIGH.

Waveform of **BUSY** Arbitration Controlled by \overline{CE} Timing⁽¹⁾



Waveform of **BUSY** Arbitration Cycle Controlled by Address Match Timing⁽¹⁾



NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If t_{APS} is not satisfied, the \overline{BUSY} signal will be asserted on one side or the other, but there is no guarantee on which side \overline{BUSY} will be asserted.

Truth Table III — Address **BUSY** Arbitration

Inputs			Outputs		Function
\overline{CE}_L	\overline{CE}_R	A0L-A13L A0R-A13R	$\overline{BUSY}_L^{(1)}$	$\overline{BUSY}_R^{(1)}$	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

2945 tbl 14

NOTES:

1. Pins \overline{BUSY}_L and \overline{BUSY}_R are both outputs when the part is configured as a master. Both are inputs when configured as a slave. \overline{BUSY}_x outputs on the IDT70V26 are push pull, not open drain outputs. On slaves the \overline{BUSY}_x input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either \overline{BUSY}_L or \overline{BUSY}_R = LOW will result. \overline{BUSY}_L and \overline{BUSY}_R outputs cannot be LOW simultaneously.
3. Writes to the left port are internally ignored when \overline{BUSY}_L outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when \overline{BUSY}_R outputs are driving LOW regardless of actual logic level on the pin.

Truth Table IV — Example of Semaphore Procurement Sequence^(1,2,3)

Functions	D0 - D15 Left	D0 - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2945 tbl 15

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V26.
2. There are eight semaphore flags written to via I/O₀ and read from all I/O's (I/O₀-I/O₁₅). These eight semaphores are addressed by A0-A2.
3. $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$ to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT70V26 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V26 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (\overline{CE} HIGH). When a port is enabled, access to the entire memory array is permitted.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the

RAM is "busy". The \overline{BUSY} pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a \overline{BUSY} indication, the write signal is gated internally to prevent the write from proceeding.

The use of \overline{BUSY} logic is not required or desirable for all applications. In some cases it may be useful to logically OR the \overline{BUSY} outputs together and use any \overline{BUSY} indication as an interrupt source to flag an illegal or illogical operation. If the write inhibit function of \overline{BUSY} logic is not desirable, the \overline{BUSY} logic can be disabled by placing the part in slave mode with the $\overline{M/\overline{S}}$ pin. Once in slave mode the \overline{BUSY} pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the \overline{BUSY} pins HIGH. If desired, unintended

standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table IV). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (\overline{SEM}) and output enable (\overline{OE}) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal (\overline{SEM} or \overline{OE}) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table IV). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a

semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

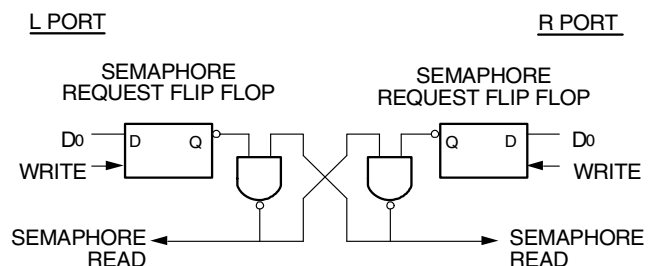
Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V26's Dual-Port RAM. Say the 16K x 16 RAM was to be divided into two 8K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could



2945 drw 17

Figure 4. IDT70V26 Semaphore Logic

undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.



Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continu-

ously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

Datasheet Document History

03/25/99:	Initiated datasheet document history Converted to new format Cosmetic and typographical corrections Page 2 and 3 Added additional notes to pin configurations
06/10/99:	Changed drawing format
08/06/99:	Page 1 Removed Preliminary
08/30/99:	Page 1 Changed 660mW to 660μW
11/12/99:	Replaced IDT logo
06/06/00:	Page 5 Increased storage temperature parameter & Clarified TA parameter Page 6 DC Electrical parameters—changed wording from "open" to "disabled" Changed ±200mV to 0mV in notes
07/21/03:	Page 2 & 3 Added date revision to pin configurations Page 2, 3, 5 -8 & 11 Changed naming conventions from V _{CC} to V _{DD} and from GND to V _{SS} Page 6 Added Industrial temp to DC Electrical Characteristics for standard power and low power for 25ns speed Page 7, 8 & 11 Added Industrial temp to AC Electrical Characteristics for 25ns speed Page 1 & 17 Added Industrial temp at 25ns to Features and in ordering information Page 1 & 17 Updated IDT logo from  to 
02/15/08:	Page 1 Added green availability to features Page 17 Added green indicator to ordering information Page 17 Added die stepping indicator to ordering information
01/19/09:	Page 17 Removed "IDT" from orderable part number
06/14/18:	Page 17 Removed the "Step" indicator and the note and added the T&R to the ordering information Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018
07/26/19:	Page 1 & 17 Deleted obsolete Industrial speed grade 25ns in Features and Ordering Information Page 2 Rotated PLG84 PLCC pin configuration to accurately reflect pin 1 orientation Page 17 Added Orderable Part Information table

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