



## Description

The IDT70T06/5 is a high-speed 16/8K x 8 Dual-Port Static RAM. The IDT70T06/5 is designed to be used as a stand-alone 128K-bit Dual-Port Static RAM or as a combination MASTER/SLAVE Dual-Port Static RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port Static RAM approach in 16-bit-or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

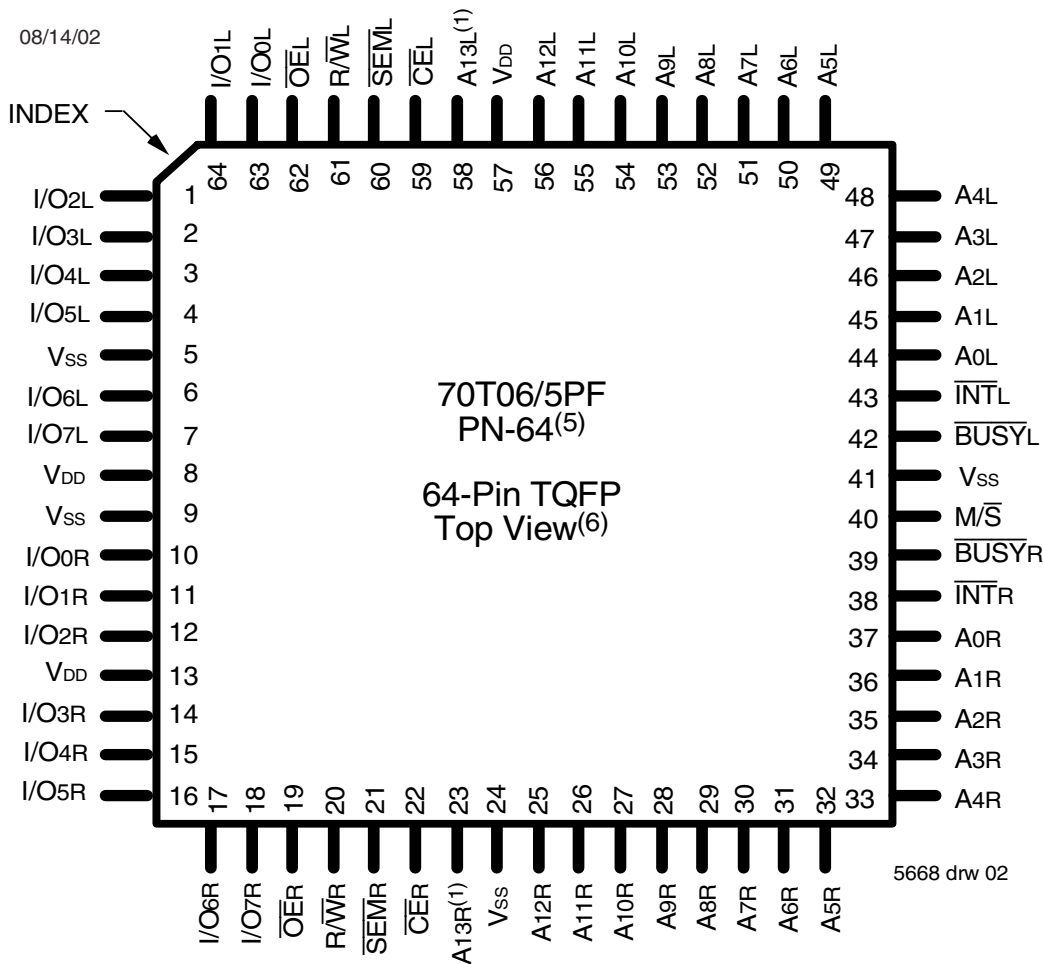
This device provides two independent ports with separate control,

address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by  $\overline{CE}$  permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 200mW of power.

The IDT70T06/5 is packaged in a 64-pin Thin Quad Flatpack and 100-pin fine pitch Ball Grd Array.

## Pin Configurations<sup>(1,2,3,4)</sup>



### NOTES:

1. A13 is a NC for IDT70T05.
2. All V<sub>DD</sub> pins must be connected to power supply.
3. All V<sub>SS</sub> pins must be connected to ground supply.
4. PN-64 package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part marking.

## Pin Configurations<sup>(1,2,3,4)</sup> (con't.)

IDT70T06/5BF  
BF100<sup>(5)</sup>

100-Pin fpBGA  
Top View<sup>(6)</sup>

08/14/02

A1 A6R	A2 A9R	A3 A12R	A4 NC	A5 VSS	A6 VSS	A7 NC	A8 R/W <sub>R</sub>	A9 NC	A10 I/O7R
B1 NC	B2 NC	B3 A8R	B4 A10R	B5 NC	B6 NC	B7 A13R <sup>(1)</sup>	B8 O <sub>E</sub> R	B9 NC	B10 I/O6R
C1 A3R	C2 A4R	C3 A5R	C4 A7R	C5 NC	C6 NC	C7 C <sub>E</sub> R	C8 NC	C9 NC	C10 I/O3R
D1 A1R	D2 I <sub>N</sub> T <sub>R</sub>	D3 A2R	D4 NC	D5 A11R	D6 NC	D7 S <sub>E</sub> M <sub>R</sub>	D8 NC	D9 I/O5R	D10 I/O1R
E1 M/S	E2 B <sub>U</sub> S <sub>Y</sub> R	E3 A0R	E4 A1L	E5 VSS	E6 VSS	E7 I/O4R	E8 I/O2R	E9 I/O0R	E10 VDD
F1 VSS	F2 B <sub>U</sub> S <sub>Y</sub> L	F3 A0L	F4 NC	F5 VDD	F6 VSS	F7 VDD	F8 I/O5L	F9 I/O6L	F10 I/O7L
G1 I <sub>N</sub> T <sub>L</sub>	G2 A3L	G3 A6L	G4 NC	G5 NC	G6 S <sub>E</sub> M <sub>L</sub>	G7 NC	G8 I/O3L	G9 VSS	G10 I/O4L
H1 A2L	H2 A5L	H3 A10L	H4 NC	H5 NC	H6 C <sub>E</sub> L	H7 NC	H8 NC	H9 NC	H10 I/O2L
J1 A4L	J2 A8L	J3 A11L	J4 NC	J5 NC	J6 A13L <sup>(1)</sup>	J7 R/W <sub>L</sub>	J8 NC	J9 VSS	J10 I/O1L
K1 A7L	K2 A9L	K3 A12L	K4 NC	K5 VDD	K6 VDD	K7 NC	K8 NC	K9 O <sub>E</sub> L	K10 I/O0L

5668 drw 03

### NOTES:

1. A13 is a NC for IDT70T05.
2. All VDD pins must be connected to power supply.
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 1.18 in x 1.18 in x .16 in.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}^{(1)}$	$A_{0R} - A_{13R}^{(1)}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$BUSY_L$	$BUSY_R$	Busy Flag
M/ $\overline{S}$		Master or Slave Select
$V_{DD}$		Power (2.5V)
$V_{SS}$		Ground (0V)

5668 tbl 01

**NOTE:**

1. A13 is a NC for IDT70T05.

## Truth Table I: Non-Contention Read/Write Control

Inputs <sup>(1)</sup>				Outputs	Mode
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O <sub>0-7</sub>	
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATA <sub>IN</sub>	Write to Memory
L	H	L	H	DATA <sub>OUT</sub>	Read Memory
X	X	H	X	High-Z	Outputs Disabled

5668 tbl 02

**NOTE:**

1. A<sub>0L</sub> — A<sub>13L</sub> ≠ A<sub>0R</sub> — A<sub>13R</sub>

## Truth Table II: Semaphore Read/Write Control<sup>(1)</sup>

Inputs				Outputs	Mode
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O <sub>0-7</sub>	
H	H	L	L	DATA <sub>OUT</sub>	Read Data in Semaphore Flag
H	↑	X	L	DATA <sub>IN</sub>	Write I/O <sub>0</sub> into Semaphore Flag
L	X	X	L	—	Not Allowed

5668 tbl 03

**NOTE:**

1. There are eight semaphore flags written to via I/O<sub>0</sub> and read from I/O<sub>0</sub> - I/O<sub>7</sub>. These eight semaphores are addressed by A<sub>0</sub> - A<sub>7</sub>.

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +3.6	V
T <sub>BIAS</sub> <sup>(3)</sup>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>JN</sub>	Junction Temperature	+150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

5668 tbl 04

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V.
- Ambient Temperature Under Bias. No AC Conditions. Chip Deselected.

### Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

5668 tbl 07

**NOTES:**

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

### Maximum Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	2.5V ± 100mV
Industrial	-40°C to +85°C	0V	2.5V ± 100mV

5668 tbl 05

**NOTE:**

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	2.4	2.5	2.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	1.7	—	V <sub>DD</sub> +0.3 <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

5668 tbl 06

**NOTES:**

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10ns.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T06/5L		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DD</sub> = 2.6V, V <sub>IN</sub> = 0V to V <sub>DD</sub>	—	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>DD</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +2mA	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2mA	2.0	—	V

5668 tbl 08

**NOTE:**

- At V<sub>DD</sub> ≤ 2.0V input leakages are undefined.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 2.5V ± 100mV)

Symbol	Parameter	Test Condition	Version	70T06/5L20 Com'l Only		70T06/5L25 Com'l & Ind		Unit
				Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	
I <sub>DD</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ , Outputs Disabled $\overline{SEM} = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L L	80	140	70	130	mA
			IND L	—	—	100	160	
I <sub>SB1</sub>	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_R$ and $\overline{CE}_L = V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L L	12	20	7	17	mA
			IND L	—	—	12	25	
I <sub>SB2</sub>	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{A^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(1)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$	COM'L L	55	90	40	80	mA
			IND L	—	—	55	100	
I <sub>SB3</sub>	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(4)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$	COM'L L	0.05	2.5	0.05	2.5	mA
			IND L	—	—	0.2	5.0	
I <sub>SB4</sub>	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{A^*} \leq 0.2V$ and $\overline{CE}_{B^*} \geq V_{DD} - 0.2V^{(1)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{DD} - 0.2V$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L L	55	90	40	80	mA
			IND L	—	—	55	100	

5668 tbl 09

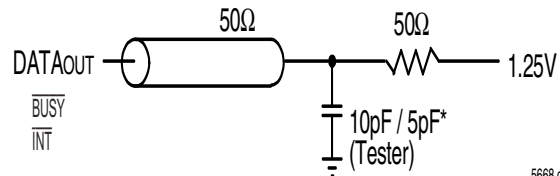
**NOTES:**

- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- V<sub>DD</sub> = 2.5V, T<sub>A</sub> = +25°C, and are not production tested. I<sub>DD</sub> dc = 85mA (typ.)
- At f = f<sub>MAX</sub>, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t<sub>RC</sub>, and using "AC Test Conditions" of input levels of GND to 3V.
- f = 0 means no address or control lines change.

## AC Test Conditions

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.25V
Output Reference Levels	1.25V
Output Load	Figure 1

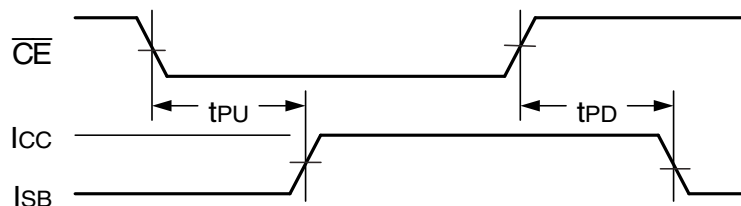
5668 tbl 10



5668 drw 04

Figure 1. AC Output Test Load  
\*(For t<sub>LZ</sub>, t<sub>HZ</sub>, t<sub>WZ</sub>, t<sub>OW</sub>)

## Timing of Power-Up Power-Down



5668 drw 05

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

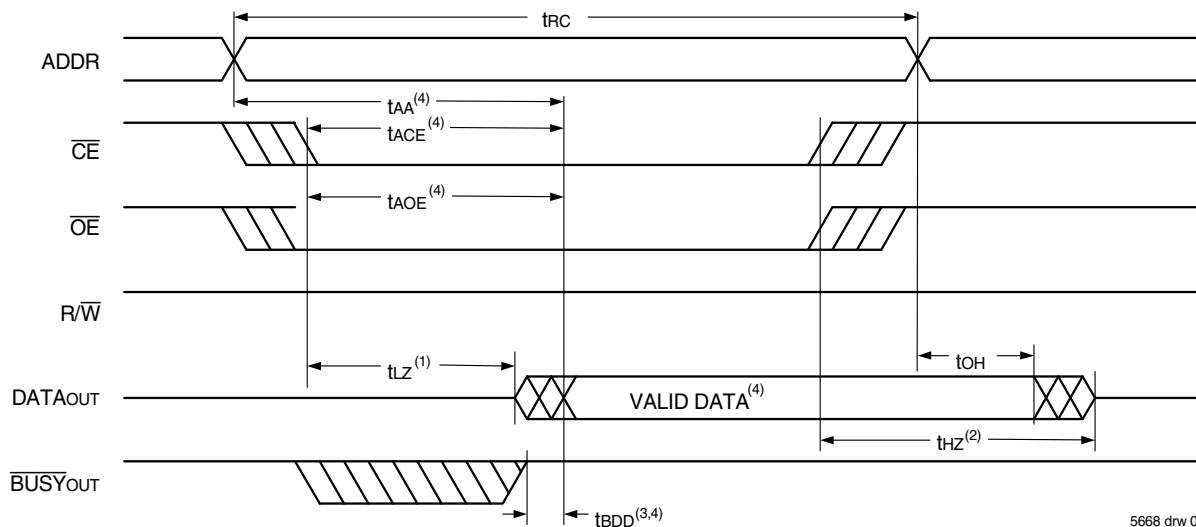
Symbol	Parameter	70T06/5L20 Com'l Only		70T06/5L25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	ns
t <sub>ACE</sub>	Chip Enable Access Time <sup>(3)</sup>	—	20	—	25	ns
t <sub>ABE</sub>	Byte Enable Access Time <sup>(3)</sup>	—	20	—	25	ns
t <sub>AOE</sub>	Output Enable Access Time <sup>(3)</sup>	—	12	—	13	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1,2)</sup>	3	—	3	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(1,2)</sup>	0	—	0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(1,2)</sup>	—	20	—	25	ns
t <sub>SOP</sub>	Semaphore Flag Update Pulse ( $\overline{OE}$ or $\overline{SEM}$ )	10	—	10	—	ns
t <sub>SAA</sub>	Semaphore Address Access <sup>(3)</sup>	—	20	—	25	ns

5668 tbl 11

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM,  $\overline{CE} = V_{IL}$  and  $\overline{SEM} = V_{IH}$ . To access semaphore,  $\overline{CE} = V_{IH}$  and  $\overline{SEM} = V_{IL}$ .

### Waveform of Read Cycles<sup>(5)</sup>



5668 drw 06

**NOTES:**

1. Timing depends on which signal is asserted last  $\overline{OE}$  or  $\overline{CE}$ .
2. Timing depends on which signal is de-asserted first  $\overline{CE}$  or  $\overline{OE}$ .
3. t<sub>BDD</sub> delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations  $\overline{BUSY}$  has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t<sub>AOE</sub>, t<sub>ACE</sub>, t<sub>AA</sub> or t<sub>BDD</sub>.
5.  $\overline{SEM} = V_{IH}$ .

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

Symbol	Parameter	70T06/5L20 Com'l Only		70T06/5L25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>						
tWC	Write Cycle Time	20	—	25	—	ns
tEW	Chip Enable to End-of-Write <sup>(3)</sup>	15	—	20	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time <sup>(3)</sup>	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	ns
tHZ	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	ns
tDH	Data Hold Time <sup>(4)</sup>	0	—	0	—	ns
twZ	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	12	—	15	ns
tOW	Output Active from End-of-Write <sup>(1,2,4)</sup>	0	—	0	—	ns
tSWRD	$\overline{\text{SEM}}$ Flag Write to Read Time	5	—	5	—	ns
tSPS	$\overline{\text{SEM}}$ Flag Contention Window	5	—	5	—	ns

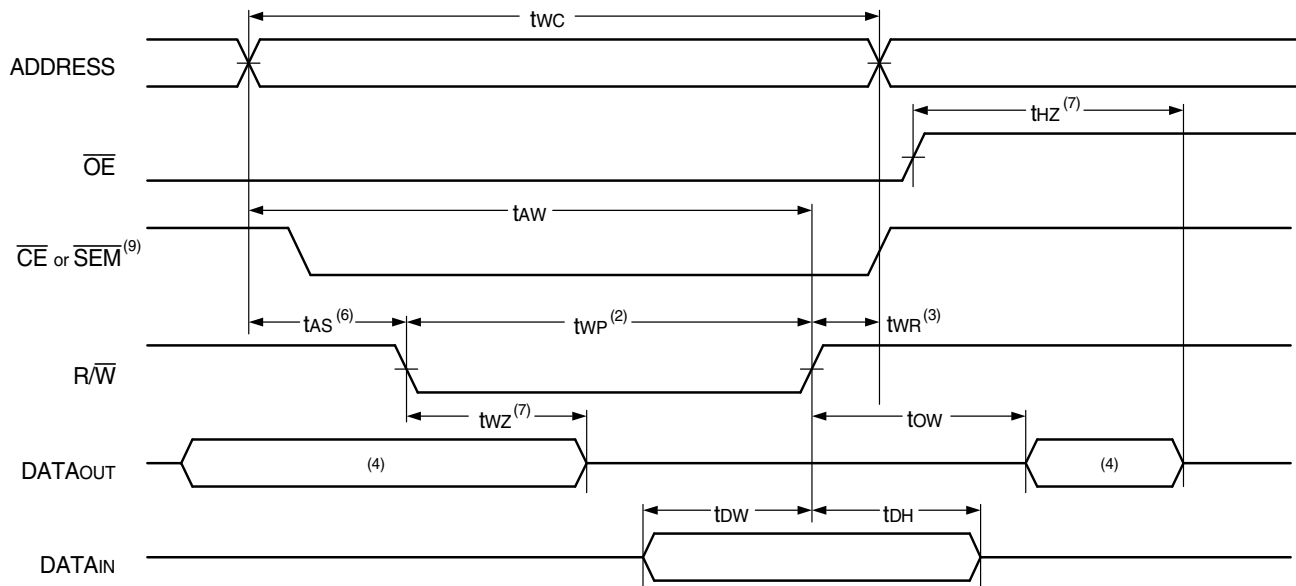
5668 tbl 12

### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 1).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access SRAM,  $\overline{\text{CE}} = \text{V}_{\text{IL}}$ ,  $\overline{\text{SEM}} = \text{V}_{\text{IH}}$ . To access semaphore,  $\overline{\text{CE}} = \text{V}_{\text{IH}}$  and  $\overline{\text{SEM}} = \text{V}_{\text{IL}}$ . Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the SRAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.

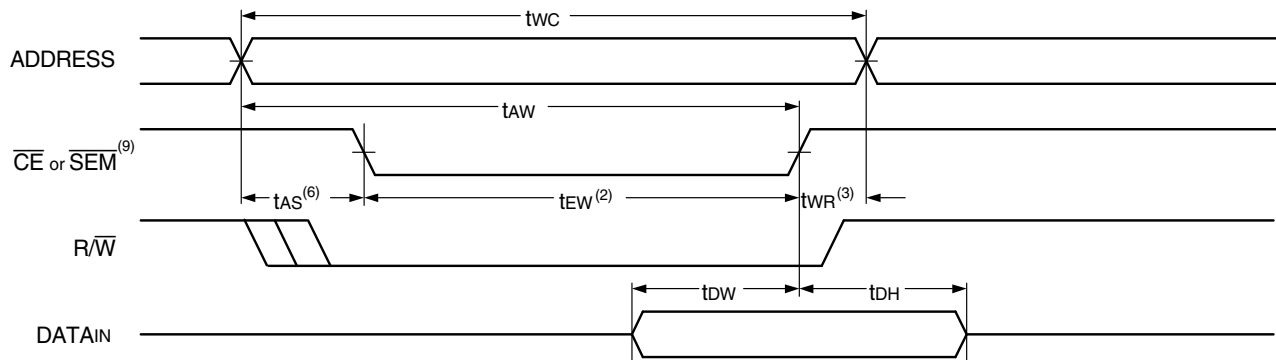


### Timing Waveform of Write Cycle No. 1, R/W Controlled Timing<sup>(1,3,5,8)</sup>



5668 drw 07

### Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing<sup>(1,3,5,8)</sup>

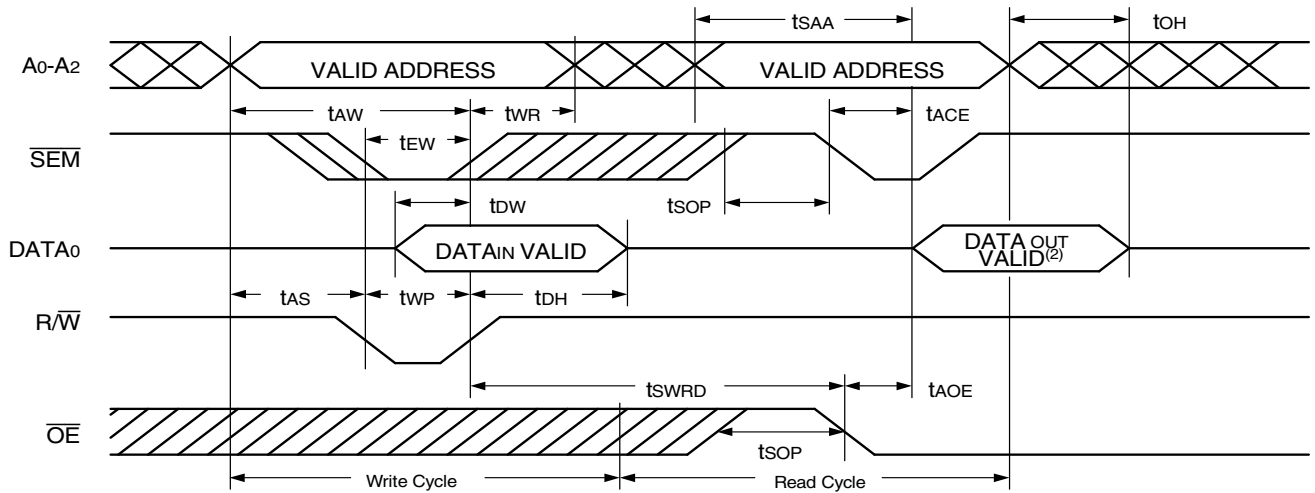


5668 drw 08

**NOTES:**

1.  $R/\overline{W}$  or  $\overline{CE}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a LOW  $\overline{CE}$  and a LOW  $R/\overline{W}$  for memory array writing cycle.
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $R/\overline{W}$  (or  $\overline{SEM}$  or  $R/\overline{W}$ ) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the  $\overline{CE}$  or  $\overline{SEM}$  LOW transition occurs simultaneously with or after the  $R/\overline{W}$  low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last  $\overline{CE}$  or  $R/\overline{W}$ .
7. Timing depends on which enable signal is de-asserted first  $\overline{CE}$  or  $R/\overline{W}$ .
8. If  $\overline{OE}$  is LOW during  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WZ} + t_{DW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE}$  is HIGH during an  $R/\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .
9. To access SRAM,  $\overline{CE} = V_{IL}$  and  $\overline{SEM} = V_{IH}$ . To access Semaphore,  $\overline{CE} = V_{IH}$  and  $\overline{SEM} = V_{IL}$ .  $t_{EW}$  must be met for either condition.

### Timing Waveform of Semaphore Read after Write Timing, Either Side<sup>(1)</sup>

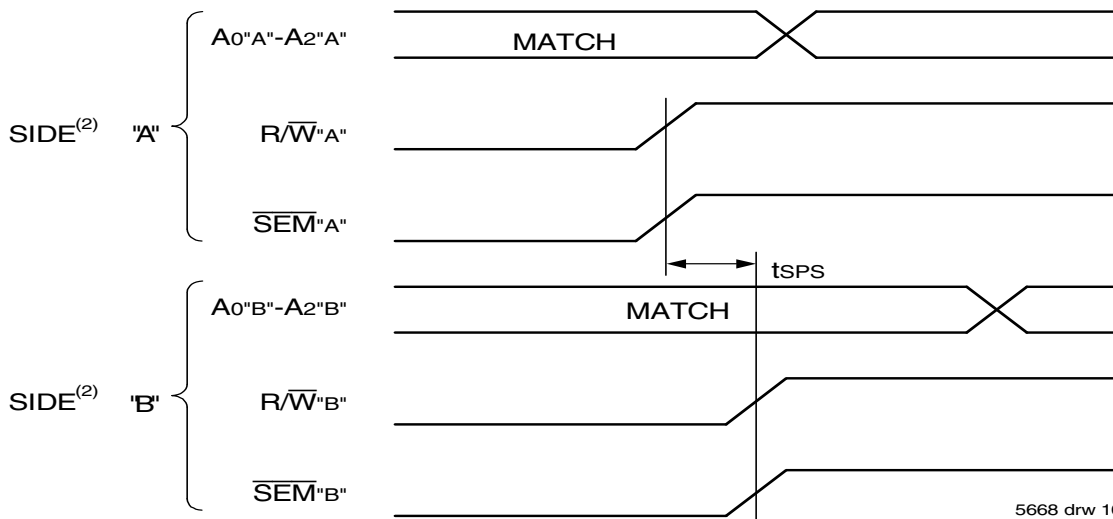


5668 drw 09

**NOTES:**

1.  $\overline{CE} = V_{IH}$  for the duration of the above timing (both write and read cycle).
2. "DATAOUT VALID" represents all I/O's (I/O<sub>0</sub> - I/O<sub>7</sub>) equal to the semaphore value.

### Timing Waveform of Semaphore Write Contention<sup>(1,3,4)</sup>



5668 drw 10

**NOTES:**

1.  $D_{OR} = D_{OL} = V_{IL}$ ,  $\overline{CE}_R = \overline{CE}_L = V_{IH}$ , Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from  $R/\overline{W}$ "A" or  $\overline{SEM}$ "A" going HIGH to  $R/\overline{W}$ "B" or  $\overline{SEM}$ "B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

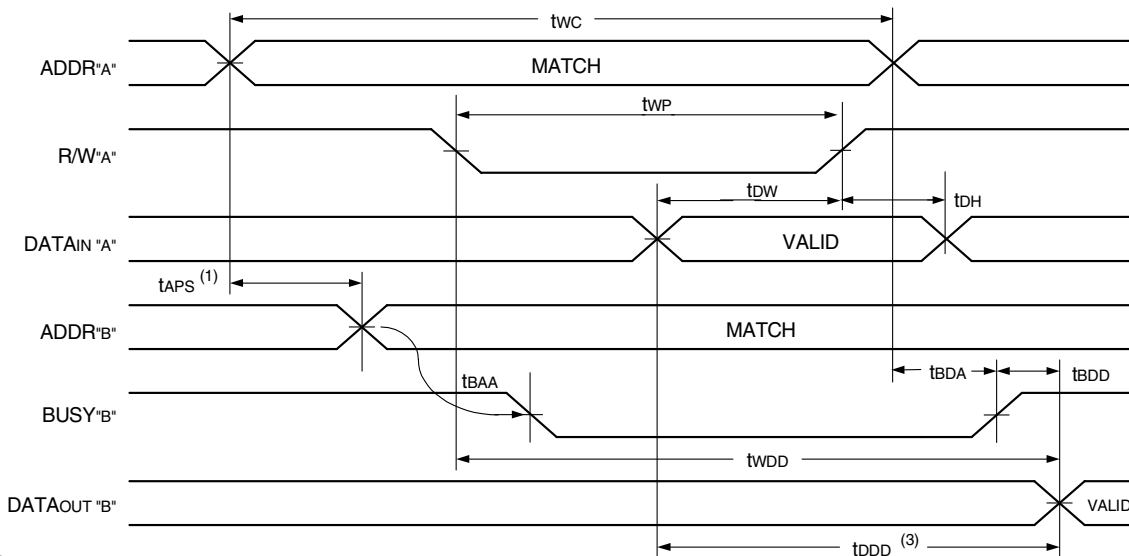
Symbol	Parameter	70T06/5L20 Com'l Only		70T06/5L25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
<b>BUSY TIMING (<math>M/\bar{S} = V_{IH}</math>)</b>						
tBAA	$\overline{\text{BUSY}}$ Access Time from Address Match	—	20	—	20	ns
tBDA	$\overline{\text{BUSY}}$ Disable Time from Address Not Matched	—	20	—	20	ns
tBAC	$\overline{\text{BUSY}}$ Access Time from Chip Enable LOW	—	20	—	20	ns
tBDC	$\overline{\text{BUSY}}$ Disable Time from Chip Enable HIGH	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time <sup>(2)</sup>	5	—	5	—	ns
tBDD	$\overline{\text{BUSY}}$ Disable to Valid Data <sup>(3)</sup>	—	30	—	30	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	15	—	17	—	ns
<b>BUSY TIMING (<math>M/\bar{S} = V_{IL}</math>)</b>						
tWB	$\overline{\text{BUSY}}$ Input to Write <sup>(4)</sup>	0	—	0	—	ns
tWH	Write Hold After $\overline{\text{BUSY}}$ <sup>(6)</sup>	15	—	17	—	ns
<b>PORT-TO-PORT DELAY TIMING</b>						
twDD	Write Pulse to Data Delay <sup>(1)</sup>	—	45	—	50	ns
tdDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	35	—	35	ns

5668 tbl 13

### NOTES:

- Port-to-port delay through SRAM cells from writing port to reading port, refer to "Timing Waveform of Write Port-To-Port Read and  $\overline{\text{BUSY}}$  ( $M/\bar{S} = V_{IH}$ )".
- To ensure that the earlier of the two ports wins.
- tBDD is a calculated parameter and is the greater of 0, twDD – twP (actual) or tDD – tdW (actual).
- To ensure that the write cycle is inhibited during contention.
- To ensure that a write cycle is completed after contention.

## Timing Waveform of Write Port-to-Port Read and $\overline{\text{BUSY}}^{(2,4,5)}$ ( $M/\bar{S} = V_{IH}$ )

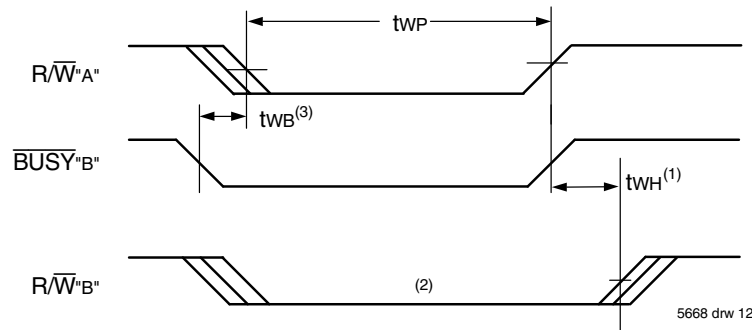


### NOTES:

- To ensure that the earlier of the two ports wins. tAPS is ignored for  $M/\bar{S} = V_{IL}$  (SLAVE).
- $\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$
- $\overline{\text{OE}} = V_{IL}$  for the reading port.
- If  $M/\bar{S} = V_{IL}$  (slave) then  $\overline{\text{BUSY}}$  is input. Then for this example  $\overline{\text{BUSY}}\text{'A'} = V_{IH}$  and  $\overline{\text{BUSY}}\text{'B'}$  input is shown above.
- All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the port opposite from Port "A".

5668 drw 11

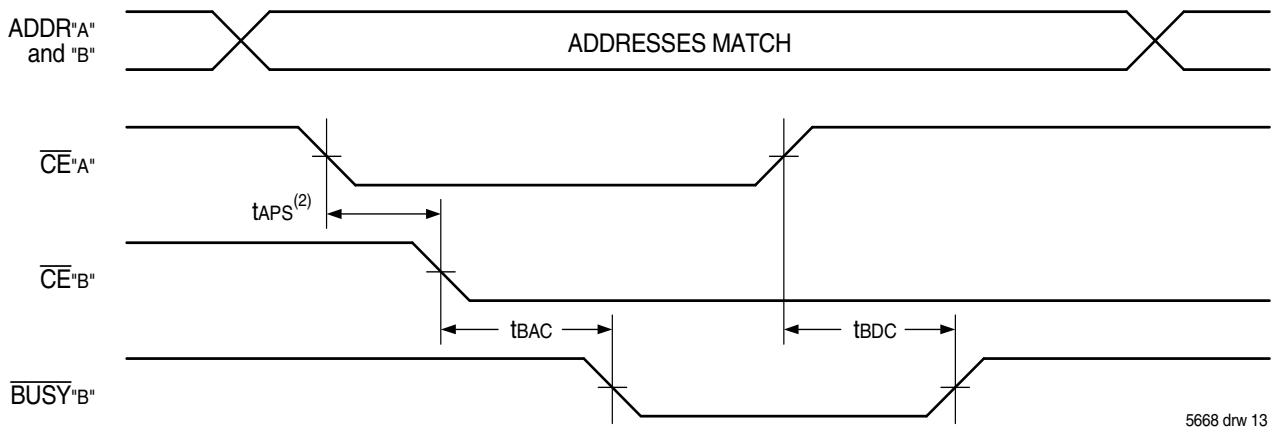
## Timing Waveform of Write with $\overline{\text{BUSY}}$



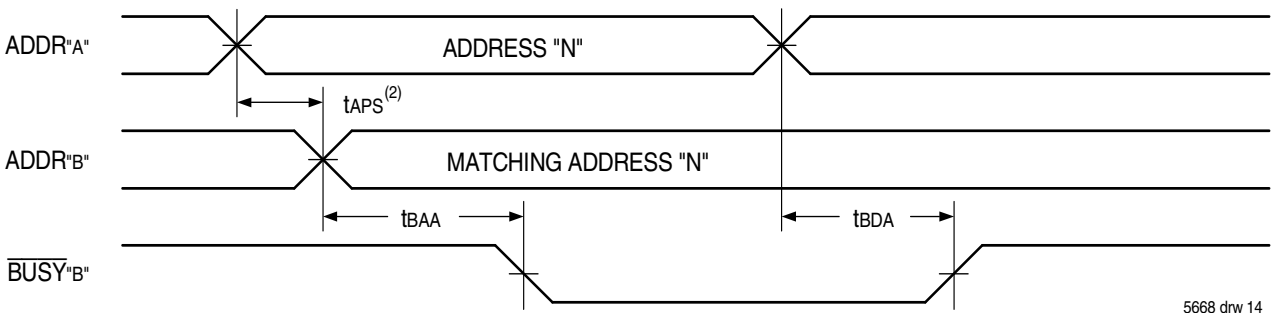
**NOTES:**

1.  $t_{WH}$  must be met for both  $\overline{\text{BUSY}}$  input (slave) output master.
2.  $\overline{\text{BUSY}}$  is asserted on Port "B" Blocking  $R/\overline{W}$ 'B', until  $\overline{\text{BUSY}}$ 'B' goes HIGH.
3.  $t_{WB}$  is only for the slave version.

## Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing<sup>(1)</sup> ( $M/\overline{S} = V_{IH}$ )



## Waveform of $\overline{\text{BUSY}}$ Arbitration Cycle Controlled by Address Match Timing<sup>(1)</sup> ( $M/\overline{S} = V_{IH}$ )



**NOTES:**

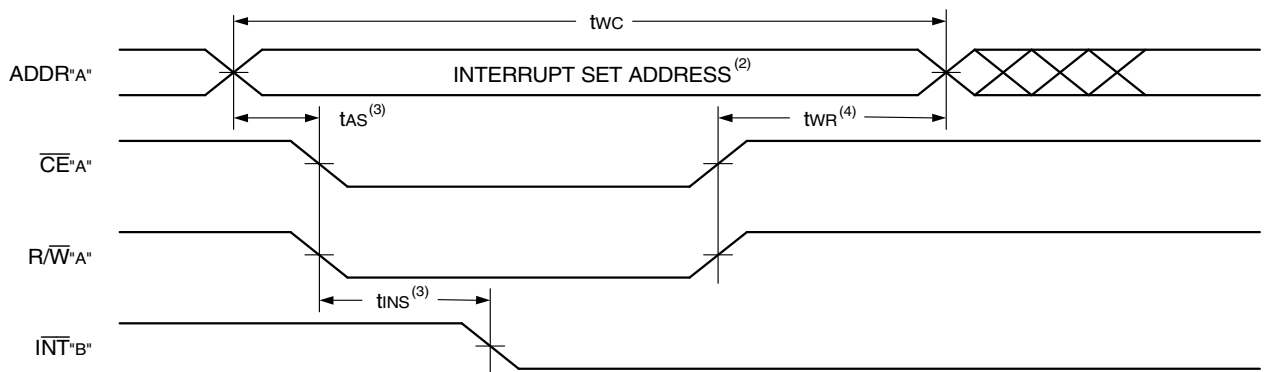
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If  $t_{APS}$  is not satisfied, the  $\overline{\text{BUSY}}$  signal will be asserted on one side or another but there is no guarantee on which side  $\overline{\text{BUSY}}$  will be asserted.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

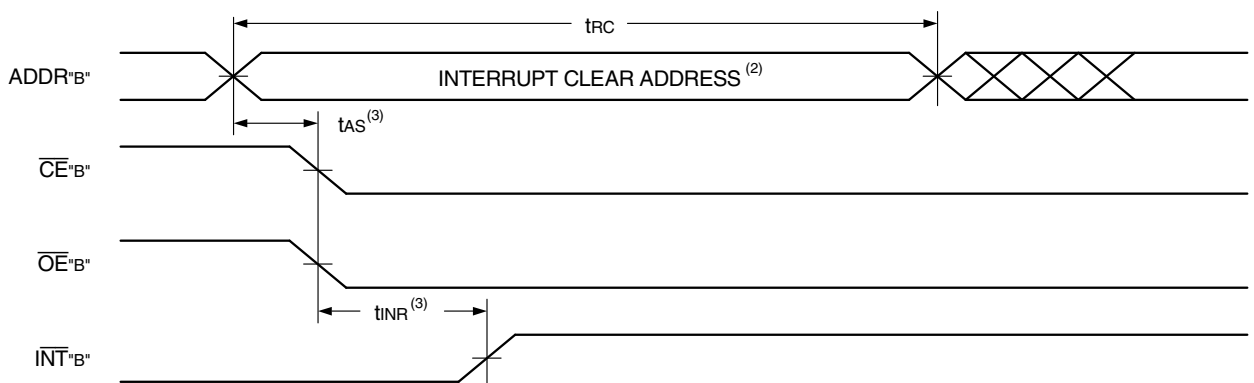
Symbol	Parameter	70T06/5L20 Com'l Only		70T06/5L25 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
<b>INTERRUPT TIMING</b>						
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	ns
t <sub>NS</sub>	Interrupt Set Time	—	20	—	20	ns
t <sub>NR</sub>	Interrupt Reset Time	—	20	—	20	ns

5668 tbl 14

### Waveform of Interrupt Timing<sup>(1)</sup>



5668 drw 15



5668 drw 16

**NOTES:**

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Truth Table III.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

**Truth Table III — Interrupt Flag<sup>(1)</sup>**

Left Port					Right Port					Function
R/WL	$\overline{CE}_L$	$\overline{OE}_L$	A13L-A0L	$\overline{INT}_L$	R/WR	$\overline{CE}_R$	$\overline{OE}_R$	A13R-A0R	$\overline{INT}_R$	
L	L	X	3FFF <sup>(4)</sup>	X	X	X	X	X	L <sup>(2)</sup>	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF <sup>(4)</sup>	H <sup>(3)</sup>	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L <sup>(3)</sup>	L	L	X	3FFE <sup>(4)</sup>	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE <sup>(4)</sup>	H <sup>(2)</sup>	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

**NOTES:**

- Assumes  $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$ .
- If  $\overline{BUSY}_L = V_{IL}$ , then no change.
- If  $\overline{BUSY}_R = V_{IL}$ , then no change.
- A13 is a NC for IDT70T05, therefore Interrupt Addresses are 1FFF and 1FFE.

5668 tbl 15

**Truth Table IV — Address  $\overline{BUSY}$  Arbitration**

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A13L-A0L <sup>(4)</sup> A13R-A0R	$\overline{BUSY}_L$ <sup>(1)</sup>	$\overline{BUSY}_R$ <sup>(1)</sup>	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

**NOTES:**

- Pins  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  are both outputs when the part is configured as a master. Both are inputs when configured as a slave.  $\overline{BUSY}_x$  outputs on the IDT70T06/5 are push pull, not open drain outputs. On slaves the  $\overline{BUSY}_x$  input internally inhibits writes.
- L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either  $\overline{BUSY}_L$  or  $\overline{BUSY}_R = LOW$  will result.  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  outputs cannot be LOW simultaneously.
- Writes to the left port are internally ignored when  $\overline{BUSY}_L$  outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when  $\overline{BUSY}_R$  outputs are driving LOW regardless of actual logic level on the pin.
- A13 is a NC for IDT70T05. Address comparison will be for A0 - A12.

5668 tbl 16

**Truth Table V — Example of Semaphore Procurement Sequence<sup>(1,2,3)</sup>**

Functions	D0 - D7 Left	D0 - D7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

**NOTES:**

- This table denotes a sequence of events for only one of the eight semaphores on the IDT70T06/5.
- There are eight semaphore flags written to via I/O0 and read from all I/O's (I/O0 - I/O7). These eight semaphores are addressed by A0 - A2.
- $\overline{CE} = V_{IH}$ ,  $\overline{SEM} = V_{IL}$  to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

5668 tbl 17

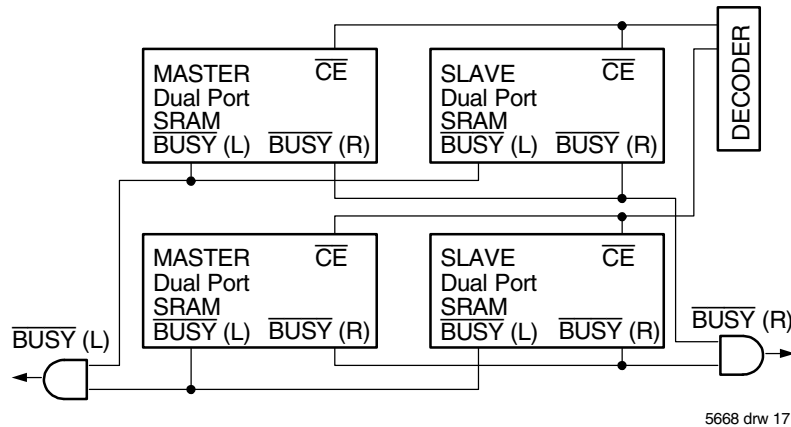


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70T06/5 SRAMs.

## Functional Description

The IDT70T06/5 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70T06/5 has an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{CE} = V_{IH}$ ). When a port is enabled, access to the entire memory array is permitted.

## Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ( $\overline{INTL}$ ) is set when the right port writes to memory location 3FFE (HEX). The left port clears the interrupt by reading address location 3FFE. Likewise, the right port interrupt flag ( $\overline{INTR}$ ) is set when the left port writes to memory location 3FFF (HEX) (1FFE or 1FFF for IDT70T05) and to clear the interrupt flag ( $\overline{INTR}$ ), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF (1FFE or 1FFF for IDT70T05) is user-defined. If the interrupt function is not used, address locations 3FFE and 3FFF (1FFE or 1FFF for IDT70T05) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

## Busy Logic

Busy Logic provides a hardware indication that both ports of the SRAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the SRAM is "busy". The  $\overline{BUSY}$  pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a  $\overline{BUSY}$  indication, the write signal is gated internally to prevent the write from proceeding.

The use of  $\overline{BUSY}$  logic is not required or desirable for all applications. In some cases it may be useful to logically OR the  $\overline{BUSY}$  outputs together and use any  $\overline{BUSY}$  indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of  $\overline{BUSY}$  logic is not desirable, the  $\overline{BUSY}$  logic can be disabled by placing the part in slave mode with the  $\overline{M/\overline{S}}$  pin. Once in slave mode the  $\overline{BUSY}$  pin operates solely as a pin. Normal operation can be programmed by tying the  $\overline{BUSY}$  pins HIGH. If desired, unintended write operations can be prevented to a port

by tying the  $\overline{BUSY}$  pin for that port LOW.

The  $\overline{BUSY}$  outputs on the IDT 70T06/5 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

## Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70T06/5 SRAM array in width while using  $\overline{BUSY}$  logic, one master part is used to decide which side of the SRAM array will receive a  $\overline{BUSY}$  indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the  $\overline{BUSY}$  signal as a write inhibit signal. Thus on the IDT70T06/5 RAM the  $\overline{BUSY}$  pin is an output if the part is used as a master ( $\overline{M/\overline{S}}$  pin =  $V_{IH}$ ), and the  $\overline{BUSY}$  pin is an input if the part used as a slave ( $\overline{M/\overline{S}}$  pin =  $V_{IL}$ ) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating  $\overline{BUSY}$  on one side of the array and another master indicating  $\overline{BUSY}$  on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for part of the other word.

The  $\overline{BUSY}$  arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a  $\overline{BUSY}$  flag to be output from the master before the actual write pulse can be initiated with the  $R/\overline{W}$  signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

## Semaphores

The IDT70T06/5 is an extremely fast Dual-Port 16/8K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port SRAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port SRAM or any other shared

resource.

The Dual-Port SRAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port SRAM. These devices have an automatic power-down feature controlled by  $\overline{CE}$ , the Dual-Port SRAM enable, and  $\overline{SEM}$ , the semaphore enable. The  $\overline{CE}$  and  $\overline{SEM}$  pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where  $\overline{CE}$  and  $\overline{SEM}$  are both HIGH.

Systems which can best use the IDT70T06/5 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70T06/5's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70T06/5 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

## How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port SRAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it assumes control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70T06/5 in a separate memory space from the Dual-Port SRAM. This address space is accessed by placing a LOW input on the  $\overline{SEM}$  pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address,  $\overline{OE}$ , and R/W) as they would be used in accessing a

standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ( $\overline{SEM}$ ) and output enable ( $\overline{OE}$ ) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ( $\overline{SEM}$  or  $\overline{OE}$ ) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no



longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

### Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70T06/5's Dual-Port SRAM. Say the 16K x 8 SRAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port SRAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by

writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port SRAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port SRAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned SRAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

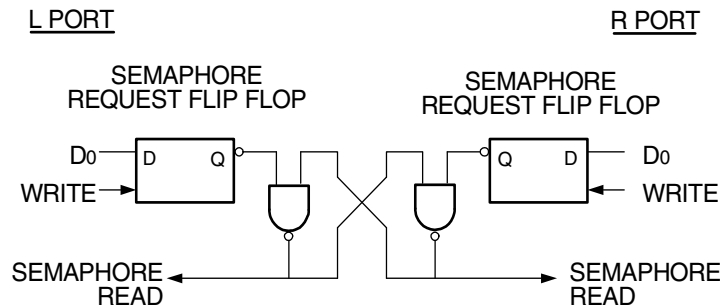
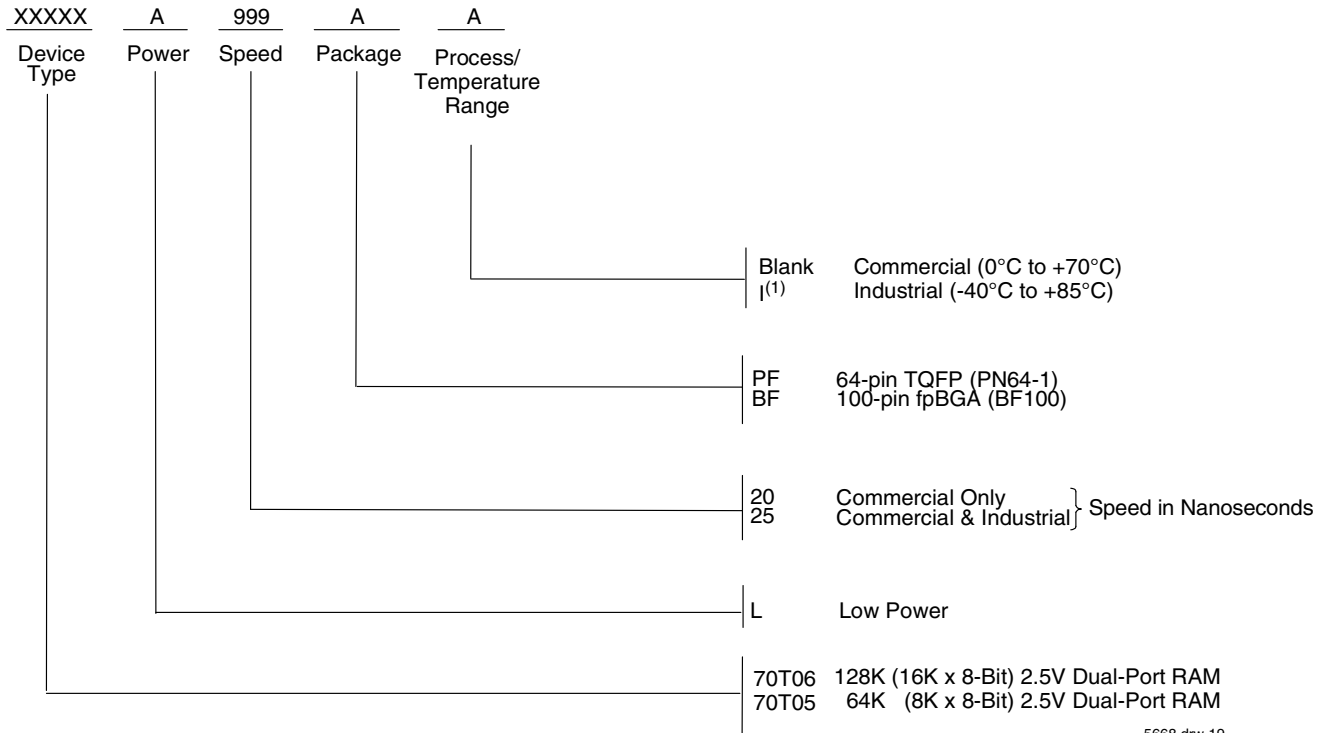


Figure 4. IDT70T06/5 Semaphore Logic

## Ordering Information



5688 drw 19

### NOTE:

- Contact your local sales office for Industrial temp range in other speeds, packages and powers.

## Preliminary Datasheet: Definition

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

## Datasheet Document History

- 08/15/02: Initial Public Release
- 01/29/09: Page 18 Removed "IDT" from orderable part number
- 04/26/09: PDN-F-09-01 issued. See idt.com for PDN specifics
- 03/31/14: 70T06\_05 Datasheet changed to Obsolete Status

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(Rev.1.0 Mar 2020)

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