

HIGH-SPEED 36K (4K x 9-BIT) SYNCHRONOUS PIPELINED **DUAL-PORT SRAM**

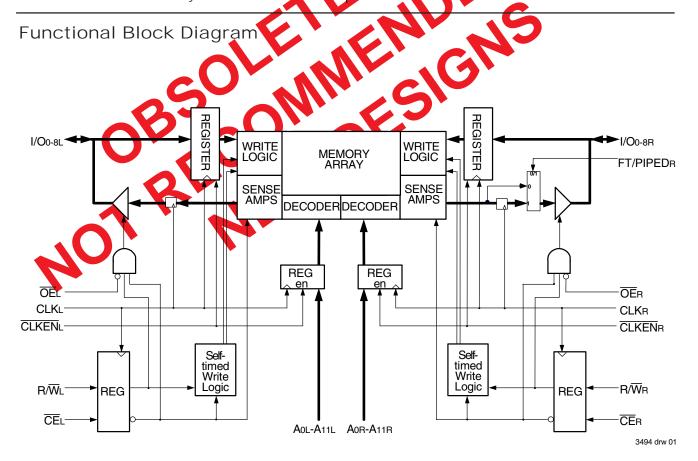
IDT709149S **OBSOLETE PART**

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- Architecture based on Dual-Port SRAM cells
 - Allows full simultaneous access from both ports
- High-speed clock-to-data output times
 - Commercial: 8/10/12ns (max.)
 - Industrial: 10ns (max.)
- Low-power operation
 - IDT709149S Active: 1500mW (typ.) Standby: 75mW (typ.)
- 4K X 9 bits
- 13ns cycle time, 76MHz operation in pipeline mode
 - Self-timed write allows for fast cycle times

- Synchronous operation
 - 4ns setup to clock, 1ns hold on all control, data, and address inputs
 - Data input, address, and control registers
- Fast 8ns clock to data out
 TTL-compatible, single 5V (±10%) powers
- Clock Enable feature
- Guaranteed data output hold times
- incustrial temperature range (-40% to +85°C) is available for selected speeds
- Green parts available, see ordering information



FEBRUARY 2018

Description

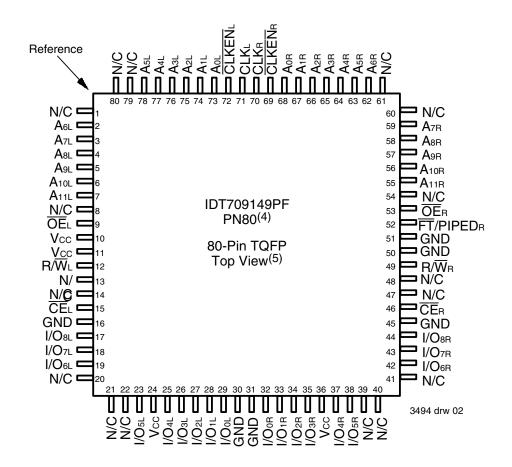
The IDT709149 is a high-speed 4K x 9 bit synchronous Dual-Port SRAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach will allow systems to be designed with very short cycle times. This device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts, by utilizing input data registers.

The IDT709149 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 800mW of power at maximum high-speed clock-to-data output times as fast as 8ns. An automatic power down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT709149 is packaged in an 80-pin TQFP.

Pin Configurations(1,2,3)



NOTES:

- 1. All Vcc pins must be connected to power supply.
- 2. All ground pins must be connected to ground supply.
- 3. Package body is approximately 14mm x 14mm x 1.4mm.
- 4, This package code is used to reference the package diagram.
- 5. This text does not indicate the orientaion of the actual part-marking.

Industrial and Commercial Temperature Ranges

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
VTERM ⁽²⁾	Terminal Voltage	-0.5 to Vcc	٧
TBIAS	Temperature Under Bias	-55 to +125	°C
Tstg	Storage Temperature	-65 to +150	°C
Іоит	DC Output Current	50	mA

NOTES:

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq 20\text{mA}$ for the period of VTERM $\geq Vcc + 10\%$.

Capacitance (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	8	pF
Соит	Output Capacitance	Vout = 3dV	9	pF

NOTES:

- 1. These parameters are determined by device characterization, but are not produc-
- 2. 3dV references the interpolated capacitance when the input and output switch from OV to 3V or from 3V to OV.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES:

1. This is the parameter Ta. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	_	6.0(2)	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	_	0.8	V

3494 tbl 03

- 1. $V_{IL} \ge -1.5V$ for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

	113	<u> </u>			
			709149S		
Symbol	Parameter	Test Conditions	Min.	Мах.	Unit
Iu	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, $Vin = 0V$ to Vcc	-	10	μA
ILO	Output Leakage Current	Vout = 0V to Vcc	-	10	μA
Vol	Output Low Voltage	lol = +4mA	_	0.4	V
Vон	Output High Voltage	IOH = -4mA	2.4	_	V

3494 tbl 04

NOTE:

1. At Vcc ≤ 2.0V, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(4)}$ (Vcc = 5V \pm 10%)

				709149S8 Com'l Only				m'l	7091 Com'	
Symbol	Parameter	Test Condition	Version	Тур.	Max.	Тур.	Max.	Тур.	Max.	Unit
lcc	Dynamic Operating	CEL and CER = VIL,	COM'L	200	320	190	310	180	300	mA
	(Both Ports Active)	Outputs Disabled $f = f_{MAX}^{(1)}$	IND			190	340		_	
ISB1	Standby Current	CEL and CER = VIH	COM'L	100	150	90	150	85	140	mA
	(Both Ports - TTL Level Inputs)	$f = f_{MAX}^{(1)}$	IND			90	175		_	
ISB2	Standby Current	CE"A" = VIL and CE"B" = VIH(3)	COM'L	180	230	170	220	160	210	mA
	(One Port - TTL Level Inputs) Active Port Outputs Disabled, f=fmax ⁽¹⁾		IND			170	250			
ISB3	Full Standby Current (Both Ports - All	CEL and CER > Vcc - 0.2V,	COM'L	5	15	5	15	5	15	mA
	CMOS Level Inputs) $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $f = 0^{(2)}$		IND			5	20		-	
ISB4	Full Standby Current (One Port - All	\overline{CE} "A" $\leq 0.2V$ and	COM'L	170	220	160	210	150	200	mA
	CMOS Level Inputs)	$\begin{array}{l} \overline{\text{CE}_{B^*}} \stackrel{>}{\geq} \text{Vcc} - 0.2 V^{(3)} \\ \text{Vin} \stackrel{>}{\geq} \text{Vcc} - 0.2 \text{V or Vin} \leq 0.2 \text{V} \\ \text{Active Port Outputs Disabled,} \\ f = \text{fmax}^{(1)} \end{array}$	IND			160	240			

3494 tbl 06

- 1. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tclk, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- 2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- 3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 4. Vcc = 5V, TA = 25°C for Typ, and are not production tested. Icc pc = 150mA (Typ).

AC Test Conditions

In	put Pulse Levels	GND to 3.0V
In	put Rise/Fall Times	3ns Max.
In	put Timing Reference Levels	1.5V
0	utput Reference Levels	1.5V
О	output Load	Figures 1,2 and 3

3494 tbl 07

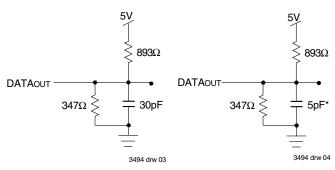


Figure 1. AC Output Test load.

Figure 2. Output Test Load (For tcкLz, tcкнz, toLz, and toнz).
*Including scope and jig.

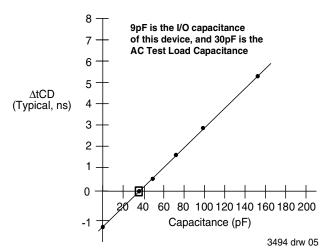


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range— (Read and Write Cycle Timing)

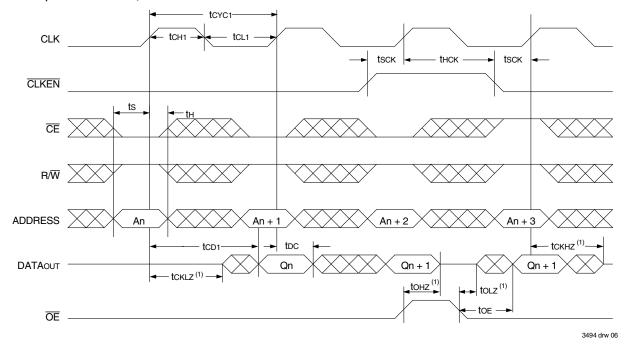
			709149S8 Com'l Only		709149S10 Com'l & Ind		709149S12 Com'l Only	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tcyc1	Clock Cycle Time (Flow-Through)(3)	16	_	20	_	20	_	ns
tcyc2	Clock Cycle Time (Pipelined)(3)	13	_	15	_	16	_	ns
tcH1	Clock High Time (Flow-Through)(3)	6	_	7	_	8	_	ns
tal1	Clock Low Time (Flow-Through) ⁽³⁾	6	_	7	_	8	_	ns
tCH2	Clock High Time (Pipelined) ⁽³⁾	6	_	6	_	6	_	ns
tCL2	Clock Low Time (Pipelined) ⁽³⁾	6		6		6	_	ns
tcD1	Clock to Data Valid (Flow-Through) ⁽³⁾	_	12		15	_	20	ns
tCD2	Clock to Data Valid (Pipelined) ⁽³⁾	_	8		10		12	ns
ts	Registered Signal Set-up Time	4		4		5		ns
tн	Registered Signal Hold Time	1	_	1	_	1	_	ns
toc	Data Output Hold After Clock High	1		1		1		ns
tcklz	Clock High to Output Low-Z ^(1,2)	2		2		2		ns
tckHz	Clock High to Output High-Z ^(1,2)	_	7		7		9	ns
toe	Output Enable to Output Valid	_	8		8		10	ns
tolz	Output Enable to Output Low-Z ^(1,2)	0	_	0		0	_	ns
toнz	Output Disable to Output High-Z ^(1,2)	_	7		7		9	ns
tsck	Clock Enable, Disable Set-Up Time	4		4		5	_	ns
thck	Clock Enable, Disable Hold Time	1		1		1		ns
tcwdd	Write Port Clock High to Read Data Delay	_	25		30		35	ns

3494 tbl 08

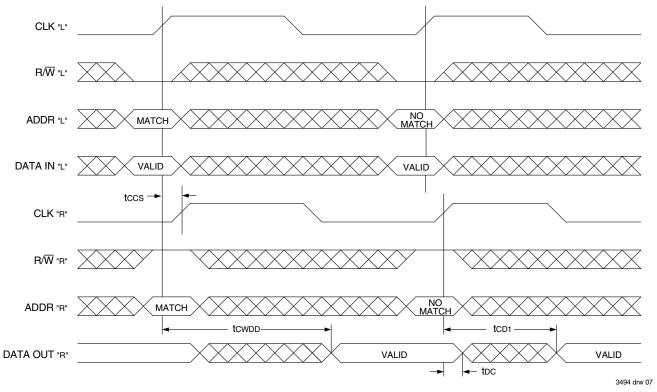
NOTES

- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. This parameter is guaranteed by device characterization, but is not production tested.
- 3. The Pipelined output parameters (tcyc2, tcp2) always apply to the Left Port. The Right Port uses the Pipelined tcyc2 and tcp2 when FT/PIPEDR = VIH and the Flow-Through parameters (tcyc1, tcp1) when FT/PIPEDR = VII.

Timing Waveform of Read Cycle for Flow-Through Output on Right Port ($\overline{\textbf{FT}}$ /PipedR = VIL)



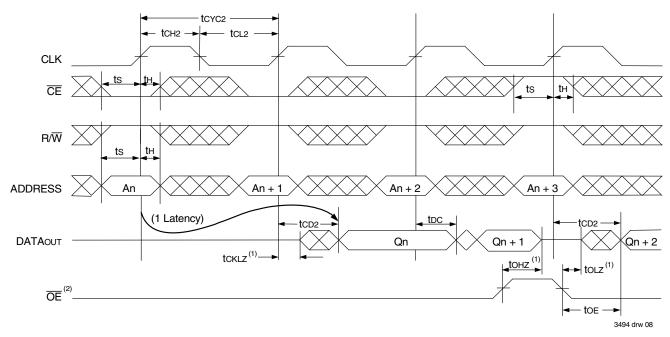
Timing Waveform of Left Port Write to Flow-Through Right Port Read $(\mathbf{FT}/Piped_R = Vil)^{(2,3)}$



NOTES:

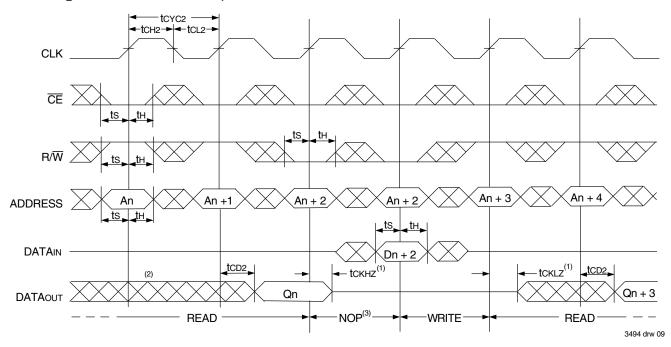
- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. $\overline{CE}L = \overline{CE}R = VIL, \overline{CLKEN}L = \overline{CLKEN}R = VIL$
- 3. \overline{OE} = VIL for the reading port, port 'R'.

Timing Waveform of Read Cycle for Pipelined Operation (Left Port; Right Port when $\overline{\bf FT}$ /Piped_R = VIH)⁽³⁾

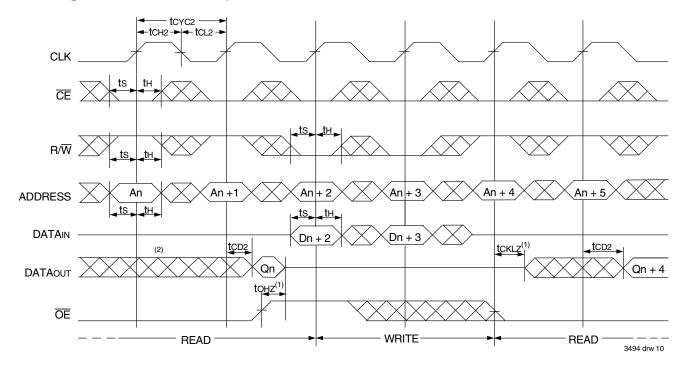


- 1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
- 2. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
- 3. CLKENL and CLKENR = VIL.

Timing Waveform of Pipelined Read-to-Write-to-Read (**OE** = VIL)



Timing Waveform of Pipelined Read-to-Write-to-Read (**OE** Controlled)



NOTES:

- $1. \quad Transition is measured 0 mV from Low or High-impedance voltage with the Output Test Load (Figure 2).$
- 2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- 3. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Functional Description

The IDT709149 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent only on the low to high transitions of the clock signal to initiate a write allowing the shortest

possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the $\overline{\text{CE}}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

When piplelined mode is enabled, two cycles are required with $\overline{\text{CE}}$ LOW to reactivate the outputs.

Truth Table I: Read/Write Control(1)

Inputs		Outputs			
Sy	Synchronous ⁽³⁾ Asynchronous				
CLK	CLK CE R/W OE		I/O ₀₋₈	Mode	
1	Н	Χ	Х	High-Z	Deselected—Power Down
1	L	L	Х	DATAIN	Selected and Write Enable
1	L	Н	L	DATAout	Read Selected and Data Output Enabled Read (1 Latency)
1	Х	Χ	Н	High-Z	Data I/O Disabled

3494 tbl 09

Truth Table II: Clock Enable Function Table (1)

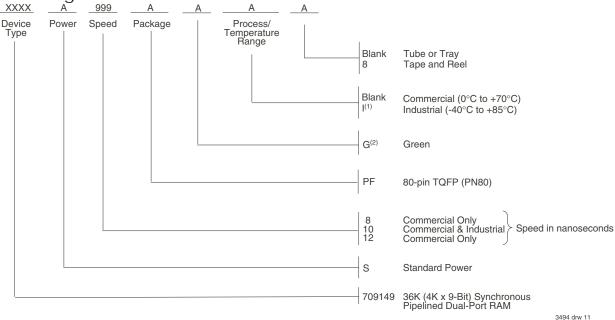
	Inp	outs	Registe	r Inputs	Register Outputs ⁽⁴⁾		
Operating Mode	CLK ⁽³⁾	CLKEN ⁽²⁾	ADDR	DATAIN	ADDR	DATAout	
Load "1"	1	L	Н	Н	Н	Н	
Load "0"	1	Ĺ	L	Ĺ	Ĺ	L	
Hold (do nothing)	↑	Н	Х	Х	NC	NC	
	Х	Н	Х	Х	NC	NC	

NOTES

3494 tbl 10

- 1. 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
- 2. CLKEN = VIL must be clocked in during Power-Up.
- 3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/W and $\overline{\text{CE}}$ are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transition of the CLK.
- 4. The register outputs are internal signals from the register inputs being clocked in or disabled by CLKEN.

Ordering Information



NOTES:

- 1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office. LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

3/8/99: Initiated datasheet document history

Converted to new format

Cosmetic and typographical corrections Added additional notes to pin configurations

6/3/99: Changed drawing format 9/1/99: Removed Preliminary 11/10/99: Replaced IDT logo

5/24/00: Page 3 Increased storage temperature parameter

Clarified Taparameter

Page 5 DC Electrical parameters—changed wording from "open" to "disabled"

Changed ±200mV to 0mV in notes

01/24/02: Page 2 Added date revision for pin configuration

Page 3, 4 & 5 Removed Industrial temp footnote from all tables

Page 4 Added Industrial temp to 10ns speed in the column heading and values of DC Electrical Characteristics

Page 5 Corrected a typo in the column heading of AC Electrical Characteristics

Page 5 Added Industrial temp to 10ns speed in the column heading of AC Electrical Characteristics

Page 10 Added Industrial temp to 10ns offering in ordering information

Pages 1& 10 Replaced TM logo with ® logo

01/29/09: Page 10 Removed "IDT" from orderable part number 04/08/15: Page 2 Removed IDT in reference to fabrication

Page 2 &10 The package code PN80-1 changed to PN80 to match standard package codes Page 4 Corrected typo in the Typical Output Derating(Lumped Capitive Load) diagram

02/02/18: Page 10 Added Tape and Reel and Green indicators with their footnote annotations to the Ordering Information

Product Discontinuation Notice - PDN# SP-17-02

Last time buy expires June 15, 2018

03/05/20: 709149 Datasheet changed to Obsolete Status



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