

## HIGH-SPEED 16K X 16 DUAL-PORT STATIC RAM

#### **Features**

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - Commercial: 15/20/25/35ns (max.)
  - Industrial: 20ns (max.)
  - Military: 25/35ns (max.)
- Low-power operation
  - IDT7026S

Active: 750mW (typ.) Standby: 5mW (typ.)

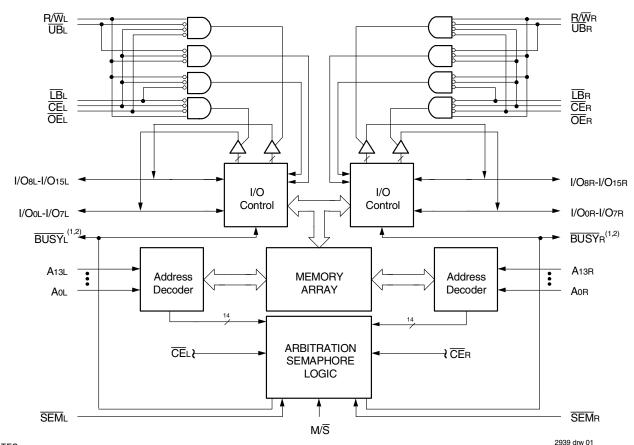
- IDT7026L

Active: 750mW (typ.) Standby: 1mW (typ.)

 Separate upper-byte and lower-byte control for multiplexed bus compatibility

- IDT7026 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/S = H for BUSY output flag on Master,
   M/S = L for BUSY input on Slave
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- ◆ TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA and 84-pin PLCC
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Green parts available, see ordering information

## Functional Block Diagram



#### NOTES:

- 1. (MASTER):  $\overline{\text{BUSY}}$  is output; (SLAVE):  $\overline{\text{BUSY}}$  is input.
- 2. BUSY outputs are non-tri-stated push-pull.

AUGUST 2019



Military, Industrial and Commercial Temperature Ranges

## Description

The IDT7026 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT7026 is designed to be used as a stand-alone Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

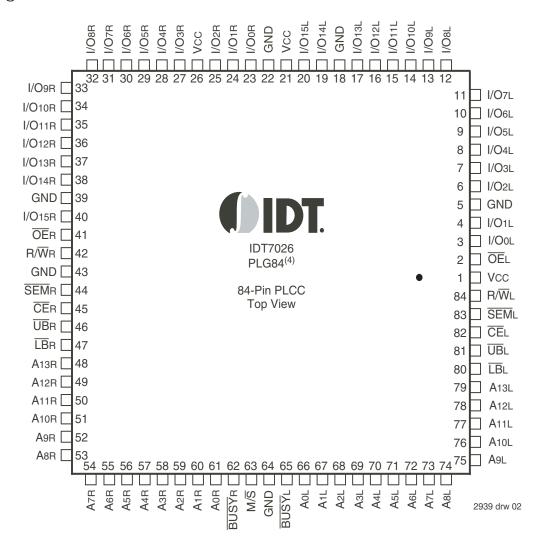
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down

feature controlled by  $\overline{\text{CE}}$  permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7026 is packaged in a ceramic 84-pin PGA, and a 84-pin PLCC. Military grade product is manufactured in compliance with MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

# Pin Configurations (1,2,3)



- 1. All Vcc pins must be connected to the power supply.
- 2. All GND pins must be connected to the ground supply.
- 3. Package body is approximately 1.15 in x 1.15 in x .17 in.
- 4. This package code is used to reference the package diagram.

# Pin Configurations (1,2,3) (con't.)

	63	61	60	58	55	54	51	48	46	45	42
11	I/O7L	I/O <sub>5</sub> L	I/O4L	I/O <sub>2</sub> L	I/OoL	ŌĒL	SEML	ŪB∟	A12L	A11L	A8L
	66	64	62	59	56	49	50	47	44	43	40
10	I/O10L	I/O8L	I/O6L	I/O3L	I/O1L	ŪB∟	CEL	A13L	A10L	A9L	A6L
	67	65			57	53	52			41	39
09	I/O11L	I/O9L			GND	Vcc	R/WL			A7L	A <sub>5</sub> L
	69	68						ı		38	37
80	I/O13L	I/O12L									Азь
	72	71	73				33	35	34		
07	I/O15L	I/O14L	Vcc			BUSYL	A1L	AoL			
	75	70	74			IDT7026 GU84 <sup>(4)</sup>	32	31	36		
06	06 I/OoR GND GND 84-Pin PGA						GND	M/S	A <sub>2</sub> L		
	76	77	78		٦	Top View	28	29	30		
05	I/O1R	I/O2R	Vcc						A1R	Aor	BUSYR
	79	80								26	27
04	I/O3R	I/O4R								<b>A</b> 3R	A <sub>2</sub> R
	81	83	1		7	11	12	]		23	25
03	I/O5R	I/O7R			GND	GND	SEMR			A6R	A4R
	82	1	2	5	8	10	14	17	20	22	24
02	I/O6R	I/O9R	I/O10R	I/O13R	I/O15R	R/WR	<del>UB</del> R	A12R	A9R	A7R	<b>A</b> 5R
	84	3	4	6	9	15	13	16	18	19	21
01	I/O8R	I/O11R	I/O12R	I/O14R	ŌĒR	LBR	CER	A13R	A11R	A10R	A8R
	A	В	С	D	E	F	G	Н	J	K	L
Index											2939 drw 0

#### NOTES:

- 1. All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- 3. Package body is approximately 1.12 in x 1.12 in x .16 in.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking.

### Pin Names

Left Port	Right Port	Names			
CEL	CER	Chip Enable			
$R/\overline{W}_L$	R/WR	Read/Write Enable			
ŌĒL	<del>OE</del> R	Output Enable			
A0L - A13L	A0R - A13R	Address			
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output			
SEML	SEM <sub>R</sub>	Semaphore Enable			
ŪB∟	<del>UB</del> R	Upper Byte Select			
<u>LB</u> ∟	<del>LB</del> R	Lower Byte Select			
BUSYL	BUSYR	Busy Flag			
N	/S	Master or Slave Select			
V	CC	Power			
G	ND	Ground			

2939 tbl 01

# Maximum Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to+125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

NOTES: 2939 tbl 02a

1. This is the parameter Ta. This is the "instant on" case temperature.

# Capacitance<sup>(1)</sup> (TA = +25°C, f = 1.0mhz)

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
Cin	Input Capacitance	VIN = 3dV	9	pF
Соит	Output Capacitance	Vout = 3dV	10	pF

NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Truth Table I - Non-Contention Read/Write Control

		Inpu	uts <sup>(1)</sup>			Out	puts	
CE	R/₩	ŌĒ	ŪB	ĪΒ	SEM	I/O <sub>8-15</sub>	I/O <sub>0-7</sub>	Mode
Н	Х	Х	Χ	Х	Н	High-Z	High-Z	Deselected: Power-Down
Х	Х	Х	Н	Н	Н	High-Z	High-Z	Both Bytes Deselected
L	L	Х	L	Н	Н	DATAIN	High-Z	Write to Upper Byte Only
L	L	Х	Н	L	Н	High-Z	DATAIN	Write to Lower Byte Only
L	L	Х	L	L	Н	DATAIN	DATAIN	Write to Both Bytes
L	Н	L	L	Н	Н	DATAout	High-Z	Read Upper Byte Only
L	Н	L	Н	L	Н	High-Z	DATAout	Read Lower Byte Only
L	Н	L	L	L	Н	DATAout	DATAout	Read Both Bytes
Х	Х	Н	Х	Х	Х	High-Z	High-Z	Outputs Disabled

2939 tbl 04

NOTE:

1. A0L — A13L  $\neq$  A0R — A13R.

Truth Table II - Semaphore Read/Write Control(1)

	1 4 6 1 6		0111010		100.0.7			-
		Inp	uts			Out	puts	
CΕ	R/W	Œ	ŪB	ĽΒ	SEM	I/O8-15	I/O <sub>0-7</sub>	Mode
Н	Н	L	Х	Χ	L	DATAout	DATAout	Read Data in Semaphore Flag
Χ	Н	L	Н	Н	L	DATAout	DATAout	Read Data in Semaphore Flag
Н	<b>↑</b>	Χ	Χ	Χ	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
Χ	<b>↑</b>	Χ	Н	Н	L	DATAIN	DATAIN	Write I/Oo into Semaphore Flag
L	Х	Х	L	Χ	L			Not Allowed
L	Χ	Χ	Χ	L	L			Not Allowed

2939 tbl 05

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
Tstg	Storage Temperature	-55 to +125	-65 to +150	٥C
Іоит	DC Output Current	50	50	mA

2939 tbl 06a

#### NOTES

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

<sup>1.</sup> There are eight semaphore flags written to via I/Oo and read from all I/O's (I/Oo-I/O15). These eight semaphores are addressed by Ao - A2.

2939 tbl 08

#### 7026S/L High-Speed 16K x 16 Dual-Port Static RAM

# Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V⊪	Input High Voltage	2.2	_	6.0(2)	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	_	0.8	V

2939 tbl

- NOTES:
- 1.  $V_{IL} \ge -1.5V$  for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 10%.

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

			7026S		702		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
Iu	Input Leakage Current <sup>(1)</sup>	Vcc = 5.5V, $Vin = 0V$ to $Vcc$	-	10	-	5	μΑ
<b>I</b> LO	Output Leakage Current	$\overline{CE}$ = ViH, Vout = 0V to Vcc	I	10	I	5	μΑ
Vol	Output Low Voltage	Iol = 4mA	-	0.4	-	0.4	V
Voh	Output High Voltage	IOH = -4mA	2.4	-	2.4	-	V

NOTE:

1. At Vcc = 2.0V, input leakages are undefined.

### **AC Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

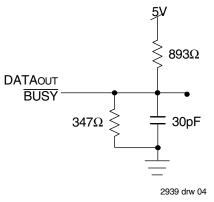


Figure 1. AC Output Test Load

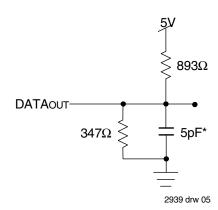


Figure 2. Output Test Load (for tLz, tHz, twz, tow) \* Including scope and jig.



# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(1)}$ (con't.) (Vcc = 5.0V $\pm$ 10%)

					7026X15 Com'l Only		7026X20 Com'l, Ind & Military.		7026X25 Com'l, Ind & Military		
Symbol	Parameter	Test Condition	Version	on	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	<u>CE</u> = VL, Outputs Disabled <u>SEM</u> = VH	COM'L	S L	190 190	325 285	180 180	315 275	170 170	305 265	mA
		$f = fMAX^{(3)}$	MIL & IND	S L	_		180 180	355 315	5 170 305 5 170 265 170 345 5 170 305 5 25 85 0 25 60 0 25 100 0 25 100 0 105 200 105 230 0 105 200 105 200 105 170		
ISB1	Standby Current (Both Ports - TTL Level	CEL = CER = VIH SEMR = SEML = VIH	COM'L	S L	35 35	95 70	30 30	85 60			mA
	Inputs)	$f = fMAX^{(3)}$	MIL & IND	S L	_	-         -         30         80         25					
ISB2	Standby Current (One Port - TTL Level Inputs)		COM'L	S L	125 125	220 190	115 115	210 180			mA
		$\frac{f = f MAX^{(3)}}{SEMR} = \overline{SEM}L = VIH$	MIL & IND	S L	_	_	115 115	245 210		Max. 305 265 345 305 85 60 100 80 200 170 230 200 15	
ISB3	Full Standby Current (Both Ports - All CMOS Level	Both Ports $\overline{CE}L$ and $\overline{CER} \ge VCC - 0.2V$ VIN > VCC - 0.2V or	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2		mA
	Inputs)	$VIN \ge VCC - 0.2V$ of $VIN \le 0.2V$ , $f = 0^{(4)}$ SEMR = SEML $\ge VCC - 0.2V$	MIL & IND	S L	_		1.0 0.2	30 10	1.0 0.2	230 200 15 5 30 10	
ISB4	Full Standby Current (One Port - All CMOS Level	$\overline{CE}^*A^* \le 0.2V$ and $\overline{CE}^*B^* \ge VCC - 0.2V^{(5)}$	COM'L	S L	120 120	195 170	110 110	185 160	100 100		mA
	Inputs)		MIL & IND	S L	_	_	110 110	210 185	100 100		

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					7026X35 Com'l, Ind & Military		7026X55 Com'l, Ind & Military		
Symbol	Parameter	Test Condition	Version		Typ. <sup>(2)</sup>	Max.	Typ. <sup>(2)</sup>	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CE = VIL, Outputs Disabled SEM = VIH f = f(MAX <sup>(8)</sup>	COM'L	S L	160 160	295 255	150 150	270 230	mA
	(Bour Poils Active)	CEL = CER = VIH SEMR = SEML = VIH	MIL & IND	S L	160 160	335 295	150 150	310 270	
ISB1	Standby Current (Both Ports - TTL Level	SEMR = SEML = VIH	COM'L	S L	20 20	85 60	13 13	85 60	mA
	inputs) $f = f_{MAX}^{(3)}$	T = IMAX <sup>©</sup> /	MIL & IND	S L	20 20	100 80	13 13	100 80	
ISB2	Standby Current (One Port - TTL Level Inputs)	CE'A" = VIL and CE'B" = VIH <sup>(5)</sup> Active Port Outputs Disabled, f=fMaX <sup>(5)</sup>	COM'L	S L	95 95	185 155	85 85	165 135	mA
	mpus)	SEMR = SEML = VIH	Wersion         Typ. (a)         Max.         Typ. (a)         Max.         Typ. (a)         Max.         Typ. (a)         Max.         Unit of the property of the pr						
ISB3	Full Standby Current (Both Ports - All CMOS	Both Ports CEL and CER > VCC - 0.2V	COM'L	S L					mA
	Level Inputs) $ \begin{array}{c} V_{IN} \geq V_{CC} - 0.2V \text{ or} \\ V_{IN} \leq 0.2V,  f = 0^{(4)} \\ \overline{\text{SEMR}} = \overline{\text{SEML}} \geq V_{CC} - 0.2V \\ \end{array} $	$VIN < 0.2V$ . $f = 0^{(4)}$							
ISB4	Full Standby Current (One Port - All CMOS	<u>CE</u> "A" ≤ 0.2V and <u>CE"B" ≥ VCC</u> - 0.2V <sup>(5)</sup>	COM'L						mA
	Level Inputs)			S L					

### NOTES:

- 1. 'X' in part numbers indicates power rating (S or L).
- X in part infinites shower fating (3 of E).
   Vcc = 5V, Ta = +25°C, and are not production tested. Iccpc = 120mA (Typ.)
   At f = fMax, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
   f = 0 means no address or control lines change.



## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(4)</sup>

		7026X15 Com'l Only		7026X20 Com'l, Ind & Military		7026X25 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
trc	Read Cycle Time	15		20	_	25		ns
taa	Address Access Time	_	15		20	_	25	ns
tace	Chip Enable Access Time <sup>(3)</sup>	_	15		20	_	25	ns
tabe	Byte Enable Access Time <sup>(3)</sup>	_	15		20	_	25	ns
taoe	Output Enable Access Time	_	10		12	_	13	ns
tон	Output Hold from Address Change	3	_	3	_	3		ns
tLz	Output Low-Z Time <sup>(1,2)</sup>	3	_	3	_	3		ns
tHZ	Output High-Z Time <sup>(1,2)</sup>		10	_	12	_	15	ns
tpu	Chip Enable to Power Up Time (2)	0	_	0	_	0	_	ns
tPD	Chip Disable to Power Down Time <sup>(2)</sup>		15		20		25	ns
tsop	Semaphore Flag Update Pulse (OE or SEM)	10	_	10	_	12		ns
tsaa	Semaphore Address Access Time		15	_	20		25	ns

2939 tbl 12a

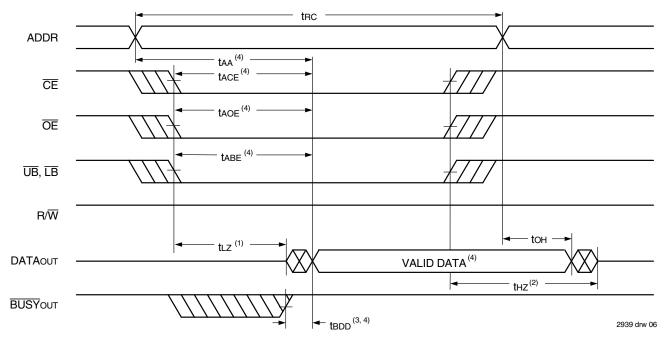
			7026X35 Com'l, Ind & Military		7026X55 Com'l, Ind & Military	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
READ CYCLE						
trc	Read Cycle Time	35		55		ns
taa	Address Access Time		35	_	55	ns
tace	Chip Enable Access Time <sup>(3)</sup>		35	_	55	ns
tabe	Byte Enable Access Time <sup>(3)</sup>		35	_	55	ns
taoe	Output Enable Access Time		20	_	30	ns
tон	Output Hold from Address Change	3		3		ns
tlz	Output Low-Z Time <sup>(1,2)</sup>	3		3		ns
tHZ	Output High-Z Time <sup>(1,2)</sup>		15	_	25	ns
tpu	Chip Enable to Power Up Time (2)	0		0		ns
tpp	Chip Disable to Power Down Time <sup>(2)</sup>		35	_	50	ns
tsop	Semaphore Flag Update Pulse (OE or SEM)	15		15		ns
tsaa	Semaphore Address Access Time	_	35		55	ns

- Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
   This parameter is guaranteed by device characterization, but is not production tested.
   To access RAM, E = VIL and SEM = VIH. To access semaphore, E = VIH and SEM = VIL.

- 4. 'X' in part numbers indicates power rating (S or L).



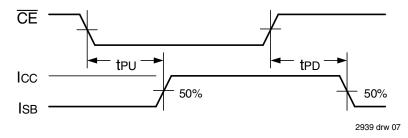
## WAVEFORM OF READ CYCLES(5)



#### NOTES:

- 1. Timing depends on which signal is asserted last,  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ .
- 2. Timing depends on which signal is de-asserted first  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ .
- 3. tedd delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
- 4. Start of valid data depends on which timing becomes effective last taoe, tace, taa or tBDD.
- 5.  $\overline{SEM} = VIH.$

## Timing of Power-Up Power-Down





# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(5,6)</sup>

Symbol	Parameter	7026X15 Com'l Only		7026X20 Com'l, Ind & Military		7026X25 Com'l, Ind & Military		
		Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
twc	Write Cycle Time	15	_	20	_	25	_	ns
tew	Chip Enable to End-of-Write <sup>(3)</sup>	12	_	15	_	20		ns
taw	Address Valid to End-of-Write	12	_	15	_	20		ns
tas	Address Set-up Time <sup>(3)</sup>	0	_	0	_	0	_	ns
twp	Write Pulse Width	12	_	15	_	20	_	ns
twr	Write Recovery Time	0		0	_	0	_	ns
tow	Data Valid to End-of-Write	10	_	15	_	15		ns
tHZ	Output High-Z Time <sup>(1,2)</sup>	_	10		12	_	15	ns
tDH	Data Hold Time <sup>(4)</sup>	0	_	0	_	0		ns
twz	Write Enable to Output in High-Z <sup>(1,2)</sup>		10		12	_	15	ns
tow	Output Active from End-of-Write <sup>(1,2,4)</sup>	0	_	0	_	0	_	ns
tswrd	SEM Flag Write to Read Time	5	_	5	_	5	_	ns
tsps	SEM Flag Contention Window	5	_	5	_	5		ns

3199 tbl 13a

Symbol	Parameter	7026X35 Com'l, Ind & Military		7026X55 Com'l, Ind & Military			
		Min.	Max.	Min.	Max.	Unit	
WRITE CYCLE	=						
twc	Write Cycle Time	35	_	55	_	ns	
tew	Chip Enable to End-of-Write <sup>(3)</sup>	30	_	45	_	ns	
taw	Address Valid to End-of-Write	30		45		ns	
tas	Address Set-up Time <sup>(3)</sup>	0	_	0	_	ns	
twp	Write Pulse Width	25	_	40	_	ns	
twr	Write Recovery Time	0	_	0	_	ns	
tow	Data Valid to End-of-Write	15	_	30		ns	
tHZ	Output High-Z Time <sup>(1,2)</sup>	_	15	_	25	ns	
tон	Data Hold Time <sup>(4)</sup>	0	_	0		ns	
twz	Write Enable to Output in High-Z <sup>(1,2)</sup>	_	15	_	25	ns	
tow	Output Active from End-of-Write <sup>(1,2,4)</sup>	0	_	0		ns	
tswrd	SEM Flag Write to Read Time	5	_	5	_	ns	
tsps	SEM Flag Contention Window	5	_	5	_	ns	

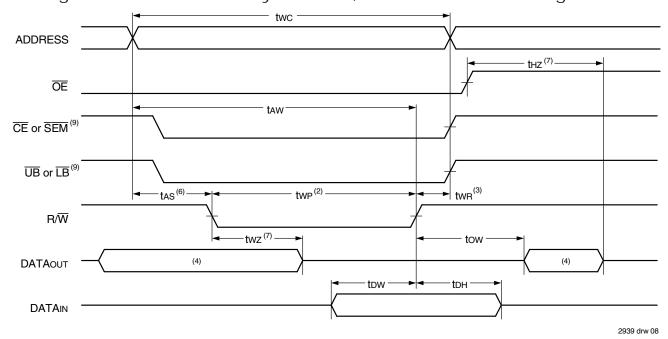
#### NOTES:

2939 tbl 13b

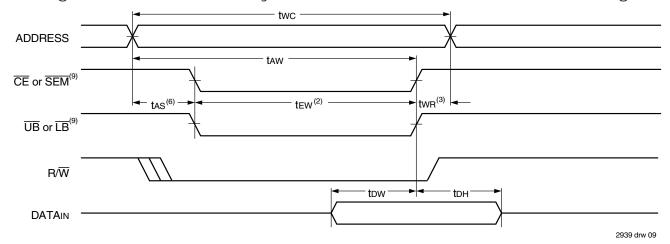
- 1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
- This parameter is guaranteed by device characterization, but is not production tested.
   To access RAM, CE = VIL and SEM = VIH. To access semaphore, CE = VIH and SEM = VIL. Either condition must be valid for the entire tew time.
- 4. The specification for ton must be met by the device supplying write data to the RAM under all operating conditions. Although ton and tow values will vary over voltage and temperature, the actual toH will always be smaller than the actual tow.
- 5. 'X' in part numbers indicates power rating (S or L).



# Timing Waveform of Write Cycle No. 1, R/W Controlled Timing (1,5,8)



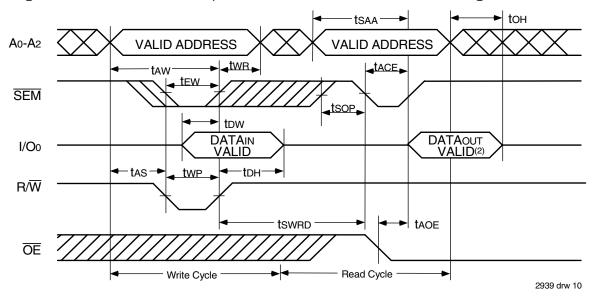
# Timing Waveform of Write Cycle No. 2, CE, UB, LB Controlled Timing(1,5)



- 1. R/ $\overline{W}$  or  $\overline{CE}$  or  $\overline{UB}$  and  $\overline{LB}$  = VIH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of a  $\underline{VlL}$   $\overline{CE} = \underline{VlL}$  and  $R\overline{NW} = VlL$  for memory array writing cycle.
- 3. two is measured from the earlier of  $\overline{\text{CE}}$  or  $R/\overline{W}$  (or  $\overline{\text{SEM}}$  or  $R/\overline{W}$ ) going ViH to the end of write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the  $\overline{\text{CE}}$  or  $\overline{\text{SEM}}$  = V<sub>IL</sub> transition occurs simultaneously with or after the  $\overline{\text{R/W}}$  = V<sub>IL</sub> transition, the outputs remain in the High-impedance state.
- 6. Timing depends on which enable signal is asserted last,  $\overline{\text{CE}}$  or  $R/\overline{W}$ .
- 7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
- 8. If  $\overline{OE} = VIL$  during  $R\overline{W}$  controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If  $\overline{OE} = VIH$  during an  $R\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 9. To access RAM,  $\overline{\text{CE}} = \text{VIL}$  and  $\overline{\text{SEM}} = \text{VII}$ . To access semaphore,  $\overline{\text{CE}} = \text{VII}$  and  $\overline{\text{SEM}} = \text{VIL}$ . Lew must be met for either condition.



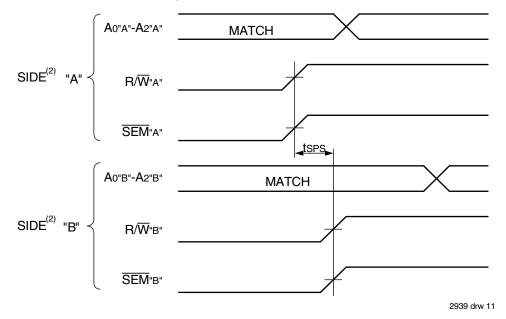
Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



#### NOTES

- 1.  $\overline{CE} = V_{IH}$  or  $\overline{UB}$  and  $\overline{LB} = V_{IH}$  for the duration of the above timing (both write and read cycle).
- 2. "DATAout VALID" represents all I/O's (I/Oo-I/O15) equal to the semaphore value.

# Timing Waveform of Semaphore Write Contention<sup>(1,3,4)</sup>



- 1. Dor = Dol = Vil,  $\overline{CE}R = \overline{CE}L = VIH$ , or both  $\overline{UB} \& \overline{LB} = VIH$ .
- 2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 3. This parameter is measured from  $R\overline{W}^a$  or  $\overline{SEM}^a$  going HIGH to  $R/\overline{W}^a$  or  $\overline{SEM}^a$  going HIGH.
- 4. If tsps is not satisfied, there is no guarantee which side will be granted the semaphore flag.



# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(6,7)}$

		7026X15 Com'l Only		Com	6X20 I, Ind litary	7026X25 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
BUSY TIMING	(M/S=VIH)							
tbaa	BUSY Access Time from Address Match		15		20		20	ns
tBDA	BUSY Disable Time from Address Not Matched		15		20		20	ns
<b>t</b> BAC	BUSY Access Time from Chip Enable Low		15		20		20	ns
tBDC	BUSY Access Time from Chip Enable High		15		17		17	ns
taps	Arbitration Priority Set-up Time <sup>(2)</sup>	5		5		5		ns
tBDD	BUSY Disable to Valid Data	_	18	_	30	_	30	ns
twн	Write Hold After BUSY <sup>(5)</sup>	12	_	15		17		ns
<b>BUSY</b> TIMING	(M/S=VIL)							
twB	BUSY Input to Write <sup>(4)</sup>	0		0		0		ns
twн	Write Hold After BUSY <sup>5)</sup>	12		15	_	17		ns
PORT-TO-POR	T DELAY TIMING							
twdd	Write Pulse to Data Delay <sup>(1)</sup>	_	30	_	45	_	50	ns
todo	Write Data Valid to Read Data Delay <sup>(1)</sup>		25		30		35	ns

2939 tbl 14a

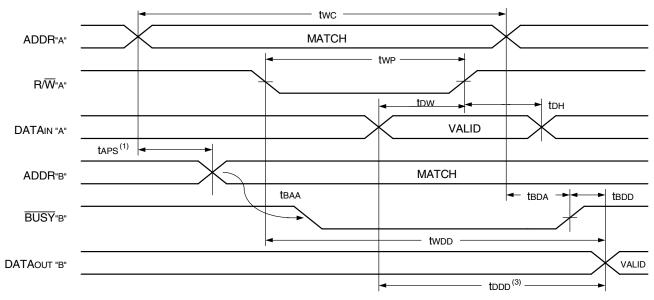
			7026X35 Com'l, Ind & Military		7026X55 Com'l, Ind & Military	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
BUSY TIMING	G (M/S=Vih)					
tbaa	BUSY Access Time from Address Match		20		45	ns
tbda	BUSY Disable Time from Address Not Matched	_	20	_	40	ns
tbac	BUSY Access Time from Chip Enable Low	_	20	_	40	ns
tbdc	BUSY Access Time from Chip Enable High	_	20	_	35	ns
taps	Arbitration Priority Set-up Time <sup>(2)</sup>	5	_	5		ns
tbdd	BUSY Disable to Valid Data <sup>(3)</sup>		35		40	ns
twн	Write Hold After BUSY <sup>(5)</sup>	25	_	25		ns
BUSY TIMING	G (M/S=VIL)					
twB	BUSY Input to Write <sup>(4)</sup>	0	_	0	_	ns
twн	Write Hold After BUSY <sup>(5)</sup>	25	_	25		ns
PORT-TO-PO	RT DELAY TIMING					
twdd	Write Pulse to Data Delay <sup>(1)</sup>		60		80	ns
todd	Write Data Valid to Read Data Delay <sup>(1)</sup>		45		65	ns

#### NOTES:

2939 tbl 14b

- 1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY (M/S = VIH)".
- 2. To ensure that the earlier of the two ports wins.
- 3. tbdd is a calculated parameter and is the greater of 0, twdd twp (actual), or tddd tdw (actual).
- 4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
- 5. To ensure that a write cycle is completed on port "B" after contention on port "A".
- 6. 'X' in part numbers indicates power rating (S or L).
- 7. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write with Port-to-Port Read and **BUSY** (M/**S** = VIH)<sup>(2,4,5)</sup>

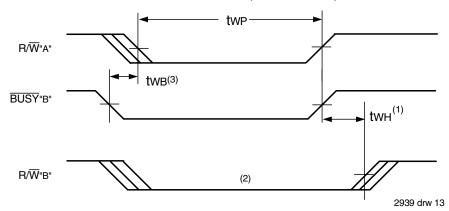


NOTES:

2939 drw 12

- 1. To ensure that the earlier of the two ports wins. taps is ignored for  $M/\overline{S} = V_{IL}$  (slave).
- $2. \quad \overline{CE}_L = \overline{CE}_R = V_{IL}.$
- 3.  $\overline{OE} = V_{IL}$  for the reading port.
- 4. If  $M/\overline{S} = V_{IL}$  (slave),  $\overline{BUSY}$  is an input. Then for this example  $\overline{BUSY}^*A^* = V_{IH}$  and  $\overline{BUSY}^*B^*$  input is shown above.
- 5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with **BUSY** (M/**S** = VIL)

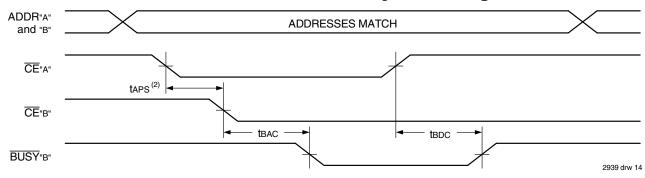


- 1. twH must be met for both  $\overline{BUSY}$  input (SLAVE) and output (MASTER).
- 2. BUSY is asserted on port "B" blocking R/W"B", until BUSY"B" goes HIGH.
- 3. twb is only for the "SLAVE" version.

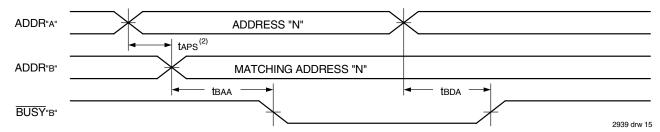


Military, Industrial and Commercial Temperature Ranges

# Waveform of **BUSY** Arbitration Controlled by **CE** Timing (M/**S** = VIH)(1)



# Waveform of **BUSY** Arbitration Cycle Controlled by Address Match Timing $(M/\overline{S} = VIH)^{(1)}$



#### NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
- 2. If taps is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.

# Truth Table III — Example of Semaphore Procurement Sequence(1,2,3)

Functions	Do - D15 Left	Do - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTES:

- 1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7026.
- 2. There are eight semaphore flags written to via I/Oo and read from all I/O's (I/Oo-I/O1s). These eight semaphores are addressed by Ao A2.
- 3.  $\overline{\text{CE}} = \text{VIH}$ ,  $\overline{\text{SEM}} = \text{VIL}$  to access the semaphores. Refer to the semaphore Read/Write Control Truth Table.

## Truth Table IV — Address **BUSY** Arbitration

Inputs			Outputs		
<u>C</u> EL	<del>C</del> ER	Aol-A13L Aor-A13R	BUS YL(1)	BUSY <sub>R</sub> (1)	Function
Χ	Χ	NO MATCH	Н	Н	Normal
Н	Χ	MATCH	Н	Н	Normal
Χ	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

NOTES:

- Pins BUSYL and BUSYR are both outputs when the part is configured as a master. Both are inputs when configured as a slave. BUSYx outputs on the IDT7026 are push pull, not open drain outputs. On slaves the BUSYx input internally inhibits writes.
- LOW if the inputs to the opposite port were stable prior to the address and enable inputs of this port. HIGH if the inputs to the opposite port became stable after the address and enable inputs of this port. If taps is not met, either BUSYL or BUSYR = LOW will result. BUSYL and BUSYR outputs cannot be LOW simultaneously.
- Writes to the left port are internally ignored when BUSY L outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

## **Functional Description**

The IDT7026 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7026 has an automatic power down feature controlled by  $\overline{\text{CE}}$ . The  $\overline{\text{CE}}$  controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{\text{CE}}$  = VIH). When a port is enabled, access to the entire memory array is permitted.

## **Busy Logic**

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The  $\overline{\text{BUSY}}$  pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a  $\overline{\text{BUSY}}$  indication, the write signal is gated internally to prevent the write from proceeding.

The use of  $\overline{BUSY}$  logic is not required or desirable for all applications. In some cases it may be useful to logically OR the  $\overline{BUSY}$  outputs together and use any  $\overline{BUSY}$  indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of  $\overline{BUSY}$  logic is not desirable, the  $\overline{BUSY}$  logic can be disabled by placing the part in slave mode with the  $M/\overline{S}$  pin. Once in slave mode the  $\overline{BUSY}$  pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the  $\overline{BUSY}$  pins HIGH. If desired, unintended write operations can be prevented to a port by tying the  $\overline{BUSY}$  pin for that port LOW.

The BUSY outputs on the IDT 7026 RAM in master mode, are pushpull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

# Width Expansion with **BUSY** Logic Master/Slave Arrays

When expanding an IDT7026 RAM array in width while using  $\overline{BUSY}$  logic, one master part is used to decide which side of the RAM array will receive a  $\overline{BUSY}$  indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the  $\overline{BUSY}$  signal as a write inhibit signal. Thus on the IDT7026 RAM the  $\overline{BUSY}$  pin is an output if the part is used as a master (M/ $\overline{S}$  pin = VIH), and the BUSY pin is an input if the part used as a slave (M/ $\overline{S}$  pin = VIL) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the

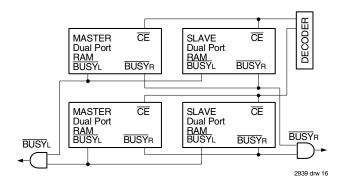


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7026 RAMs.

array and another master indicating  $\overline{\text{BUSY}}$  on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The  $\overline{BUSY}$  arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a  $\overline{BUSY}$  flag to be output from the master before the actual write pulse can be initiated with either the  $R/\overline{W}$  signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

# Semaphores

The IDT7026 is an extremely fast Dual-Port  $16K \times 16$  CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical infunction to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts

in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by  $\overline{CE}$ , the Dual-Port RAM enable, and  $\overline{SEM}$ , the semaphore enable. The  $\overline{CE}$  and  $\overline{SEM}$  pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where  $\overline{CE}$  and  $\overline{SEM}$  = VIH.

Systems which can best use the IDT7026 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7026's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7026 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

### How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7026 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the  $\overline{SEM}$  pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address,  $\overline{OE}$ , and  $R/\overline{W}$ ) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a

one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ( $\overline{SEM}$ ) and output enable ( $\overline{OE}$ ) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ( $\overline{SEM}$  or  $\overline{OE}$ ) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that

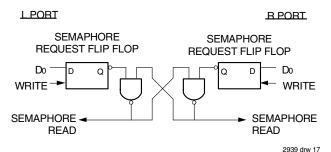


Figure 4. IDT7026 Semaphore Logic

semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

## Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7026's Dual-Port RAM. Say the 16K  $\times$  16 RAM was to be divided into two 8K  $\times$  16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K

section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

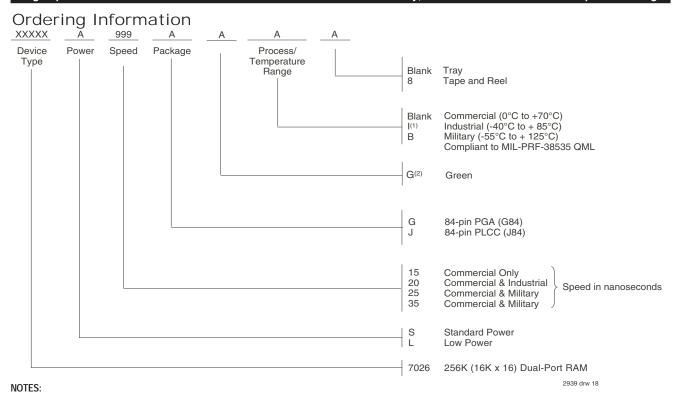
Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphorerequest and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphoreflags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate anywait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby quaranteeing a consistent data structure.



 $1. \ Industrial temperature range is available. For specific speeds, packages and powers contact your sales of fice.\\$ 

2. Green parts available. For specific speeds, packages and powers contact your local sales office

LEAD FINISH (SnPb) parts are Obsolete excluding PGA. Product Discontinuation Notice - PDN# SP-17-02 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

### Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	7026L15JG	PLG84	PLCC	С
	7026L15JG8	PLG84	PLCC	С
20	7026L20G	GU84	PGA	С
	7026L20JGI	PLG84	PLCC	I
	7026L20JGl8	PLG84	PLCC	I
25	7026L25G	GU84	PGA	С
	7026L25GB	GU84	PGA	М
35	7026L35G	GU84	PGA	С
	7026L35GB	GU84	PGA	М

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	7026S20G	GU84	PGA	С
25	7026S25G	GU84	PGA	С
35	7026S35G	GU84	PGA	С



Military, Industrial and Commercial Temperature Ranges

## **Datasheet Document History**

01/14/99: Initiated datasheet document history

Converted to new format

Cosmetic and typographical corrections

Pages 2 and 3 Added additional notes to pin configurations

060/3/99: Changed drawing format

Page 1 Corrected DSC number

03/10/00: Added Industrial Temperature Ranges and removed related notes

Replaced IDT logo

Page 1 Fixed format in Features Changed ±200mV to 0mV in notes

05/22/00: Page 3 Clarified Taparameter

Page 6 DC Electrical parameters-changed wording from "open" to "disabled"

11/20/01: Page 1 & 18 Verified accuracy of Industrial temp information throughout datasheet and updated with registered logo

Page 2 & 3 Added date revision for pin configurations

01/29/09: Page 18 Removed "IDT" from orderable part number

08/05/15: Page 1 In Features: Added text: "Green parts available, see ordering information".

Page 2 In Descriptions: Removed IDT in reference to fabrication

Page 2 &18 The package code J84-1 changed to J84 to match standard package codes Page 3 &18 The package code G84-1 changed to G84 to match standard package codes

Page 18 Added Green and Tape & Reel indicators to the Ordering Information and updated footnotes

03/07/18: Product Discontinuation Notice - PDN# SP-17-02

Last time buy expires June 15, 2018

08/29/19: Page 1 & 18 Deleted obsolete speed grades

Page 2 Rotated PLG84 PLCC pin configuration to accurately reflect pin 1 orientation

Page 18 Added Orderable Part Information tables

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