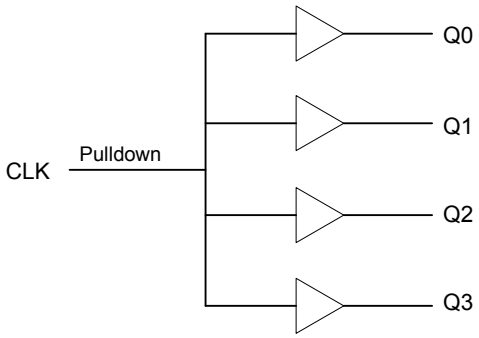
General Description

The IDT6T30028 is a low skew, 1-to-4 Fanout Buffer for Freescale systems. The IDT6T30028 is characterized at full 3.3V for input VDD, and mixed 3.3V and 2.5V for output operating supply modes (VDDO). Guaranteed output and part-to-part skew characteristics make the IDT6T30028 ideal for those clock distribution applications demanding well defined performance and repeatability.

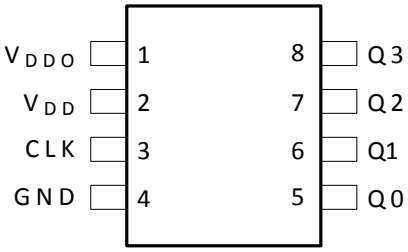
Features/Benefits

- Four LVCMOS / LVTTL outputs
- LVCMOS clock input
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 166MHz
- Output skew: 60ps (maximum)
- Part-to-part skew: 650ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- -40°C to +85°C ambient operating temperature
- Lead-free (RoHS 6) compliant packaging

Block Diagram



Pin Assignment



IDT6T30028
8-Lead SOIC
DCG Package
Top View

Pin Descriptions

Number	Name	Type		Description
1	VDDO	Power		Output supply pin. Connect to 3.3V or 2.5V.
2	VDD	Power		Positive supply pin. Connect to 3.3V.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground. Connect to ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

NOTE: Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} , V_{DDO} = 3.465V			15	pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance			7		Ω

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the IDT6T30028. These ratings are stress specifications only. Functional operation of the device at these or any other conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Symbol	Conditions	Rating	Units	Notes
Supply Voltage	V_{DD}		4.6	V	1,2
Inputs	V_I		-0.5 to V_{DD} + 0.5	V	1
Outputs	V_O		-0.5 to V_{DDD} + 0.5	V	1
Package Thermal Impedance	θ_{JA}		112.7	°C/W (0 lfpm)	1
Storage Temperature	T_{STG}		-65 to 150	°C	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Power Supply DC Characteristics

V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

Power Supply DC Characteristics

V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

LVCMOS/LVTTL DC Characteristics

V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.6			V
		I_{OH} = -16mA	2.9			V
		I_{OH} = -100µA	3			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V
		I_{OH} = -16mA			0.25	V
		I_{OH} = -100µA			0.15	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Section, "3.3V Output Load Test Circuit".

LVCMOS/LVTTL DC Characteristics

V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.1			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Section, "3.3V/2.5V Output Load Test Circuit".

AC Characteristics

V_{DD} = V_{DDO} = 3.3V±5% T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2		3.3	ns
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	125MHz, Integration Range 12kHz – 20MHz		0.17		ps
$t_{SK(O)}$	Output Skew; NOTE 2, 4	f = 133MHz			50	ps
$t_{SK(pp)}$	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 166MHz unless noted otherwise
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

AC Characteristics

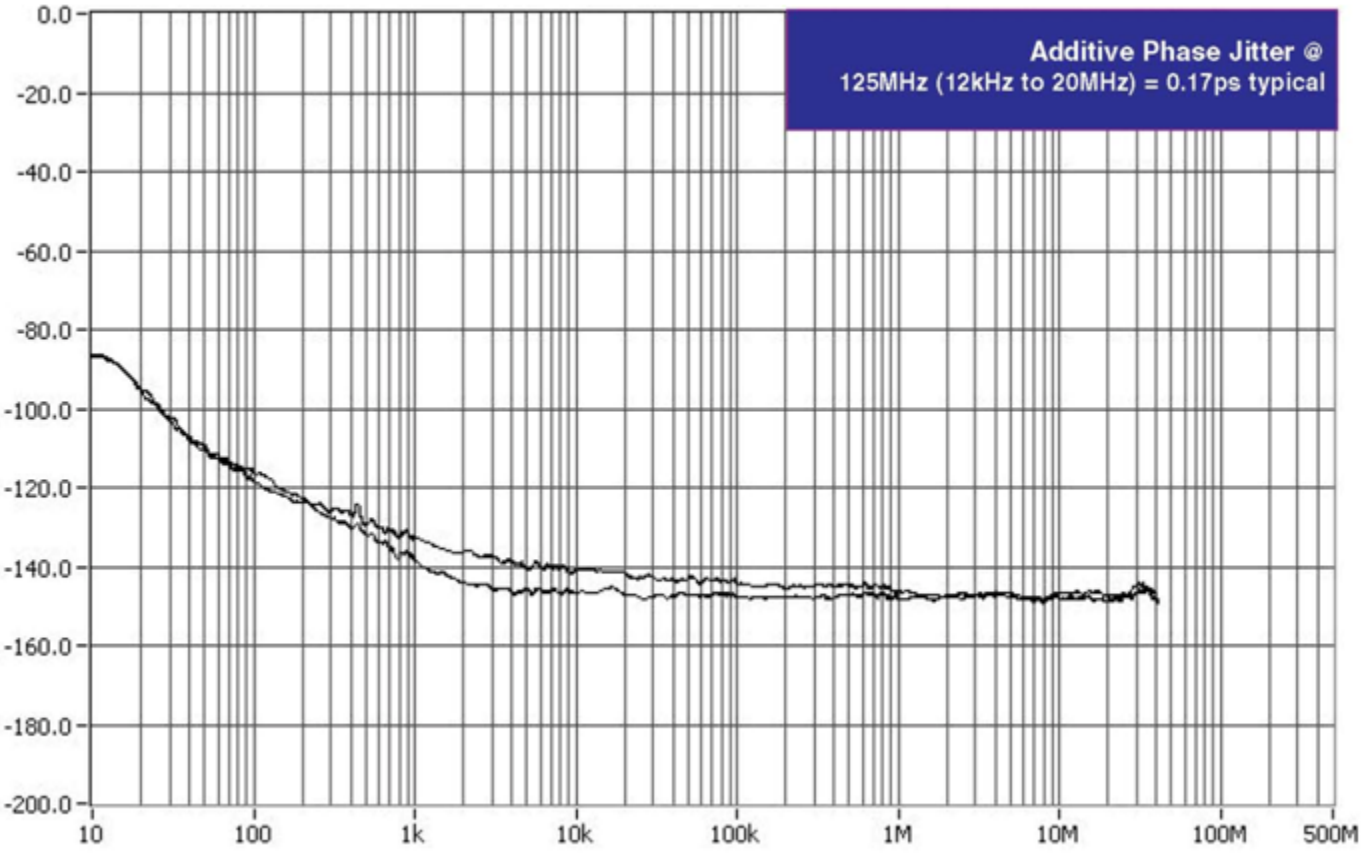
V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq$ 166MHz	2.3		3.7	ns
$t_{SK(O)}$	Output Skew; NOTE 2, 4	f = 133MHz			60	ps
$t_{SK(pp)}$	Part-to-Part Skew; NOTE 3, 4				650	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 166MHz unless noted otherwise
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

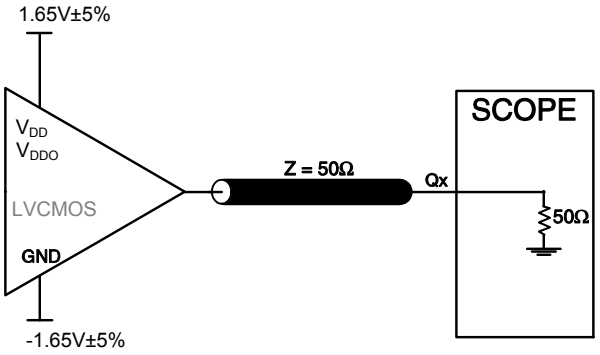
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a dBc value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

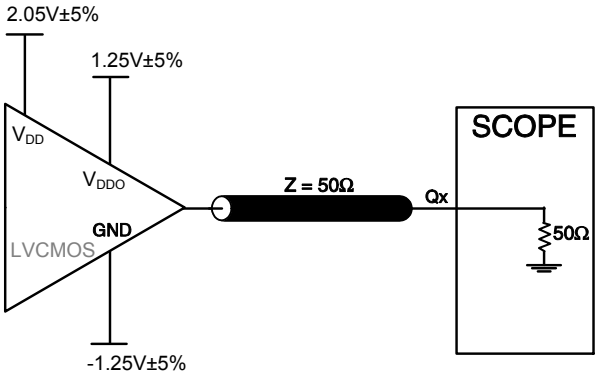


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

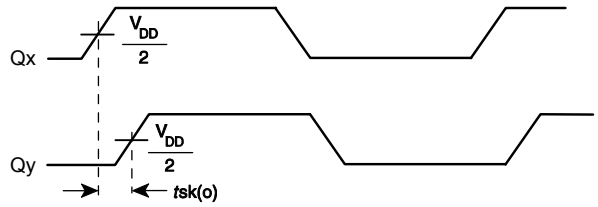
Parameter Measurement Information



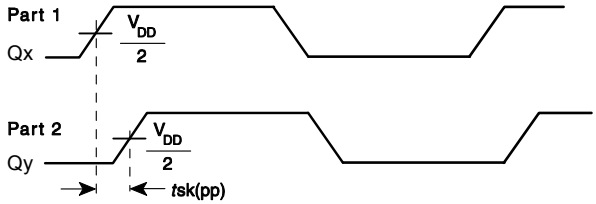
3.3V Output Load AC Test Circuit



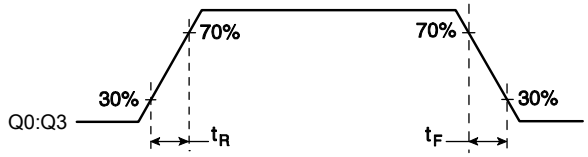
2.5V Output Load AC Test Circuit



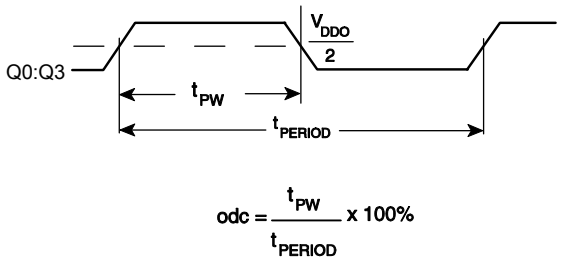
Output Skew



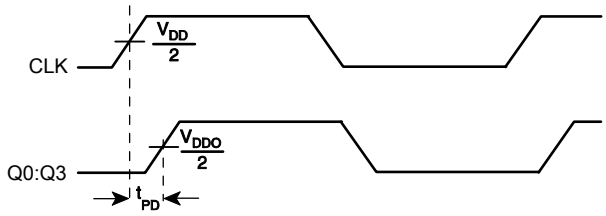
Part-to-Part Skew



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Propagation Delay

Reliability Information

θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)

	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

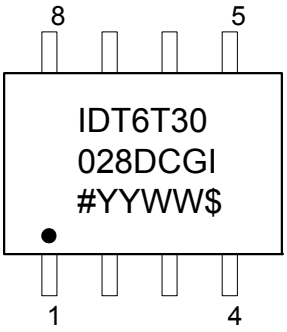
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transitor Count
The transistor count for IDT6T30028 is: 416

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		20		°C/W

Marking Diagram

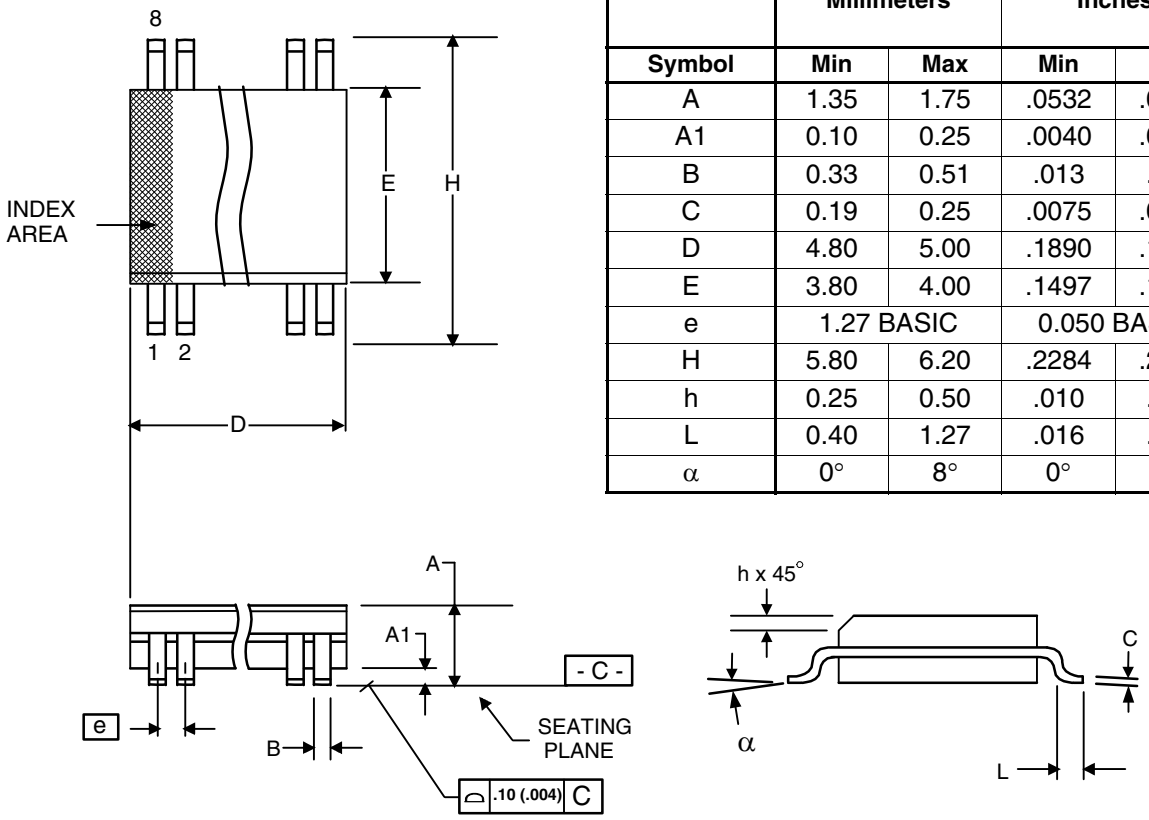


Notes:

1. '#' denotes the lot number.
2. '$' denote the mark code.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. "G" denotes RoHS compliant package.
5. 'I' denotes industrial temperature range.
6. Bottom marking: country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Package	Package	Temperature
6T30028DCGI	see page 9	Tubes	8-pin SOIC	-40 to +85°C
6T30028DCGI8		Tape and Reel	8-pin SOIC	-40 to +85°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Issuer	Issue Date	Description	Page #
A	L. Lua	6/18/2012	Initial release - preliminary	
B	RDW	4/18/2013	1. Updated front page description to include “for Freescale systems”. 2. Updated packaging information. 3. Moved from Preliminary to Final.	

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