## HDTV AUDIO/VIDEO CLOCK SOURCE

## ICS662-03

## Description

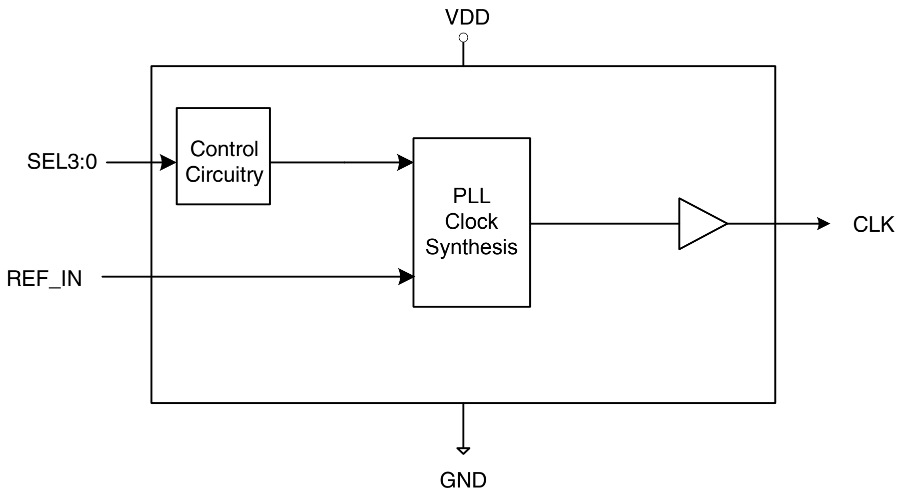
The ICS662-03 provides synchronous clock generation for audio sampling clock rates derived from an HDTV stream. The device uses the latest PLL technology to provide superior phase noise and long term jitter performance. The device also supports a 27 MHz output clock for video MPEG applications from an HDTV reference clock.

Please contact IDT if you have a requirement for an input and output frequency not included here.

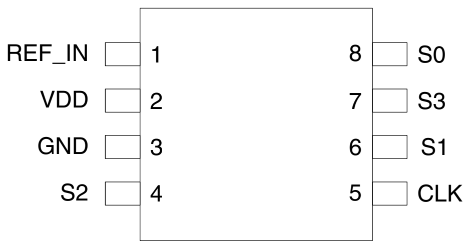
## Features

- Packaged in 8-pin SOIC
- Pb (lead) free package, RoHS compliant
- HDTV clock input
- Low phase noise
- Exact (0 ppm) multiplication ratios
- Support for 256 and 384 times sampling rate
- Supports 27 MHz output for video (MPEG)

## Block Diagram



## Pin Assignment




8 pin (150 mil) SOIC

## Output Clock Selection Table

| S3 | S2 | S1 | S0 | Input Frequency (MHz) | Output Frequency (MHz) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $74.\overline{175824}$ | 8.192 |
| 0 | 0 | 0 | 1 | $74.\overline{175824}$ | 11.2896 |
| 0 | 0 | 1 | 0 | $74.\overline{175824}$ | 12.288 |
| 0 | 0 | 1 | 1 | $74.\overline{175824}$ | 24.576 |
| 0 | 1 | 0 | 0 | $74.\overline{175824}$ | 16.9344 |
| 0 | 1 | 0 | 1 | $74.\overline{175824}$ | 18.432 |
| 0 | 1 | 1 | 0 | $74.\overline{175824}$ | 36.864 |
| 0 | 1 | 1 | 1 | $74.\overline{175824}$ | 27 |
| 1 | 0 | 0 | 0 | 74.25 | 8.192 |
| 1 | 0 | 0 | 1 | 74.25 | 11.2896 |
| 1 | 0 | 1 | 0 | 74.25 | 12.288 |
| 1 | 0 | 1 | 1 | 74.25 | 24.576 |
| 1 | 1 | 0 | 0 | 74.25 | 16.9344 |
| 1 | 1 | 0 | 1 | 74.25 | 18.432 |
| 1 | 1 | 1 | 0 | 74.25 | 36.864 |
| 1 | 1 | 1 | 1 | 74.25 | 27 |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | REF_IN | Input | Connect this pin to a HDTV clock input. |
| 2 | VDD | Power | Connect to +3.3 V. |
| 3 | GND | Power | Connect to ground. |
| 4 | S2 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 5 | CLK | Output | Clock output. |
| 6 | S1 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 7 | S3 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |
| 8 | S0 | Input | Output frequency selection. Determines output frequency per table above. On chip pull-up. |

## Application Information

### Series Termination Resistor

Clock output traces should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

### Decoupling Capacitors

As with any high performance mixed-signal IC, the ICS662-03 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between VDD (pin 2) and the PCB ground plane (pin 3).

### PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI and obtain the best signal integrity, the 33Ω series termination resistor should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS662-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS662-03. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 5.5 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.0 | 3.3 | 3.6 | V |
| Supply Current | IDD | No Load, first 8 modes | | 25 | 29 | mA |
| | | No Load, last 8 modes | | 16 | 21 | mA |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | | | 0.4 | V |
| Short Circuit Current | $I_{OS}$ | Each output | | ±50 | | mA |
| Nominal Output Impedance | $Z_{OUT}$ | | | 20 | | Ω |
| Input Capacitance | $C_{IN}$ | input pins | | 7 | | pF |
| Internal pull-up resistor | $R_{PU}$ | S2 pin | | 510 | | kΩ |
| | | S3, S1, S0 pins | | 120 | | kΩ |

## AC Electrical Characteristics

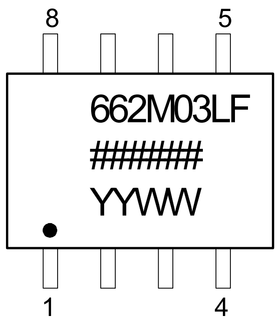
Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Clock Rise Time | $t_{OR}$ | 20% to 80%, 15 pF load | | 1.2 | 1.5 | ns |
| Output Clock Fall Time | $t_{OF}$ | 80% to 20%, 15 pF load | | 1.0 | 1.5 | ns |
| Output Duty Cycle | $t_{OD}$ | at VDD/2, 15 pF load | 45 | | 55 | % |
| Jitter, short term | $t_{P-P}$ | 15 pF load | | ±75 | | ps |
| Jitter, long term | | 27M output, 15 pF load, first 8 modes, 1000 cycles delay | | 900 | | ps |
| | | 27M output, 15 pF load, last 8 modes, 1000 cycles delay | | 600 | | ps |
| Frequency Synthesis Error | | | | 0 | | ppm |

## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 150 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 140 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 40 | | °C/W |

## Marking Diagram (ICS662M-03LF)

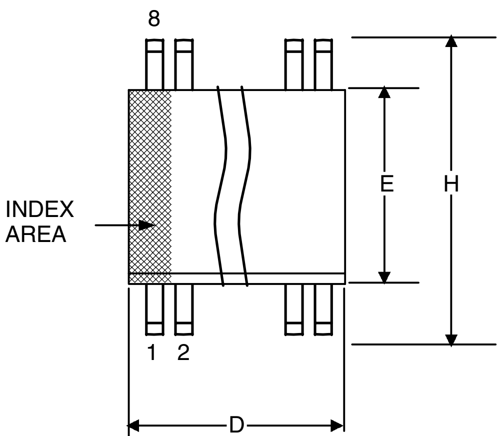



Notes:

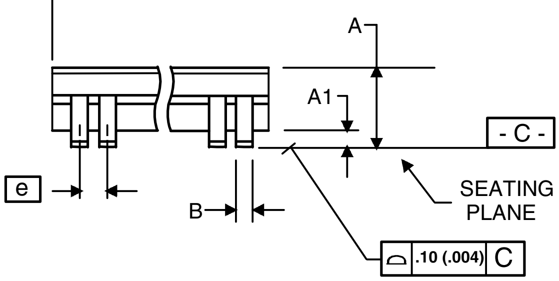
1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LF” denotes Pb (lead) free package.
4. Bottom marking: (origin). Origin = country of origin if not USA.

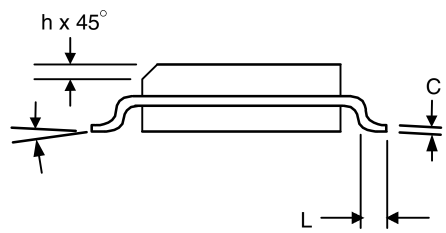
## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 4.80 | 5.00 | .1890 | .1968 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| $\alpha$ | 0° | 8° | 0° | 8° |




## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 662M-03LF | see page 5 | Tubes | 8-pin SOIC | 0 to +70° C |
| 662M-03LFT | | Tape and Reel | 8-pin SOIC | 0 to +70° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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