ETHERNET SWITCH CLOCK SOURCE

ICS650-40

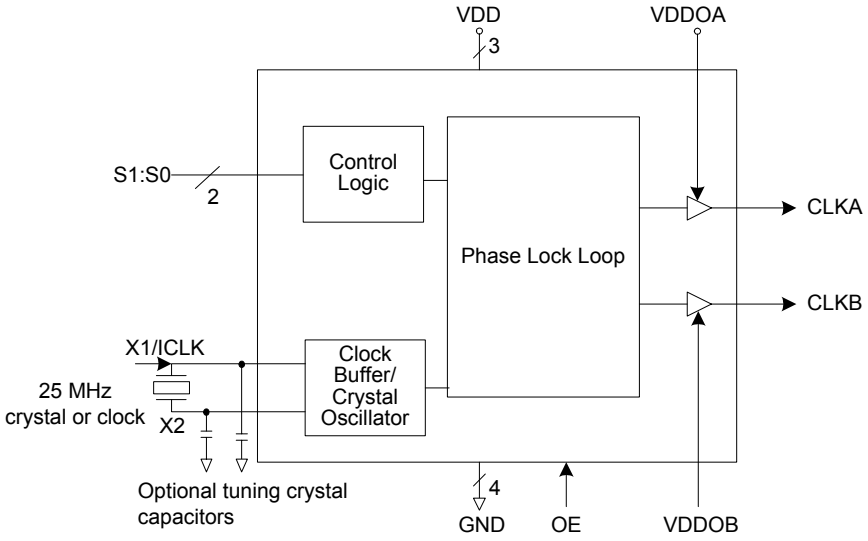
Description

The ICS650-40 is a clock chip designed for use in Ethernet Switch applications. Using IDT's patented Phase-Locked Loop (PLL) techniques, the device takes a 25 MHz crystal input and produces various output clock frequencies as listed in Output Select Table.

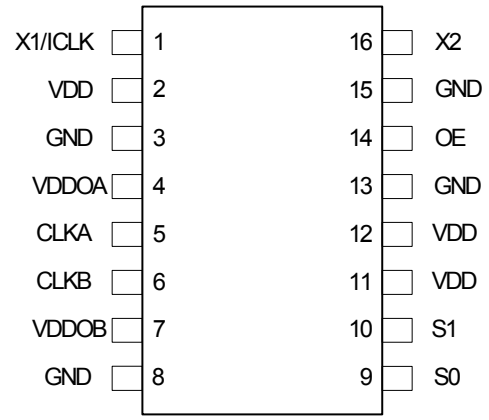
Features

- Packaged in 16-pin TSSOP
- Pb (lead) free package
- Operating voltage of 3.3 V
- Low power consumption
- Input frequency of 25 MHz
- Low long-term jitter
- 2.5 V to 3.3 V clock outputs

Block Diagram



Pin Assignment



16-pin (173 mil) TSSOP

Output Select Table (MHz)

S1	S0	CLKA (MHz)	CLKB (MHz)
0	0	127	127
0	1	133	133
1	0	157	157
1	1	189	189

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Crystal or clock input. Connect to a 25 MHz crystal or single ended clock.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	VDDOA	Power	Connect to +2.5 V or +3.3 V. For clock output buffer A only.
5	CLKA	Output	Clock A output with weak pull-down resistor.
6	CLKB	Output	Clock B output with weak pull-down resistor.
7	VDDOB	Power	Connect to +2.5 V or +3.3 V. For clock output buffer B only.
8	GND	Power	Connect to ground.
9	S0	Input	Select pin 0.
10	S1	Input	Select pin 1.
11	VDD	Power	Connect to +3.3 V.
12	VDD	Power	Connect to +3.3 V.
13	GND	Power	Connect to ground.
14	OE	Input	Output enable tri-states outputs and device is not shut down. Internal pull-up resistor.
15	GND	Power	Connect to ground.
16	X2	Output	Crystal connection. Leave unconnected for clock input.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD and GND pairs. The capacitors should be placed between pins VDD and GND, and VDDO and GND, as close to the device as possible. A 33Ω series terminating resistor should be used on each clock output if the trace is longer than 1 inch. A 25 MHz fundamental mode parallel resonant crystal should be used with C_L=18 pF.

On chip capacitors. On Chip capacitors are used for a 18 pF load crystal. Small 2 to 3 pf trimming capacitors are used from pins X1 to ground and X2 to ground to optimize the initial accuracy.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-40. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V

DC Electrical Characteristics

Unless otherwise specified, **VDD=3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Output Operating Voltage	VDDOA, B		2.375		3.45	V
Input High Voltage, ICLK	V_{IH}	Note 1	VDD/2+0.5			V
Input Low Voltage, ICLK	V_{IL}	Note 1			VDD/2-0.5	V
Input High Voltage, S1:S0:OE	V_{IH}		2		VDD	V
Input Low Voltage, S1:S0:OE	V_{IL}				0.4	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	No load		40		mA
IDD at Output Disable Condition(OE low)		No load		16		mA
Short Circuit Current	I_{OS}	Each output		±35		mA
Internal Pull-up Resistor	R_{PUP}	OE pin		250		kΩ
Internal Pull-down Resistor	R_{PD}	CLK outputs		525		kΩ

Note: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

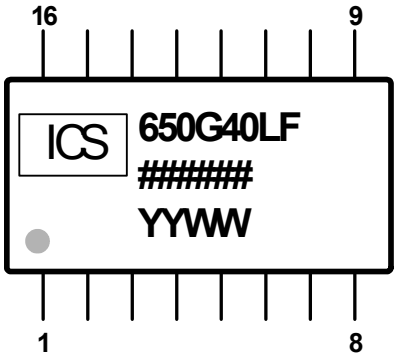
, **VDD = 3.3 V ±5%**, **VDDO = 2.5 - 3.3 V ±5%, C_L=10 pF** Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Rise Time	t_{OR}	20% to 80% of VDD		1.6		ns
Output Fall Time	t_{OF}	80% to 20% of VDD		1.6		ns
Output Clock Duty Cycle		at VDD/2	40	49-51	60	%
Frequency Error		all clocks		0		ppm
Output to Output Skew between clocks of the same frequency					250	ps
Absolute Jitter, Short-term P-P		variation from mean		±100	±200	ps
Absolute Jitter, Short-term C-C				200	400	ps
Long-term Jitter		1000 clock cycles		250	400	ps

Thermal Characteristics (16-pin TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Marking Diagram

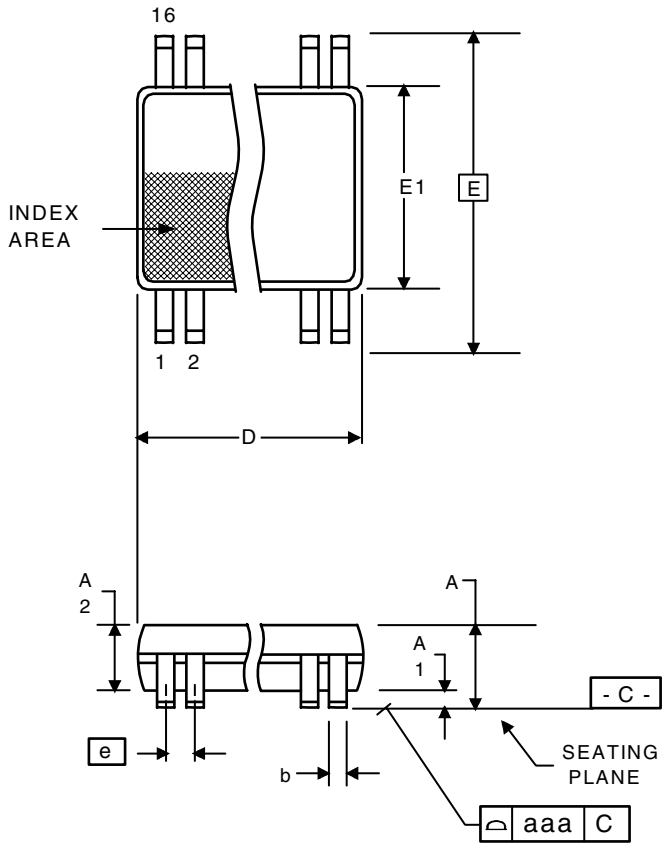


Notes:

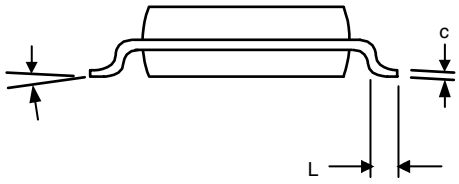
1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LF” designates Pb (lead) free package.
4. Bottom marking: (origin). Origin = country of origin if not USA.

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650G-40LF	See Page 6	Tubes	16-pin TSSOP	0 to +70° C
650G-40LFT		Tape and Reel	16-pin TSSOP	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.