

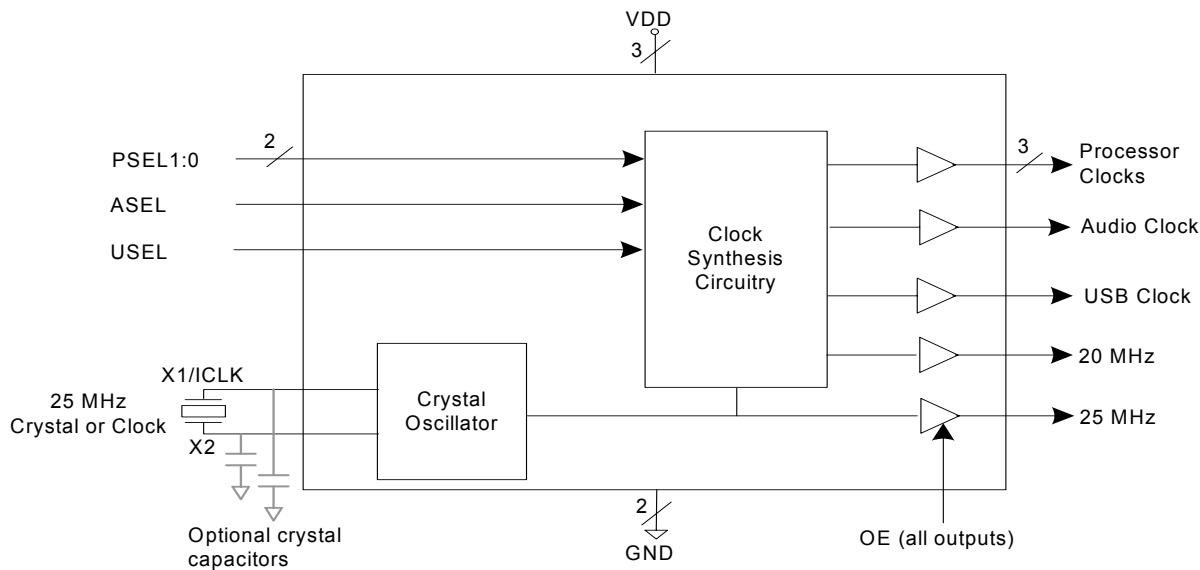
## Description

The ICS650-21 is a low cost, low-jitter, high-performance clock synthesizer for system peripheral applications. Using analog/digital Phase Locked Loop (PLL) techniques, the device accepts a parallel resonant 25 MHz crystal input to produce up to eight output clocks. The device provides clocks for PCI, SCSI, Fast Ethernet, Ethernet, USB, and AC97. The user can select one of three USB frequencies and also one of two AC97 audio frequencies. The OE pin puts all outputs into a high-impedance state for board level testing. All frequencies are generated with less than one ppm error, meeting the demands of SCSI and Ethernet clocking.

## Features

- Packaged in 20-pin SSOP (QSOP)
- Pb (lead) free package, RoHS compliant
- Lower jitter version of ICS650-01
- Operating voltage of 3.3 V or 5 V
- Zero ppm synthesis error in all clocks
- Inexpensive 25 MHz crystal or clock input
- Provides Ethernet and Fast Ethernet clocks
- Provides SCSI clocks
- Provides PCI clocks
- Selectable AC97 audio clock
- Selectable USB clock
- OE pin tri-states the outputs for testing
- Selectable frequencies on three clocks
- Duty cycle of 45/55 for Processor clock and Audio clock
- Advanced, low-power CMOS process
- Industrial temperature range available

## Block Diagram



## Pin Assignment

USEL	1	20	PSEL1
X2	2	19	PSEL0
X1/ICLK	3	18	PCLK2
VDD	4	17	PCLK3
VDD	5	16	VDD
GND	6	15	ASEL
UCLK	7	14	GND
20M	8	13	OFF/14.318M
ACLK	9	12	PCLK1
25M	10	11	OE

20-pin (150 mil) SSOP

## Processor Clock (MHz)

PSEL1	PSEL0	PCLK1	PCLK2, 3
0	0	25	50
0	M	TEST MODE	
0	1	TEST MODE	
M	0	40	80
M	M	33.3333	66.6667
M	1	20	40
1	0	20	33.3333
1	M	20	66.6667
1	1	50	100

## USB Clock (MHz)

USEL	UCLK
0	12
M	24
1	48

## Audio Clock (MHz)

ASEL	ACLK
0	49.152
M	24.576
1	14.318

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	USEL	Input	UCLK select pin. Determines frequency of USB clock per table above.
2	X2	XO	Crystal connection. Connect to parallel mode 25 MHz crystal. Leave open for clock.
3	X1/ICLK	XI	Crystal connection. Connect to parallel mode 25 MHz crystal or clock.
4	VDD	Power	Connect to VDD. Must be same value as other VDD. Decouple with pin 6.
5	VDD	Power	Connect to VDD. Must be same value as other VDD.
6	GND	Power	Connect to ground.
7	UCLK	Output	USB clock output per table above.
8	20M	Output	Fixed 20 MHz output for Ethernet.
9	ACLK	Output	AC97 audio clock output per table above.
10	25M	Output	Fixed 25 MHz reference output for Fast Ethernet.
11	OE	Input	Output enable. Tri-states all outputs when low.
12	PCLK1	Output	PCLK output number 1 per table above.

Pin Number	Pin Name	Pin Type	Pin Description
13	OFF/14.318M	Output	14.31818 MHz clock output only when ASEL = VDD.
14	GND	Power	Connect to ground.
15	ASEL	Input	ACLK select pin. Determines frequency of audio clock per table above.
16	VDD	Power	Connect to VDD. Must be same value as other VDD. Decouple with pin 14.
17	PCLK3	Output	PCLK output number 3 per table above.
18	PCLK2	Output	PCLK output number 2 per table above.
19	PSEL0	Input	Processor select pin #0. Determines frequencies on PCLKs 1-3 per table above.
20	PSEL1	Input	Processor select pin #1. Determines frequencies on PCLKs 1-3 per table above.

## External Components

The ICS650-21 requires a minimum number of external components for proper operation.

### Decoupling Capacitor

Decoupling capacitors of  $0.01\mu\text{F}$  must be connected between each VDD and GND (pins 4 and 6, pins 16 and 14), as close to the device as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

### Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a  $50\Omega$  trace (a commonly used trace

impedance) place a  $33\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is  $20\Omega$

### Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation,  $C_L$  is the crystal load capacitance. So, for a crystal with a  $16\text{pF}$  load capacitance, two  $20\text{ pF}$   $[(16-6) \times 2]$  capacitors should be used.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS650-21. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0	+3.3	+5.5	V

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V  $\pm$ 5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Supply Current	IDD	No load, Note 1		30		mA
Input High Voltage	V <sub>IH</sub>	Select inputs, OE	2			V
Input Low Voltage	V <sub>IL</sub>	Select inputs, OE			0.8	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	VDD-0.4			V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8 mA	2.4			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA			0.4	V
Short Circuit Current	I <sub>os</sub>	CLK output		$\pm$ 50		mA
Input Capacitance, inputs		Except X1		5		pF

Note 1: With all clocks at highest frequencies.

## AC Electrical Characteristics

Unless stated otherwise,  $VDD = 3.3 \text{ V} \pm 5\%$ , Ambient Temperature 0 to  $+70^\circ \text{ C}$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Clocks Accuracy (synthesis error)		All clocks			1	ppm
Output Rise Time	$t_{OR}$	0.8 to 2.0 V, Note 2		1.5		ns
Output Fall Time	$t_{OF}$	2.0 to 0.8 V, Note 2		1.5		ns
Output Clock Duty Cycle		UCLK, at $VDD/2$	40	50	60	%
		PCLK, ACLK, at $VDD/2$	45	50	55	%
One Sigma Jitter		Except ACLK		75		ps
		ACLK		120		ps
Absolute Clock Period Jitter		UCLK, 20M	-500		500	ps
Power-up Time		PLL lock time from power-up to 1% of final value		1	4	ms

Note 1: Values dependent on programming.

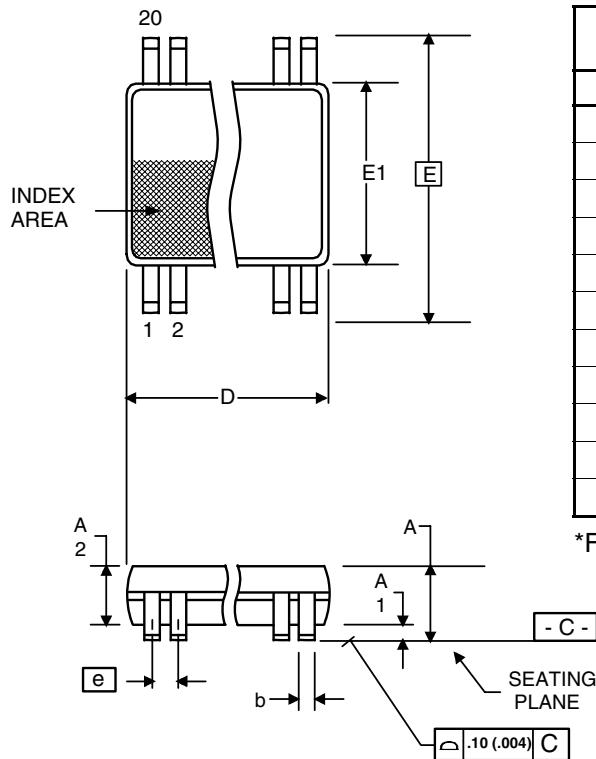
Note 2: Measured with 15 pF load.

## Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		135		$^\circ\text{C}/\text{W}$
	$\theta_{JA}$	1 m/s air flow		93		$^\circ\text{C}/\text{W}$
	$\theta_{JA}$	3 m/s air flow		78		$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Case	$\theta_{JC}$			60		$^\circ\text{C}/\text{W}$

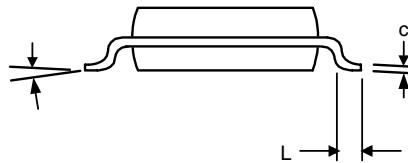
## Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	0.008	0.012
C	0.18	0.25	.007	.010
D	8.55	8.75	.337	.344
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
$\alpha$	0°	8°	0°	8°

\*For reference only. Controlling dimensions in mm.



## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
650R-21LF	ICS650R-21L	Tubes	20-pin SSOP	0 to +70° C
650R-21LFT	ICS650R-21L	Tape and Reel	20-pin SSOP	0 to +70° C
650R-21ILF	650R-21ILF	Tubes	20-pin SSOP	-40 to 85° C
650R-21ILFT	650R-21ILF	Tape and Reel	20-pin SSOP	-40 to 85° C

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

## Revision History

Rev.	Originator	Date	Description of Change
G	P. Griffith	02/15/06	Added “Power-up Time” spec in AC chars.
H		11/04/09	Added EOL note for non-green parts.
J		05/13/10	Removed EOL note and non-green parts.



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).