RJE0623JSP

–60V, –1.5A, P Channel Thermal FET
Power Switching

R07DS1470EJ0100
Rev.1.00
Jan 30, 2020

Description

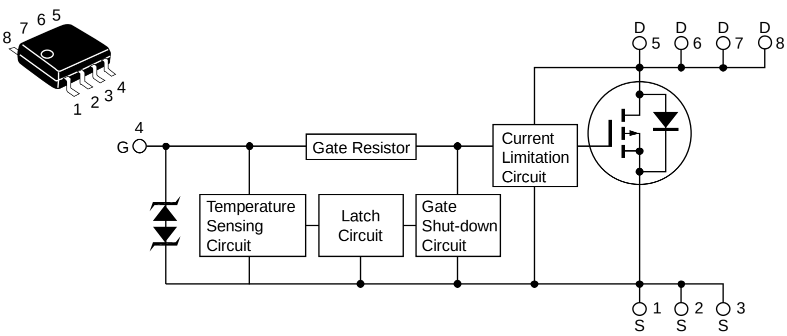
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (3 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Hysteresis type shut down operation.
- High density mounting.
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V.
- AEC-Q101compliant.

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	–16	V
Gate to source voltage	V_{GSS}	2.5	V
Drain current	I_D Note 3	–1.5	A
Body-drain diode reverse drain current	I_{DR}	–1.5	A
Avalanche current	I_{AP} Note 2	–1.5	A
Avalanche energy	E_{AR} Note 2	9.6	mJ
Channel dissipation	Pch Note 1	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s
2. Tch = 25°C, Rg ≥ 50 Ω
3. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	–3	—	—	V	
	V_{IL}	—	—	–1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	–100	µA	Vi = –8 V, V_{DS} = 0
	I_{IH2}	—	—	–50	µA	Vi = –3.5 V, V_{DS} = 0
	I_{IL}	—	—	–10	µA	Vi = –1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	–0.8	—	mA	Vi = –8 V, V_{DS} = 0
	$I_{IH(sd)2}$	—	–0.35	—	mA	Vi = –3.5 V, V_{DS} = 0
Shut down temperature	Tsd	—	175	—	°C	Channel temperature
Return temperature	Thr	—	105	—	°C	Channel temperature
Gate operation voltage	Vop	–3	—	–12	V	
Drain current (Current limitation value)	$I_{D\ limt}$	–1.5	—	—	A	V_{GS} = –12 V, V_{DS} = –10 V Note 4

Notes; 4. Pulse test

Electrical Characteristics

(Ta = 25°C)

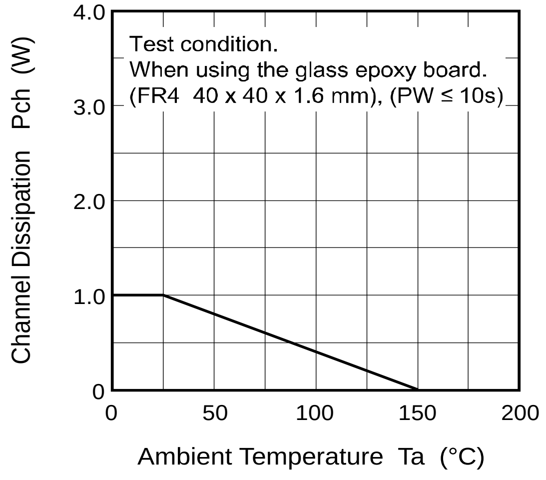
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_D	–1.5	—	–12	A	V_{GS} = –3.5 V, V_{DS} = –10 V Note 5
	I_D	—	—	–40	mA	V_{GS} = –1.2 V, V_{DS} = –10 V
	I_D	–1.5	—	—	A	V_{GS} = –12 V, V_{DS} = –10 V Note 5
	I_D	–0.8	—	—	A	V_{GS} = –3 V, V_{DS} = –10 V Note 5
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–16	—	—	V	I_G = –800 µA, V_{DS} = 0
	$V_{(BR)GSS}$	2.5	—	—	V	I_G = 100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	–100	µA	V_{GS} = –8 V, V_{DS} = 0
	I_{GSS}	—	—	–50	µA	V_{GS} = –3.5 V, V_{DS} = 0
	I_{GSS}	—	—	–10	µA	V_{GS} = –1.2 V, V_{DS} = 0
	I_{GSS}	—	—	100	µA	V_{GS} = 2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS(OP)}$	—	–0.8	—	mA	V_{GS} = –8 V, V_{DS} = 0
	$I_{GS(OP)}$	—	–0.35	—	mA	V_{GS} = –3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
	I_{DSS}	—	—	–10	µA	V_{DS} = –48 V, V_{GS} = 0 Ta = 125°C
Gate to source cutoff voltage	$V_{GS(off)}$	–0.9	—	–2.1	V	V_{DS} = –10 V, I_D = –1 mA
Forward transfer admittance	$\|y_{fs}\|$	1.5	2.7	—	S	I_D = –0.75 A, V_{GS} = –10 V Note 5
Static drain to source on state resistance	$R_{DS(on)}$	—	445	800	mΩ	I_D = –0.4 A, V_{GS} = –3V Note 5
	$R_{DS(on)}$	—	363	425	mΩ	I_D = –0.75 A, V_{GS} = –4 V Note 5
	$R_{DS(on)}$	—	272	350	mΩ	I_D = –0.75 A, V_{GS} = –10 V Note 5
Output capacitance	Coss	—	213	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	0.9	—	µs	V_{GS} = –10 V, I_D= –0.75 A, R_L = 40 Ω
Rise time	t_r	—	3.4	—	µs	
Turn-off delay time	$t_{d(off)}$	—	3.2	—	µs	
Fall time	t_f	—	6.3	—	µs	
Body-drain diode forward voltage	V_{DF}	—	–0.8	—	V	I_F = –1.5 A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = –1.5 A, V_{GS} = 0 di_F/dt = 50 A/µs
Over load shut down operation time Note 6	t_{os}	—	5.4	—	ms	V_{GS} = –5 V, V_{DD} = –16 V

Notes: 5. Pulse test

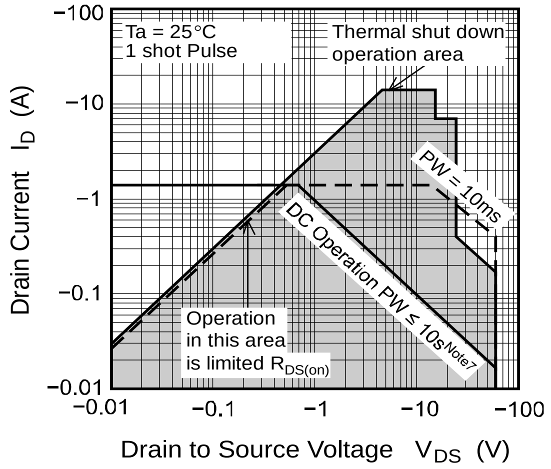
6. Including the junction temperature rise of the over loaded condition.

Main Characteristics

Power vs. Temperature Derating

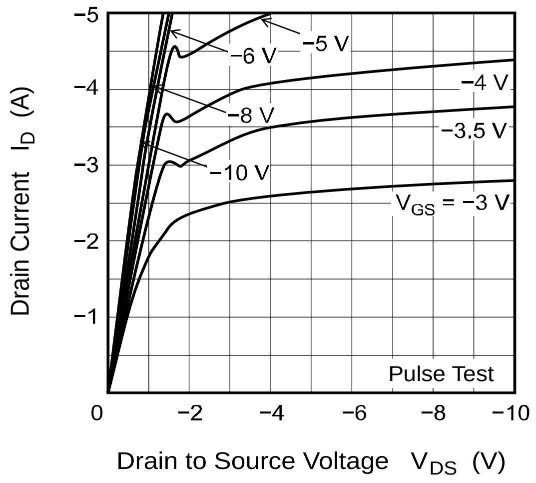


Maximum Safe Operation Area

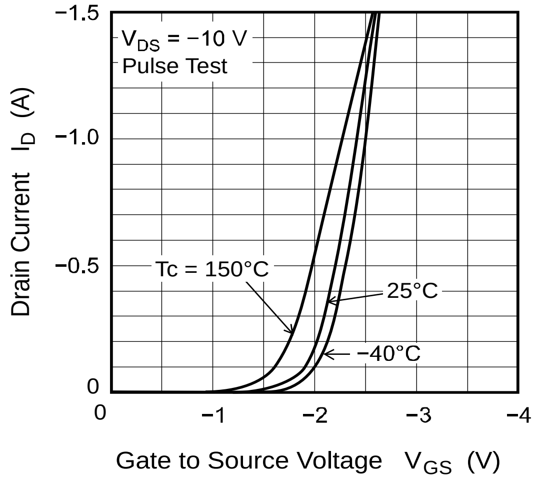


Note 7:
When using the glass epoxy board.
(FR4 40 x 40 x 1.6 mm)

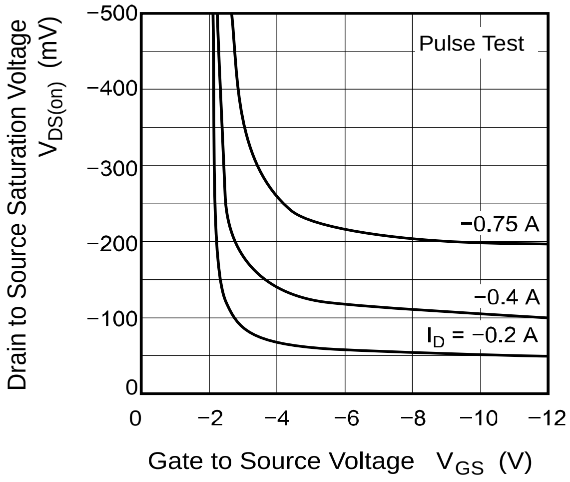
Typical Output Characteristics



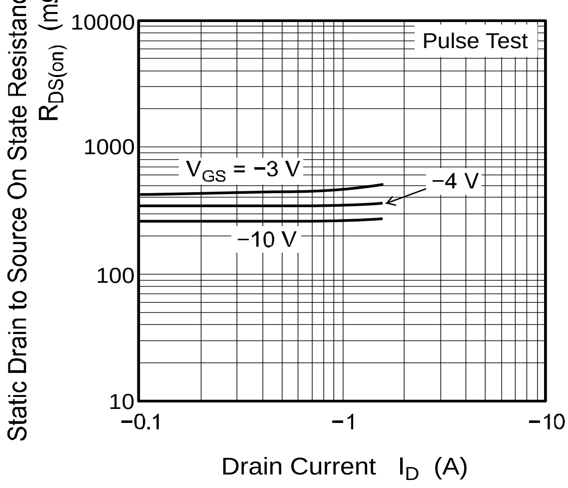
Typical Transfer Characteristics



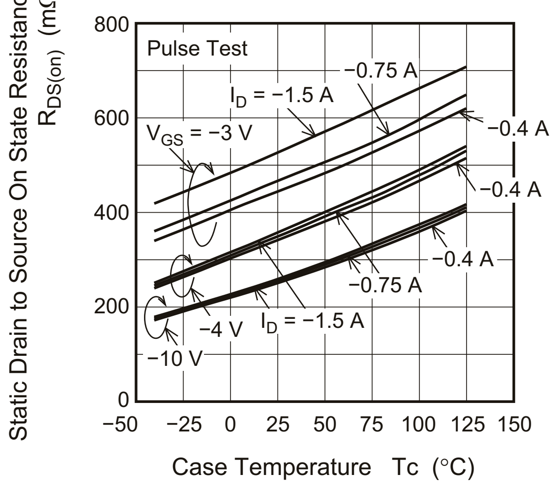
Drain Source Saturation Voltage vs.
Gate to Source Voltage



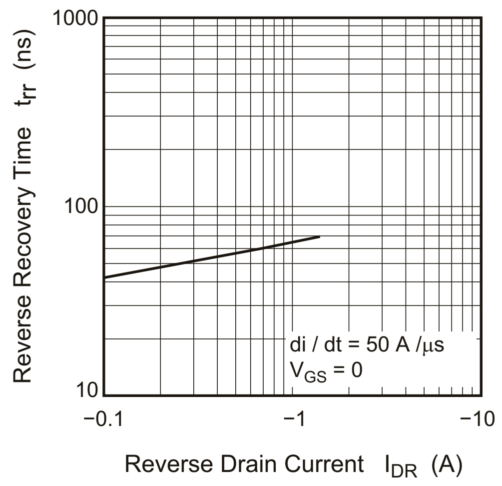
Static Drain to Source On State Resistance
vs. Drain Current



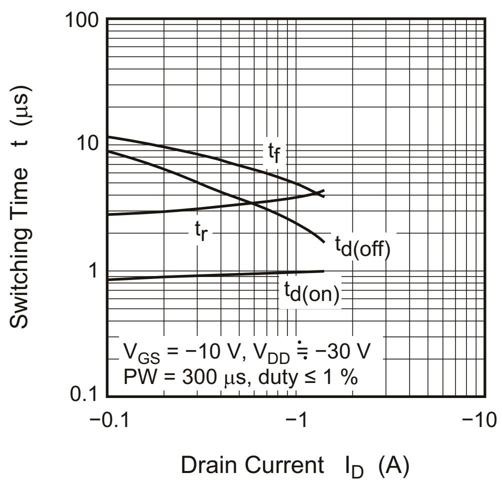
Static Drain to Source On State Resistance vs. Temperature



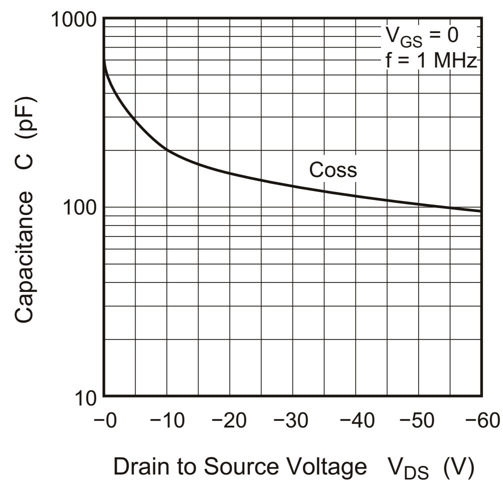
Body-Drain Diode Reverse Recovery Time



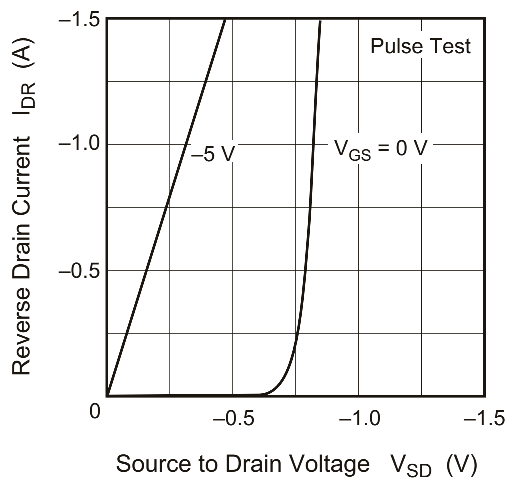
Switching Characteristics



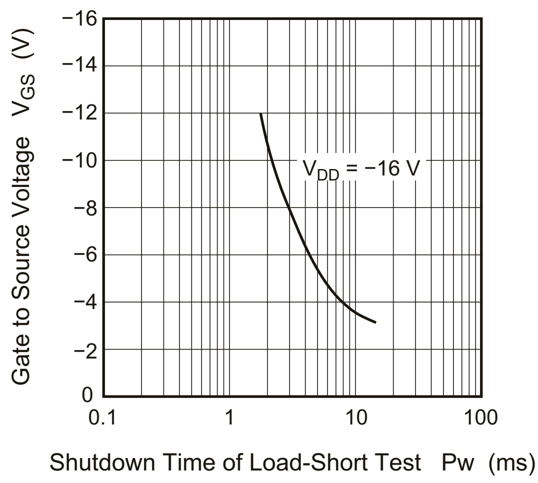
Typical Capacitance vs. Drain to Source Voltage

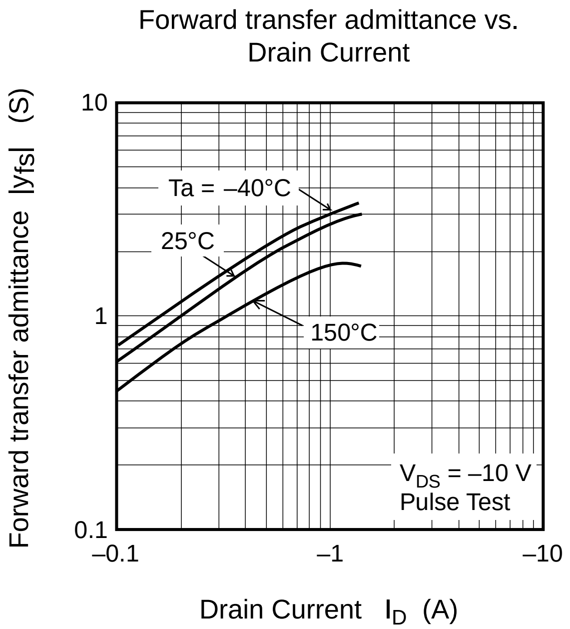


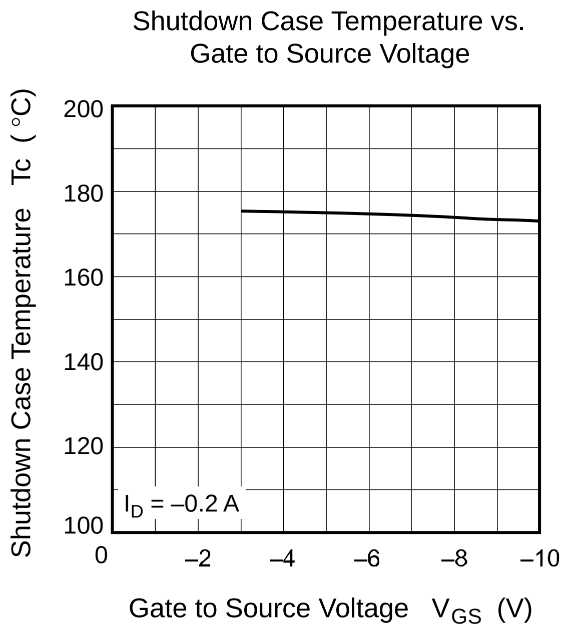
Reverse Drain Current vs. Source to Drain Voltage

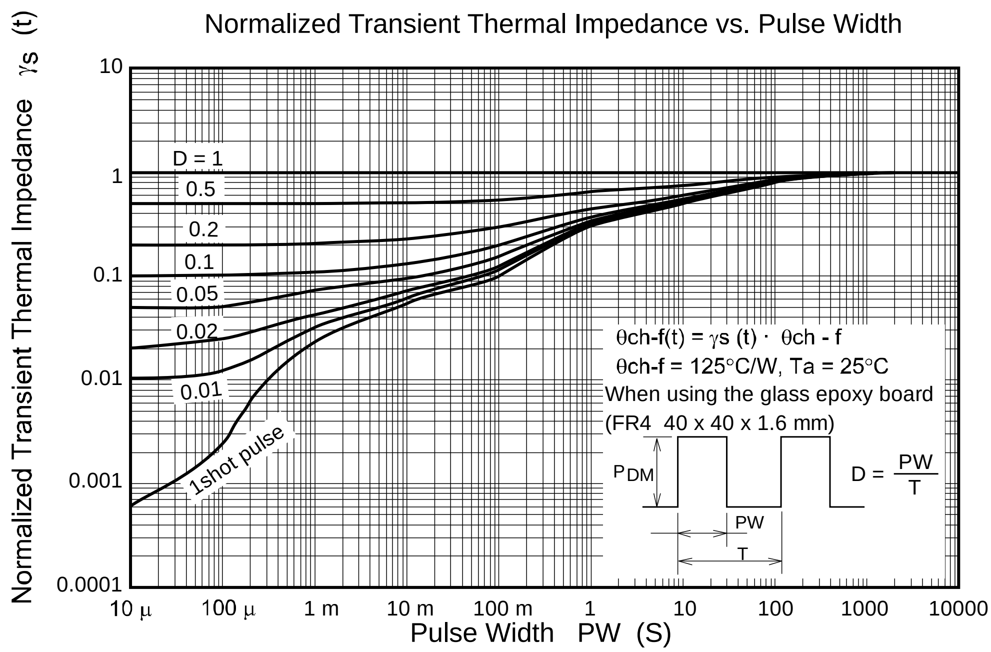


Gate to Source Voltage vs. Shutdown Time of Load-Short Test

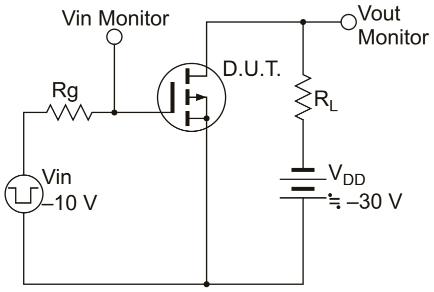



Forward transfer admittance vs.
Drain Current
Forward transfer admittance |yfs| (S)
10
1
0.1
–0.1
–1
–10
Ta = –40°C
25°C
150°C
VDS = –10 V
Pulse Test
Drain Current ID (A)

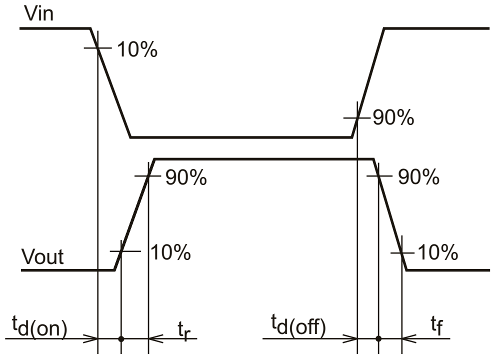

Shutdown Case Temperature vs.
Gate to Source Voltage
Shutdown Case Temperature Tc (°C)
200
180
160
140
120
100
0
–2
–4
–6
–8
–10
ID = –0.2 A
Gate to Source Voltage VGS (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
10
1
0.1
0.01
0.001
0.0001
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch-f(t) = γs (t) · θch - f
θch-f = 125°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)
PDM
D = PW / T
PW
T
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
Pulse Width PW (S)

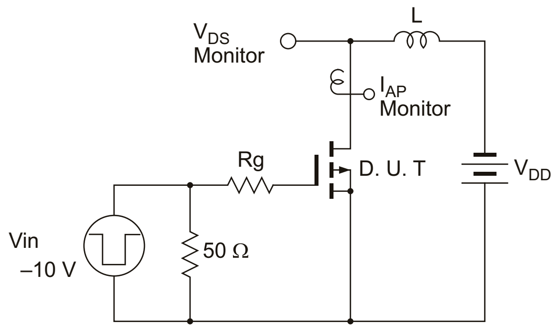
Switching Time Test Circuit



Waveform

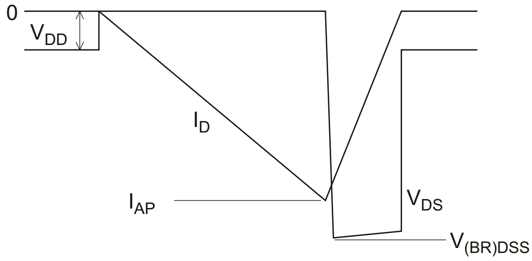


Avalanche Test Circuit



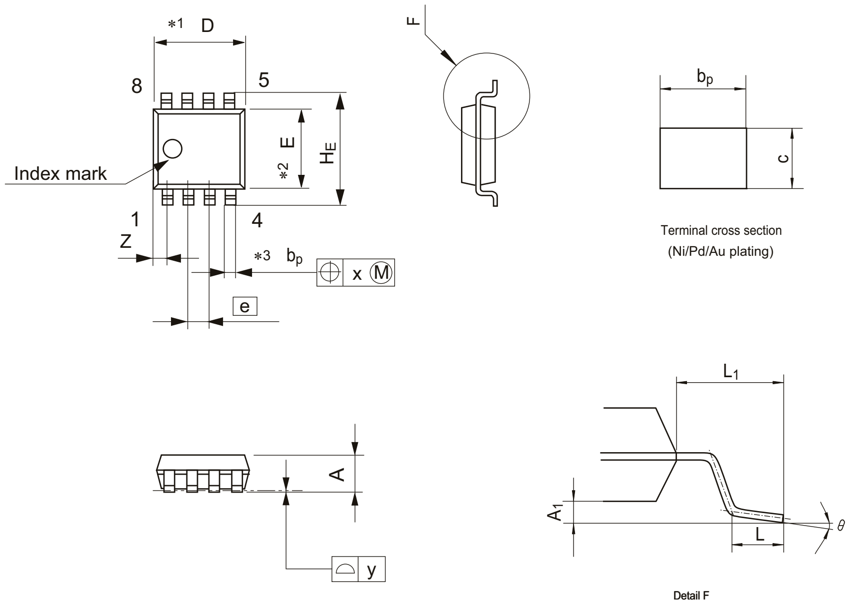
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJE0623JSP-00-J0	2500 pcs/reel	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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