Description

The 5V49EE902-255 is s a programmable clock generator intended for high performance data-communications, telecommunications, consumer, and networking applications. There are four internal PLLs, each individually programmable, allowing for four unique non-integer-related frequencies. The frequencies are generated from a single reference clock.

The IDT5V49EE902 datasheet contains detailed information on how to configure this device.

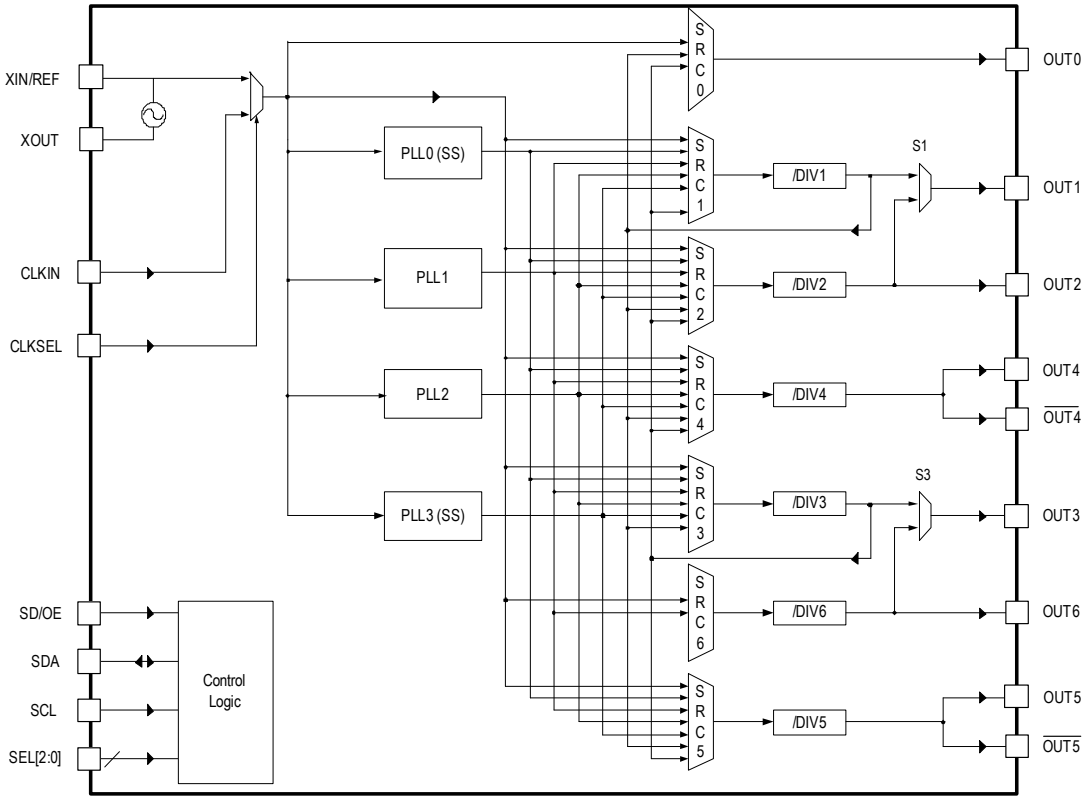
Typical Applications

- High-performance data communications
- Telecommunications
- Consumer applications
- Networking applications

Features

- Factory programmed with “5V49EE902-255” programming code
- Nine programmable outputs
- Four internal PLLs
- Two of the PLLs support spread spectrum generation capability
- Internal non-volatile EEPROM
- Fast (400kHz) mode I2C serial interface
- Four independently controlled V_{DDO} (1.8V–3.3V)
- I/O Standards:
  - Outputs: 1.8V–3.3V LVTTL/ LVCMOS
  - Outputs: LVPECL, LVDS and HCSL
  - Inputs: 3.3V LVTTL/ LVCMOS
- Redundant clock inputs with auto/manual switchover options
- Individual output enable/disable
- Power-down mode
- 3.3V core V_{DD}
- 5 x 5 mm 32-VFQFPN package, Pb-free
- -40° to +85°C industrial temperature operation

Block Diagram



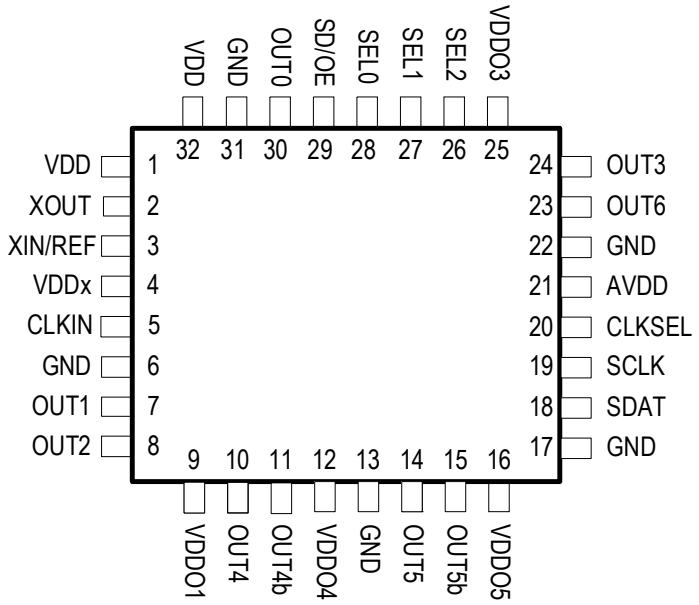
[1] OUT1/OUT2, OUT4/$\overline{\text{OUT4}}$, OUT3/OUT6, and OUT5/$\overline{\text{OUT5}}$ pairs can be configured to be LVDS, LVPECL or HCSL, or two single-ended LVTTL outputs.

[2] CLKIN, CLKSEL, SD/OE and SEL[2:0] have pull down resistors.

Contents

Pin Assignments

Figure 1. Pin Assignments for 5 × 5 mm 32-VFQFPN Package – Top View



5 × 5 mm 32-VFQFPN

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	I/O	Type	Description
5	CLKIN	I	LVTTL	Input clock. Weak internal pull-down resistor.
2	XOUT	O	LVTTL	CRYSTAL_OUT – Reference crystal feedback.
3	XIN/REF	I	LVTTL	CRYSTAL_IN – Reference crystal input or external reference clock input.
18	SDAT	I/O	Open Drain	Bidirectional I^2C data. An external pull-up resistor is required. See I^2C specification for pull-up value recommendation.
19	SCLK	I	LVTTL	I^2C clock. An external pull-up resistor is required. See I^2C specification for pull-up value recommendation.
20	CLKSEL	I	LVTTL	Input clock selector. Weak internal pull-down resistor.
26	SEL2	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
27	SEL1	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
28	SEL0	I	LVTTL	Configuration select pin. Weak internal pull -own resistor.
29	SD/OE	I	LVTTL	Enables/disables the outputs or powers down the chip. See Output Selection table. Weak internal pull-down resistor.
30	OUT0	O	LVTTL	Configurable clock output 0. 3.3V LVTTL levels.
7	OUT1	O	Adjustable[1]	Configurable clock output 1. Single-ended or differential when combined with OUT2. Output levels controlled by VDDO1.
8	OUT2	O	Adjustable[1]	Configurable clock output 2. Single-ended or differential when combined with OUT1. Output levels controlled by VDDO1.

Table 1. Pin Descriptions (Cont.)

Number	Name	I/O	Type	Description
24	OUT3	O	Adjustable[1]	Configurable clock output 3. Single-ended or differential when combined with OUT6. Output levels controlled by VDDO3.
10	OUT4	O	Adjustable[1,2]	Configurable clock output 4. Single-ended or differential when combined with OUT4b. Output levels controlled by VDDO4.
11	OUT4b	O	Adjustable[1,2]	Configurable clock output 4b. Single-ended or differential when combined with OUT4. Output levels controlled by VDDO4.
14	OUT5	O	Adjustable[1,2]	Configurable clock output 5. Single-ended or differential when combined with OUT5b. Output levels controlled by VDDO5.
15	OUT5b	O	Adjustable[1,2]	Configurable clock output 5b. Single-ended or differential when combined with OUT5. Output levels controlled by VDDO5.
23	OUT6	O	Adjustable[1]	Configurable clock output 6. Single-ended or differential when combined with OUT3. Output levels controlled by VDDO3.
1, 4, 21, 32	VDD		Power	Device power supply. Connect to 3.3V.
4	VDDx		Power	Crystal oscillator power supply. Connect to 3.3V through 5Ω resistor. Use filtered analog power supply if available.
21	AVDD		Power	Device analog power supply. Connect to 3.3V. Use filtered analog power supply if available.
9	VDDO1		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1 and OUT2.
25	VDDO3		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3 and OUT6.
12	VDDO4		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT4 and OUT4b.
16	VDDO5		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT5 and OUT5b.
6, 13, 17, 22, 31, PAD	GND		Power	Connect to Ground.

[1] Outputs are user programmable to drive single-ended 3.3V LVTTL, or differential LVDS, LVPECL or HCSL interface levels

[2] When only an individual single-ended clock output is required, tie OUT# and OUT#b together.

[3] Analog power plane should be isolated from a 3.3V power plane through a ferrite bead.

[4] Each power pin should have a dedicated 0.01µF de-coupling capacitor. Digital VDDs may be tied together.

[5] Unused clock inputs (REFIN or CLKIN) must be pulled high or low - they cannot be left floating. If the crystal oscillator is not used, XOUT must be left floating.

Output Selection

SEL			SD/OE	Input	Input Frequency (MHz)	OUT0 (MHz)	OUT1 (P) (MHz)	OUT2 (N) (MHz)	OUT3 (MHz)	OUT4 (P) (MHz)	OUT4b (N) (MHz)	OUT5 (P) (MHz)	OUT5b (N) (MHz)	OUT6 (MHz)
S2	S1	S0												
0	0	0	1	Crystal	24	24.000	100.00	100.00	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	1	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
0	1	0	1	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
0	1	1	1	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	1	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
1	0	1	1	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
000–101			0	Crystal	24	24.000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
110–111			X	N/A										
Driver Type				N/A	N/A	LVTTL	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS
VDDO (V)				N/A	N/A	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
VDDO Pin				N/A	N/A	VDD	VDDO1	VDDO1	VDDO3	VDDO4	VDDO4	VDDO5	VDDO5	N/A

Programming the Device

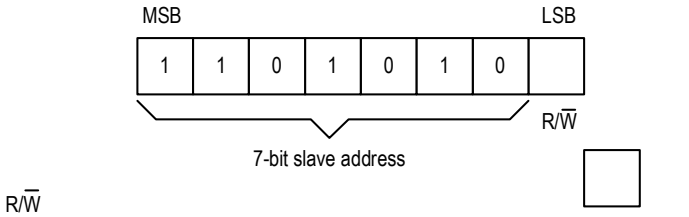
I2C may be used to program the 5V49EE902-255.

- Device (slave) address = 7'b1101010

I2C Programming

The 5V49EE902-255 is programmed through an I2C-Bus serial interface, and is an I2C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

Figure 2. First Byte Transmitted on I2C Bus

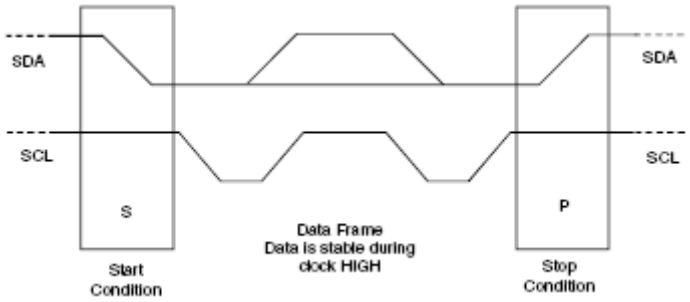


R/W
0 – Slave will be written by master
1 – Slave will be read by master

The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a "1" bit.

The frame formats are shown in Figure 3.

Figure 3. Framing



External I2C Interface Condition

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence
Normally, data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a separate START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDAT LOW)
NACK – Not Acknowledge (SDAT HIGH)
SR – Repeated Start Condition
S – START Condition
P – STOP Condition

Progwrite

Figure 4. Progwrite Command Frame

S§	Address§	R/W§	ACK§	Command Code§	ACK§	Register§	ACK§	Data§	ACK§	P§
§	7-bits§	0§	1-bit§	8-bits: xxxx xx00§	1-bit§	8-bits§	1-bit§	8-bits§	1-bit§	§

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

Progread

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S§	Address§	R/W§	ACK§	Command Code§	ACK§	Register§	ACK§	P§
§	7-bits§	0§	1-bit§	8-bits: xxxx xx00§	1-bit§	8-bits§	1-bit§	§

Prior to Progread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgment bit (i.e., followed by the Progread command):

Figure 5. Progread Command Frame

S§	Address§	R/W§	ACK§	ID Byte§	ACK§	Data_1§	ACK§	Data_2§	ACK§	Data_last§	NACK§	P§
§	7-bits§	1§	1-bit§	8-bits§	1-bit§	8-bits§	1-bit§	8-bits§	1-bit§	8-bits§	1-bit§	§

Progsave

S§	Address§	R/W§	ACK§	Command Code§	ACK§	P§
§	7-bits§	0§	1-bit§	8-bits: xxxx xx01§	1-bit§	§

Note:

PROGWRITE is for writing to the 5V49EE902-255 registers.

PROGREAD is for reading the 5V49EE902-255 registers.

PROGSAVE is for saving all the contents of the 5V49EE902-255 registers to the EEPROM.

PROGRESTORE is for loading the entire EEPROM contents to the 5V49EE902-255 registers.

Progrestore

S§	Address§	R/W§	ACK§	Command Code§	ACK§	P§
§	7-bits§	0§	1-bit§	8-bits: xxxx xx10§	1-bit§	§

EEPROM Interface

The 5V49EE902-255 can also store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (Progsave) and can be loaded back to the internal programming registers by issuing a restore instruction (Progrestore).

To initiate a save or restore using I2C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the 5V49EE902-255 will not generate Acknowledge bits. The 5V49EE902-255 will acknowledge the instructions after it has completed execution of them. During that time, the I2C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5V49EE902-255, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The 5V49EE902-255 will be ready to accept a programming instruction once it acknowledges its 7-bit I2C address.

I²C Bus Characteristics

Table 2. I²C Bus DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Level		0.7 x V_{DDD}			V
V_{IL}	Input Low Level				0.3 x V_{DDD}	V
V_{HYS}	Hysteresis of Inputs		0.05 x V_{DDD}			V
I_{IN}	Input Leakage Current				±1.0	µA
V_{OL}	Output Low Voltage	I_{OL} = 3mA.			0.4	V

Table 3. I²C Bus AC Characteristics for Standard Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
F_{SCLK}	Serial Clock Frequency (SCL)		0		100	kHz
t_{BUF}	Bus Free Time between Stop and Start		4.7			µs
$t_{SU:START}$	Setup Time, Start		4.7			µs
$t_{HD:START}$	Hold Time, Start		4			µs
$t_{SU:DATA}$	Setup Time, Data Input (SDA)		250			µs
$t_{HD:DATA}$	Hold Time, Data Input (SDA) [1]		0			µs
t_{OVD}	Output Data Valid from Clock				3.45	µs
C_B	Capacitive Load for Each Bus Line				400	pF
t_R	Rise Time, Data and Clock (SDAT, SCLK)				1000	ns
t_F	Fall Time, Data and Clock (SDAT, SCLK)				300	ns
t_{HIGH}	High Time, Clock (SCLK)		4			µs
t_{LOW}	Low Time, Clock (SCLK)		4.7			µs
$t_{SU:STOP}$	Setup Time, Stop		4			µs

[1] A device must internally provide a hold time of at least 300ns for the SDAT signal (referred to the $V_{IH(MIN)}$ of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

Table 4. I²C Bus AC Characteristics for Fast Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
F_{SCLK}	Serial Clock Frequency (SCL)		0		400	kHz
t_{BUF}	Bus Free Time between Stop and Start		1.3			µs
$t_{SU:START}$	Setup Time, Start		0.6			µs
$t_{HD:START}$	Hold Time, Start		0.6			µs
$t_{SU:DATA}$	Setup Time, Data Input (SDA)		100			ns
$t_{HD:DATA}$	Hold Time, Data Input (SDA) [1]		0			µs
t_{OVD}	Output Data Valid from Clock				0.9	µs

Table 4. I^2C Bus AC Characteristics for Fast Mode (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C_B	Capacitive Load for Each Bus Line				400	pF
t_R	Rise Time, Data and Clock (SDA, SCL)		20 + 0.1 x C_B		300	ns
t_F	Fall Time, Data and Clock (SDA, SCL)		20 + 0.1 x C_B		300	ns
t_{HIGH}	High Time, Clock (SCL)		0.6			µs
t_{LOW}	Low Time, Clock (SCL)		1.3			µs
$t_{SU:STOP}$	Setup Time, Stop		0.6			µs

[1] A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5V49EE902-255 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Internal Power Supply Voltage	-0.5	+4.6	V
V_I	Input Voltage [1]	-0.5	+4.6	V
V_O	Output Voltage (not to exceed 4.6 V) [1]	-0.5	V_{DD}+0.5	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

[1] Input negative and output voltage ratings may be exceeded if the input and output current ratings are observed.

Thermal Characteristics

Table 6. Thermal Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still air.		34		°C/W
	Θ_{JA}	1 m/s air flow.		29		°C/W
	Θ_{JA}	3 m/s air flow.		27		°C/W
Thermal Resistance Junction to Case	Θ_{JC}			32		°C/W

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage for V_{DD} pins supporting core and outputs.	3.135	3.3	3.465	V
V_{DDX}	Power supply voltage for crystal oscillator. Use filtered analog power supply if available.	3.135	3.3	3.465	V
AV_{DD}	Analog power supply voltage. Use filtered analog power supply if available.	3.135	3.3	3.465	V
V_{DDOX}	3.3V V_{DDO} Range.	3.0	3.3	3.465	V
	Power supply voltage for V_{DD} pins supporting LVDS/LVPECL/HCSL outputs.	3.135	3.3	3.465	V
T_A	Operating temperature, ambient.	-40		+85	°C
C_{LOAD_OUT}	Maximum load capacitance (3.3V LVTTL only).			15	pF
F_{IN}	External reference crystal.		24		MHz
	External reference clock CLKIN.		24		MHz
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05		5	ms

Capacitance

(T_A = +25°C)

Table 8. Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance (CLKIN, CLKSEL, SD/OE, SDA, SCL, SEL[2:0]).		3	7	pF
Pull-down Resistor	CLKIN, CLKSEL, SD/OE, SEL[2:0].		180		kΩ
Crystal Specifications					
XTAL_FREQ	Crystal frequency.		24		MHz
XTAL_MIN	Minimum crystal load capacitance.	3.5			pF
XTAL_MAX	Maximum crystal load capacitance.			35.5	pF
XTAL_V_{PP}	Voltage swing (peak-to-peak, nominal).	1.5	2.3	3.2	V

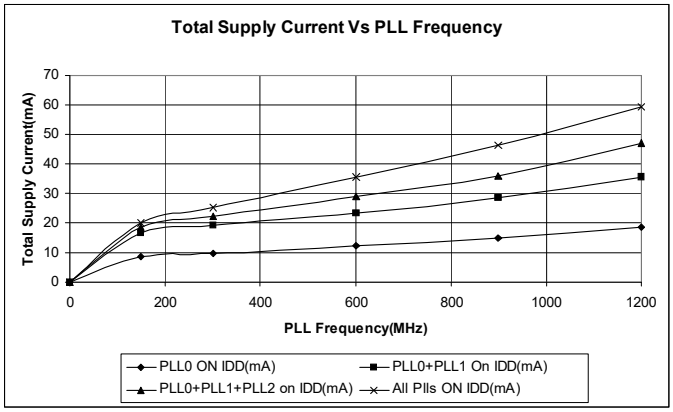
DC Electrical Characteristics

Table 9. DC Electrical Characteristics for 3.3V LVTTL

(see Recommended Operating Conditions table)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output HIGH Voltage		2.4		V_{DD}	V
V_{OL}	Output LOW Voltage				0.4	V
V_{IH}	Input HIGH Voltage		2			V
V_{IL}	Input LOW Voltage				0.8	V
I_{OZDD}	Output Leakage Current	3-state outputs. $V_O = V_{DD}$ or GND, V_{DD} = 3.465V			10	µA

Figure 6. Power Supply Characteristics for PLLs and LVTTL Outputs



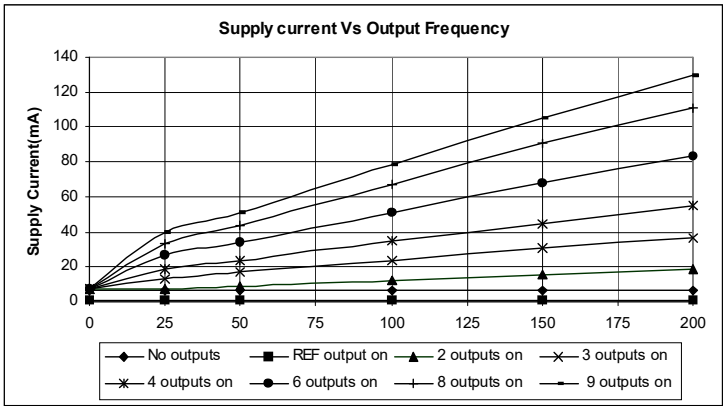


Table 10. DC Electrical Characteristics for LVDS

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{OT} (+)	Differential Output Voltage for the TRUE binary state	247		454	mV
V_{OT} (-)	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\triangle V_{OT}$	Change in V_{OT} between Complimentary Output States			50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)	1.125	1.2	1.375	V
$\triangle V_{OS}$	Change in V_{OS} between Complimentary Output States			50	mV
I_{OS}	Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DD}		9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-		6	12	mA

Table 11. Power Supply Characteristics for LVDS Outputs [1]

Symbol	Parameter	Conditions [2]	Typical	Maximum	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	REF = LOW Outputs enabled, all outputs unloaded.	68	90	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Maximum, C_L = 0pF.	30	45	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current	$F_{REFERENCE\ CLOCK}$ = 100MHz, C_L = 2pF.	86	130	mA
		$F_{REFERENCE\ CLOCK}$ = 200MHz, C_L = 2pF.	100	150	
		$F_{REFERENCE\ CLOCK}$ = 400MHz, C_L = 2pF.	122	190	

[1] Output banks 4 and 5 are toggling. Other output banks are powered down.

[2] The termination resistors are excluded from these measurements.

AC Timing Electrical Characteristics

Table 12. AC Timing Electrical Characteristics

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{IN} [1]	Input Frequency	Input frequency limit (CLKIN).		24		MHz
		Input frequency limit (XIN/REF).		24		MHz
t2	Input Duty Cycle	Duty cycle for input.	40		60	%
t3	Output Duty Cycle	Measured at V_{DD}/2, all outputs except Reference output.	45		55	%
		Measured at V_{DD}/2, Reference output.	40		60	%
t4 [2]	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DD}. (Output Load = 5pF)		2.5		V/ns
t5	Rise Times	LVDS, 20% to 80%.		505		ps
	Fall Times	LVDS, 80% to 20%.		505		
	Rise Times	LVTTL, 20% to 80%.		826		ps
	Fall Times	LVTTL, 80% to 20%.		826		
t7	Clock Jitter	Peak-to-peak period jitter, 1PLL, multiple output frequencies switching, LVTTL outputs.		80	100	ps
		Peak-to-peak period jitter, all 4 PLLs on, LVTTL outputs.		200	270	ps
		Peak-to-peak period jitter, 1PLL, multiple output frequencies switching, LVPECL, LVDS or HCSL outputs.		60	80	ps
		Peak-to-peak period jitter, all 4 PLLs on, LVPECL, LVDS or HCSL outputs.		120	160	ps

Table 12. AC Timing Electrical Characteristics (Cont.)

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t8	Output Skew	Skew between output to output on the same bank.			75	ps
t9 [3]	Lock Time	PLL lock time from power-up.		10	20	ms
t10 [4]	Lock Time	PLL lock time from shutdown mode.			2	ms

[1] Practical lower frequency is determined by loop filter settings.

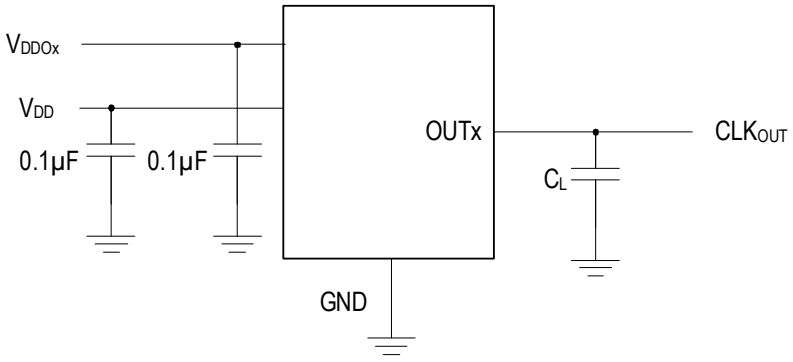
[2] A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

[3] Includes loading the configuration bits from EEPROM to PLL registers. It does not include EEPROM programming/write time.

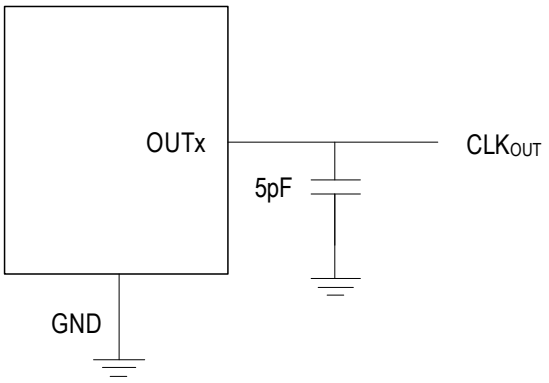
[4] Actual PLL lock time depends on the loop configuration.

Test Circuits and Conditions

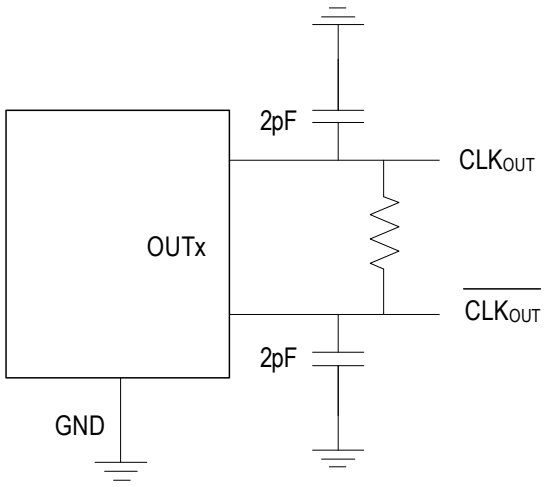
Figure 7. Test Circuits for DC Outputs



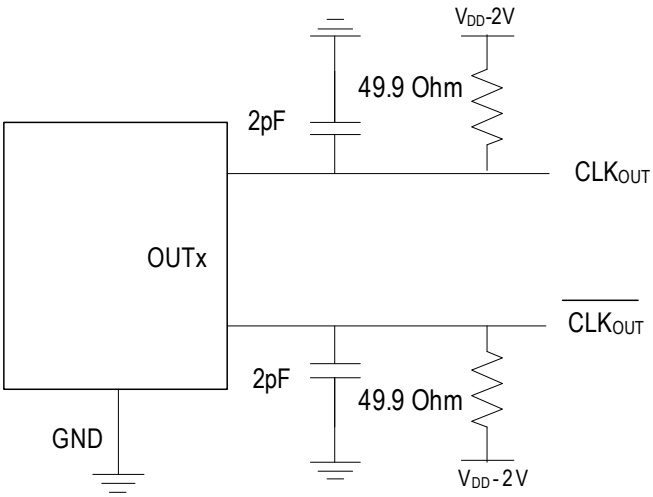
Other Termination Scheme (Block Diagrams)



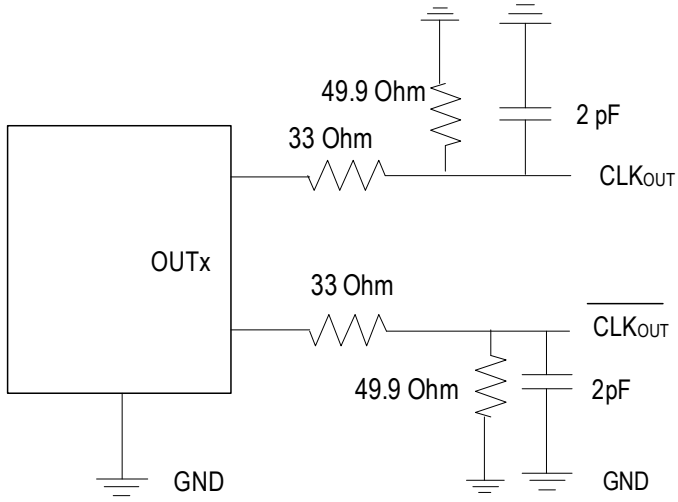
LVTTL: 5pF for each output



LVDS: 100 Ohm between differential outputs



LVPECL



HCSL

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available.

Marking Diagram

- Lines 1 and 2 indicate the part number.
- Line 3 indicates the following:
  - "YY" is the last two digits of the year; "WW" is the work week number when the part was assembled.
  - "$" denotes the mark code.
- "LOT" denotes the sequential lot number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
5V49EE902-255NLGI	5.0 × 5.0 × 0.9 mm, 32-VFQFPN	Tray	-40° to +85°C
5V49EE902-255NLGI8	5.0 × 5.0 × 0.9 mm, 32-VFQFPN	Tape and Reel	-40° to +85°C

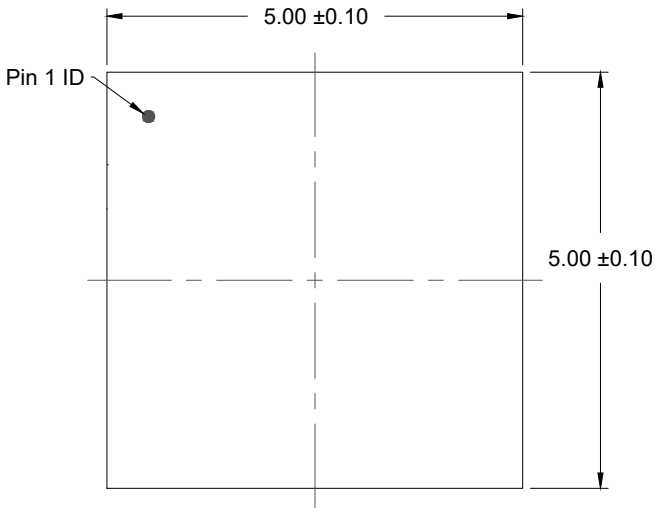
"G" after the two-letter package code denotes Pb-free, RoHS compliant.

Revision History

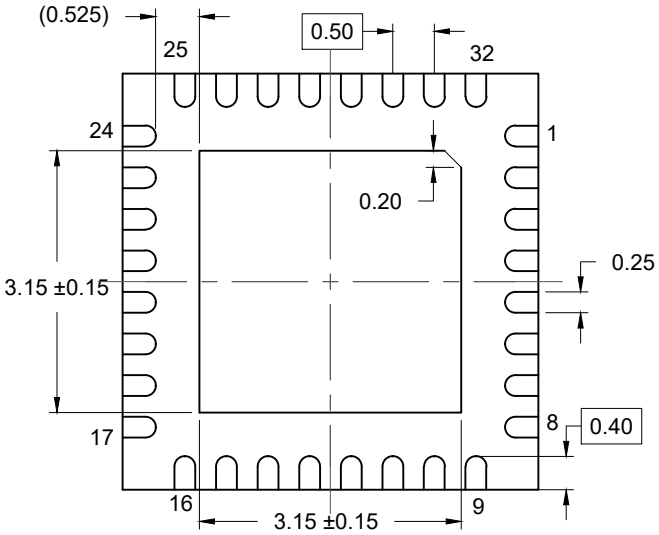
Revision Date	Description of Change
February 7, 2023	Updated POD links in Ordering Information and disclaimer.
November 29, 2018	Updated document to latest format.
October 3, 2018	Initial release.

Package Outline Drawing

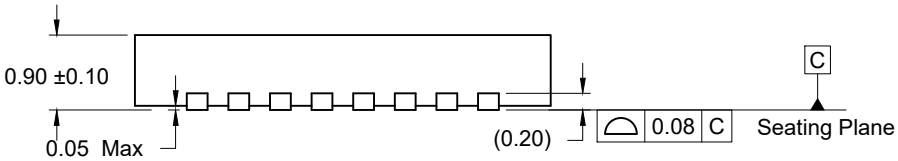
Package Code:NLG32P1
32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4171-01, Revision: 04, Date Created: Aug 15, 2022



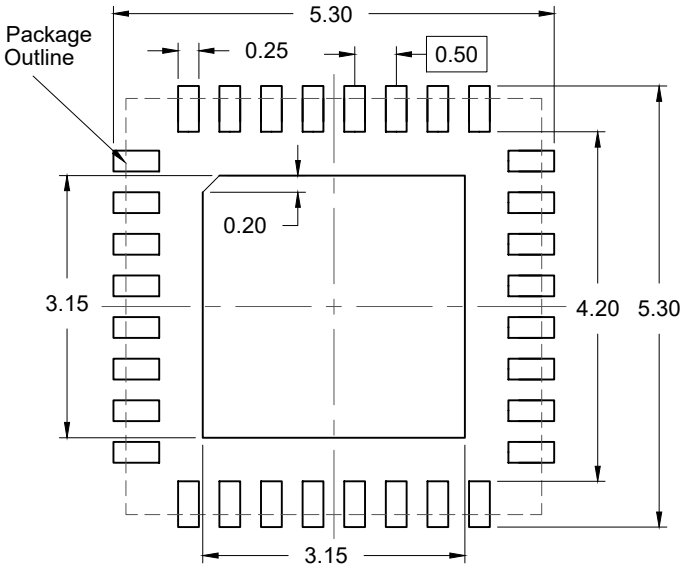
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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