

General Description

The IDT5U49319 is a very low power clock for Freescale MCU's. It uses a 1.5V core and Low-Power HCSL (LP-HCSL) differential outputs for minimal power consumption. The SATA and SRC outputs are PCIe Gen1/2 compatible.

Recommended Application

Clock Chip for Freescale P10xx & P20xx MCU's

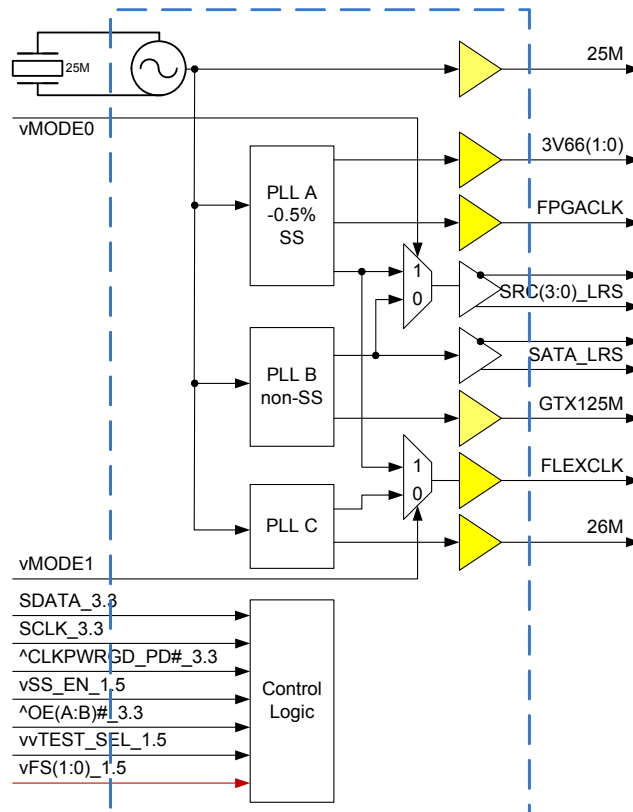
Output Features

- 4 - LP-HCSL SRC pairs w/integrated source terminations
- 1 - LP-HCSL SATA pair w/integrated source terminations
- 1 - 25MHz 2.5V/3.3V LVCMOS output
- 2 - 66.66MHz 3.3V LVCMOS outputs
- 1 - FPGA 33.33MHz 2.5V/3.3V LVCMOS output
- 1 - FLEX clock 2.5V/3.3V LVCMOS output
- 1 - 125M GTX clock 2.5V LVCMOS output
- 1 - 26MHz 2.5V/3.3V LVCMOS output

Key Specifications

- SRC/SATA cycle-to-cycle jitter <85ps
- SRC/SATA PCIe Gen1/2 compliant

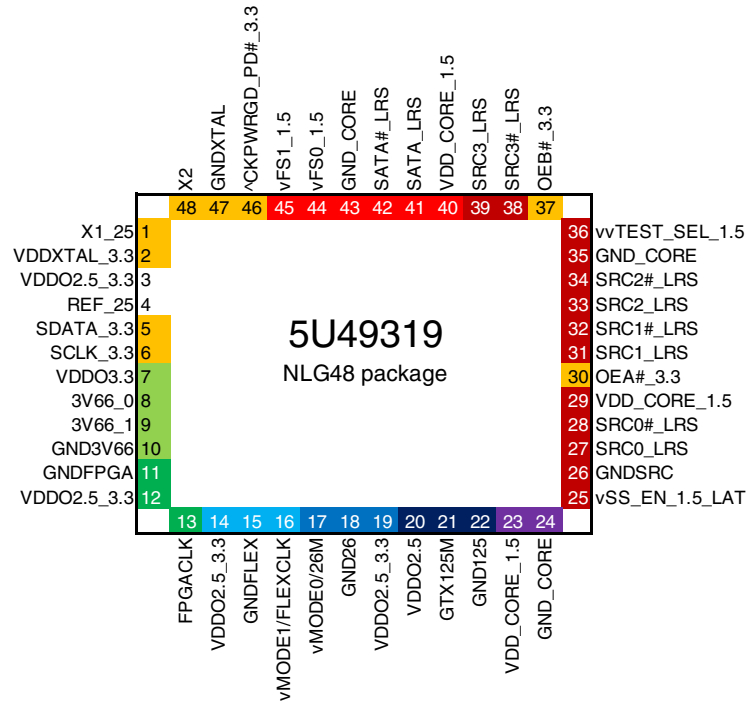
Block Diagram



Features/Benefits

- Various outputs are configurable to run in power down; supports Wake_On_LAN
- FPGA clock frequency is selectable via SMBus; allows low-power system standby
- Strapping pin sources SRC outputs from either spreading or non-spreading PLL; maximum system flexibility
- FLEX clock is pin selectable to be FPGA clock or USB PHY clock; maximum system flexibility
- TEST pin tri-states all outputs; speeds up board test
- External 25MHz crystal; supports tight ppm
- OE# pins; support SRC power management
- Low power differential clock outputs; reduced power and board space
- Differential outputs internally terminated to 100Ω differential impedance; reduced board space
- Space-saving 7x7mm 48-pin VFQFPN with 0.5mm pad pitch; reduced board space without the need for fine pitch assembly techniques

Pin Configuration



48-pin VFQFPN, 7X7 mm, 0.5mm pitch

- v prefix indicates internal 120KOhm pull down resistor
- vv prefix indicates internal 60KOhm pull down resistor
- ^ prefix indicates internal 120KOhm pull up resistor
- Color coding indicates the power domains in the device.

NOTE: ePAD is not electrically connected to the die and should be soldered to PCB Ground plane for specified thermal performance

Singled-ended Output Power Management Table

CKPWRGD_PD#_3.3	SMBus OE bit	SMBus PD# Run bit	REF_25	3V66_(1:0)	FPGACLK	GTX125M
1	Enable	1	Running	Running	Running	Running
1	Enable	0	Running	Running	Running	Running
0	Enable	1	Running	Running	Running	Running
0	Enable	0	Low	Low	Low	Low
X	Disable	X	Low	Low	Low	Low

SRC Power Management Table

CKPWRGD_PD#_3.3	SMBus Register OE	OEA#_3.3	SRC(1:0)_LRS	OEB#_3.3	SRC(3:2)_LRS
			True/Comp		True/Comp
1	Enable	0	Running	0	Running
1	Enable	1	Low/Low	1	Low/Low
0	Enable	X	Low/Low	X	Low/Low
X	Disable	X	Low/Low	X	Low/Low

Note: OEA#_3.3 controls SRC(1:0)_LRS. OEB#_3.3 controls SRC(3:2)_LRS.

SATA Power Management Table

CKPWRGD_PD#_3.3	SMBus Register OE	SATA_LRS True/Comp
1	Enable	Running
0	Enable	Low/Low
X	Disable	Low/Low

Singled-ended Latched I/O and I/O Power Management Table

CKPWRGD_PD#_3.3	SMBus Register OE	SMBus PD# Run bit	FLEXCLK	26M
1	Enable	1	Running	Running
1	Enable	0	Running	Running
1	Disable	X	Low	Low
0	Enable	1	Running	Running
0	Enable	0	Hi-Z	Hi-Z
0	Disable	1	Low	Low
0	Disable	0	Hi-Z	Hi-Z

Note: After power is applied and *before* CKPWRGD_PD#_3.3 is asserted, these outputs are Hi-Z to allow for any pull up or pull down to be latched on the first high assertion of CKPWRGD_PD#_3.3.

Power Connections

Pin Number		Description
VDD	GND	
2	47	XTAL OSC Circuit, SMBus
3	47	REF_25 Output
7	10	3V66 outputs and logic
12	11	FPGACLK output and logic
14	15	FLEXCLK output and logic
19	18	26M output and logic
20	22	GTX125M output and logic
23	24	PLL C Analog
29	26	SRC Outputs
29	35	PLL A Analog
40	43	PLL B Analog and SATA

PLL A Spread Enable/Selection Table

vSS_EN_1.5 (B4b0)	SS1 (B4b2) ¹	SS0 (B4b1) ¹	SPREAD
0	X	X	OFF
1	0	0	-0.50%
1	0	1	-0.40%
1	1	0	-0.30%
1	1	1	0.00%

NOTES:

- Default for SS(1:0) is 00
- Only applies to SRC(3:0)_LRS if vMODE0 = 1

vMODE0 Definition Table

vMODE0	SRC(3:0)_LRS Source
0	Non-spread PLL B
1	Spread-Capable PLL A

vMODE1 Defintion Table

vMODE1	vFS1_1.5	vFS0_1.5	FLEXCLK Source	FLEXCLK Frequency (MHz)
0	0	0	PLL C	30.00
0	0	1	PLL C	48.00
0	1	0	PLL C	24.00
0	1	1	PLL C	12.00
1	0	0	PLL A	33.33
1	0	1	PLL A	16.67
1	1	0	PLL A	8.33
1	1	1	PLL A	4.17

FPGACLK Frequency Select Table

FPGA FS1 (B0b3)	FPGA FS0 (B0b2)	FPGACLK Frequency (MHz)
0	0	33.33
0	1	16.67
1	0	8.33
1	1	4.17

Pin Descriptions

Num.	Pin Name	Type	Description
1	X1_25	IN	Crystal input, Nominally 25.00MHz.
2	VDDXTAL_3.3	PWR	Power supply for XTAL, nominal 3.3V
3	VDDO2.5_3.3	PWR	Power supply for outputs, either 2.5V or 3.3V.
4	REF_25	OUT	25 MHz reference clock.
5	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
6	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
7	VDDO3.3	PWR	Power supply for outputs, nominal 3.3V.
8	3V66_0	OUT	3.3V 66.66MHz clock output
9	3V66_1	OUT	3.3V 66.66MHz clock output
10	GND3V66	GND	Ground pin for the 3.3V 66MHz clocks
11	GNDFPGA	GND	Ground pin for the FPGA clock output.
12	VDDO2.5_3.3	PWR	Power supply for outputs, either 2.5V or 3.3V.
13	FPGACLK	OUT	FPGA clock output. See frequency tables for values.
14	VDDO2.5_3.3	PWR	Power supply for outputs, either 2.5V or 3.3V.
15	GNDFLEX	GND	Ground pin for the FLEX clock output.
16	vMODE1/FLEXCLK	LATCHED I/O	Mode Select Pin/FLEX clock output. This pin has an internal pull-down and is latched on the first power up of the device.
17	vMODE0/26M	LATCHED I/O	Mode Select Pin/26MHz output. This pin has an internal pull-down and is latched on the first power up of the device.
18	GND26	GND	Ground pin for the 26MHz output.
19	VDDO2.5_3.3	PWR	Power supply for outputs, either 2.5V or 3.3V.
20	VDDO2.5	PWR	Power supply for outputs, nominally 2.5V.
21	GTX125M	OUT	125MHz output
22	GND125	GND	Ground pin for 125M output
23	VDD_CORE_1.5	PWR	Power for PLL core components requiring 1.5V
24	GND_CORE	GND	Ground pin for the PLL core.
25	vSS_EN_1.5_LAT	LATCHED IN	1.5V LVCMOS latched input to select spread spectrum amount: 1 = -0.5% spread, 0 = Spread Off
26	GNDSRC	GND	Ground pin for the SRC outputs
27	SRC0_LRS	OUT	True clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
28	SRC0#_LRS	OUT	Complementary clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
29	VDD_CORE_1.5	PWR	Power for PLL core components requiring 1.5V
30	OEA#_3.3	IN	Active low input 3.3V tolerant for enabling output bank A. 1 = disable output, 0 = enable output
31	SRC1_LRS	OUT	True clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
32	SRC1#_LRS	OUT	Complementary clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
33	SRC2_LRS	OUT	True clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
34	SRC2#_LRS	OUT	Complementary clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
35	GND_CORE	GND	Ground pin for the PLL core.
36	vvTEST_SEL_1.5	LATCHED IN	TEST_SEL: latched input to select TEST MODE. Max input voltage is 1.5V 1 = All outputs are tri-stated for test 0 = All outputs behave normally.
37	OEB#_3.3	IN	Active low input 3.3V tolerant for enabling output bank B. 1 = disable output, 0 = enable output
38	SRC3#_LRS	OUT	Complementary clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.

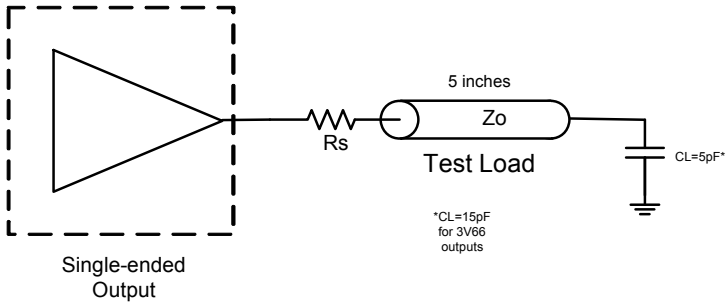
Pin Descriptions (cont.)

Num.	Pin Name	Type	Description
39	SRC3_LRS	OUT	True clock of LP-HCSL SRC clock with integrated source termination. See Differential Test Load for output impedance.
40	VDD_CORE_1.5	PWR	Power for PLL core components requiring 1.5V
41	SATA_LRS	OUT	True clock of LP-HCSL SATA clock with integrated source termination. See Differential Test Load for output impedance.
42	SATA#_LRS	OUT	Complementary clock of LP-HCSL SATA clock with integrated source termination. See Differential Test Load for output impedance.
43	GND_CORE	GND	Ground pin for the PLL core.
44	vFS0_1.5	LATCHED IN	1.5V latched input pin for frequency selection. See Frequency Select Tables for Details. This pin has an internal pull down.
45	vFS1_1.5	LATCHED IN	1.5V latched input pin for frequency selection. See Frequency Select Tables for Details. This pin has an internal pull down.
46	^CKPWRGD_PD#_3.3	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor and is 3.3V tolerant.
47	GNDXTAL	GND	GND for XTAL
48	X2	OUT	Crystal output.

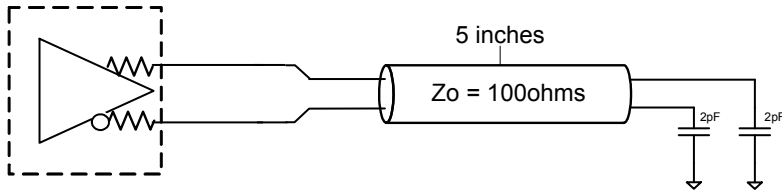
Test Loads

Rs for Single-Ended Outputs Driving Test Loads

Output	Number of Loads	Rs
All except GTX125M	1	33Ω
GTX125M	1	23Ω

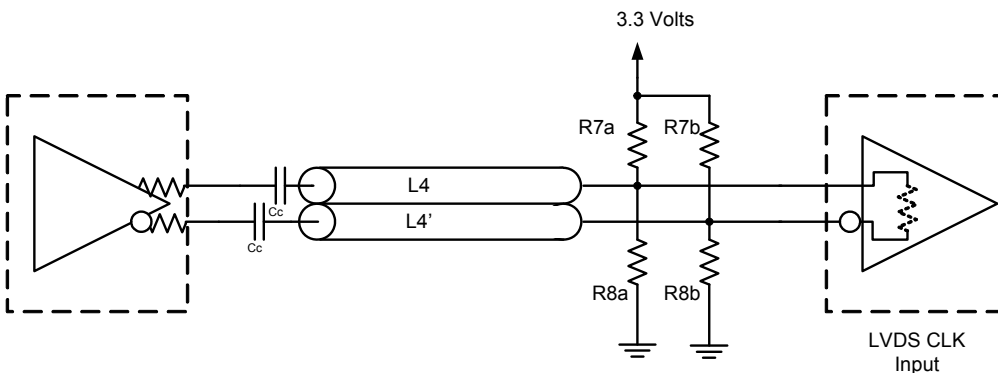


Differential Test Load



Driving LVDS inputs

Component	Value		Note
	Receiver has termination	Receiver does not have termination	
R7a, R7b	10K ohm	140 ohm	
R8a, R8b	5.6K ohm	75 ohm	
Cc	0.1 uF	0.1 uF	
Vcm	1.2 volts	1.2 volts	



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5U49319. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxx_3.3	Supply Voltage			4.6	V	1
Maximum Supply Voltage	VDD_CORE_1.5	Supply Voltage			1.9	V	1
Maximum Supply Voltage	VDDO2.5_3.3	Supply Voltage			4.6	V	1
Maximum Input Voltage	V _{IH}	3.3V Inputs, including SMBus			4.6	V	1,2
Minimum Input Voltage	V _{IL}	Any Input	GND - 0.5			V	1
Storage Temperature	T _s	-	-65		150	°C	
Junction Temperature	T _j	-			125	°C	
Input ESD protection	ESD prot	Human Body Model	2000			V	

NOTES on Absolute Max Parameters

¹ Operation under these conditions is neither implied, nor guaranteed.

² Maximum V_{IH} is not to exceed VDD

AC Electrical Characteristics—SRCx_LRS, SATA_LRS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f			100.00		MHz	2,3
Synthesis error	ppm _{SSoff}	SRC/SATA	0			ppm	1,2,6
	ppm _{SSon}	SRC @ -0.5% spread	-150			ppm	1,2
Rising/Falling Edge Slew Rate	t _{SLEW}	B11[7:6] = '11', Dif. Measurement	2.0	3.1	4.0	V/ns	1,2
		B11[7:6] = '00', Dif. Measurement	1.5	2.4	3.0	V/ns	1,2
Slew Rate Variation	t _{SLVAR}	Single-ended Measurement		9	20	%	1
Maximum Output Voltage	V _{HIGH}	Includes overshoot		812	1150	mV	1
Minimum Output Voltage	V _{LOW}	Includes undershoot	-300	-23		mV	1
Differential Voltage Swing	V _{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V _{XABS}	Single-ended Measurement	300	377	550	mV	1,3,4
Crossing Point Variation	V _{XABSVAR}	Single-ended Measurement		20	140	mV	1,3,5
Duty Cycle	DCYC	Differential Measurement	45	49.0	55	%	1
SRC Jitter - Cycle to Cycle	SRC _{JC2C}	Differential Measurement		21	85	ps	1
SATA Jitter - Cycle to Cycle	SATA _{JC2C}	Differential Measurement		22	85	ps	1
SRC[2:3] Skew	SKEW _{SRC23}	Differential Measurement		16	50	ps	1
SRC[0:1] Skew	SKEW _{SRC01}	Differential Measurement		8	50	ps	1

Notes:

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF_25 is at 25MHz

³ Slew rate measured through V_{swing} voltage range centered about differential zero

⁴ V_{cross} is defined at the voltage where Clock = Clock#.

⁵ Only applies to the differential rising edge (Clock rising, Clock# falling.)

⁶ At default SMBus settings.

Electrical Characteristics—Input/Supply/Common Output DC Parameters

$T_{AMB} = 0 - 70^{\circ}\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDCORE} = 1.5\text{ V} \pm 5\%$, $V_{DDO2.5_3.3} = 2.5\text{--}3.3\text{ V} \pm 5\%$; All outputs driving test loads (unless noted otherwise).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	T_{AMB}	-	0	25	70	$^{\circ}\text{C}$	
Supply Voltage	VDDxx_3.3	Supply Voltage	3.135	3.3	3.465	V	
	VDD_CORE_1.5	Supply Voltage	1.425	1.5	1.575	V	
	VDDO_2.5_3.3	Supply Voltage	2.375	2.5	3.465	V	
Input High Voltage	$V_{IHSE_3.3}$	Single-ended 3.3V inputs	2.1		$V_{DD} + 0.3$	V	3
Input Low Voltage	$V_{ILSE_3.3}$	Single-ended 3.3V inputs	$V_{SS} - 0.3$		0.8	V	3
Latched Input High Voltage	V_{IH_LI}	Single-ended Latched Inputs	2.1		$V_{DD} + 0.3$	V	
Latched Input Low Voltage	V_{IL_LI}	Single-ended Latched Inputs	$V_{SS} - 0.3$		0.8	V	
Low Voltage Latched Input-High Voltage	V_{IH_FS}	Low Voltage inputs (xx_1.5)	1.2		$V_{DD_CORE} + 0.3$	V	
Low Voltage Latched Input-Low Voltage	V_{IL_FS}	Low Voltage inputs (xx_1.5)	$V_{SS} - 0.3$		0.4	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, $V_{IN} = \text{GND}$	-5		5	μA	2
Operating Supply Current	$I_{DDOP3.3}$	IDDxx_3.3		26	31	mA	
	$I_{DDOP1.5}$	IDD_CORE_1.5		33	40	mA	
	$I_{DDO2.5_3.3}$	IDDO_2.5_3.3		17	21	mA	
Powerdown Current (PD# RUN disabled)	$I_{DDPD3.3}$	PD# = 0, IDDxx_3.3		0.5	1	mA	5
	$I_{DDPD1.5}$	PD# = 0, IDD_CORE_1.5		0.4	1	mA	5
	$I_{DDPDO2.5_3.3}$	PD# = 0, IDDO2.5_3.3 Rails		0.1	1	mA	5
Standby Current (PD# RUN enabled, all runnable outputs running)	$I_{DDPDRUN3.3}$	PD# = 0, IDDxx_3.3		27	32	mA	6
	$I_{DDPDRUN1.5}$	PD# = 0, IDD_CORE_1.5		16	19	mA	6
	$I_{DDRUNO2.5_3.3}$	PD# = 0, IDDO_2.5_3.3		17	21	mA	6
Input Frequency	F_I		23	25	27	MHz	4
Pin Inductance	L_{pin}			5	7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5	3	5	pF	
	C_{OUT}	Output pin capacitance		5	6	pF	
	C_{INX}	X1 & X2 pins		5	6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		1.1	1.8	ms	
$T_{stop_OE_off}$	T_{OE_OFF}	Output stop after OEx#_3.3 deasserted	1	2	3	Clocks	
$T_{run_OE_on}$	T_{OE_ON}	Output run after OEx#_3.3 asserted	1	2	3	Clocks	
T_{fall_SE}	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	1
T_{rise_SE}	T_{RISE}				10	ns	1
SMBus Voltage	V_{DD}		2.7		3.3	V	
Low-level Output Voltage	V_{OL_SMB}	@ I_{PULLUP}			0.4	V	
Current sinking at $V_{OL_SMB} = 0.4\text{ V}$	I_{PULLUP}	SMB Data Pin	4			mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max $V_{IL} - 0.15$) to (Min $V_{IH} + 0.15$)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min $V_{IH} + 0.15$) to (Max $V_{IL} - 0.15$)			300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	31.5	33	kHz	

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Signal is required to be monotonic in this region.

² Input leakage current does not include inputs with pull-up or pull-down resistors

³ 3.3V referenced inputs are: OEx#_3.3, SCLK, SDATA, and CLKPWRGD_PD_3.3#

⁴ For margining purposes only. Normal operation should have $F_{in} = 25\text{MHz}$

⁵ Standard powerdown with Byte 1, bit 7 = 0

⁶ Powerdown with Byte 1, bit 7 = 1 (default).

Electrical Characteristics—Phase Jitter, SRC_LRS, SATA_LRS outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY SPEC LIMIT	UNITS	NOTES
Jitter, Phase	$t_{jphPCIe1}$	PCIe Gen 1 REFCLK phase jitter		31	48	86	ps	1,2,3
	$t_{jphPCIe2Lo}$	PCIe Gen 2 REFCLK phase jitter Lo-band content		1.0	1.2	3	ps (RMS)	1,2,3
	$t_{jphPCIe2Hi}$	PCIe Gen 2 REFCLK phase jitter Hi-band content		2.1	2.4	3.1	ps (RMS)	1,2,3

Notes on Phase Jitter:

¹ See <http://www.pcisig.com> for complete specs. Guaranteed by design and characterization, not tested in production.

² Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1^{-12}

³ Applies to SRC and SATA outputs.

Electrical Characteristics—REF_25

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f			25.00		MHz	2,3
Crystal Frequency Error	ppm	Including all aging and tuning effects	-50		50	ppm	1,2
Output High Voltage	V_{OH}	VDDO = 3.3V, I_{OH} = -1 mA	2.2			V	1
Output Low Voltage	V_{OL}	VDDO = 3.3V, I_{OL} = 1 mA			0.4	V	1
Output High Voltage	V_{OH}	VDDO = 2.5V, I_{OH} = -100 μ A	2.2			V	1
Output Low Voltage	V_{OL}	VDDO = 2.5V, I_{OL} = 100 μ A			0.4	V	1
Slew Rate VDDO = 2.5V	t_{SLEW00}	'00' Slowest Slew Rate	0.5	1.2	2.1	V/ns	1,3,4
	t_{SLEW01}	'01' Slow Slew Rate	0.7	1.6	2.5	V/ns	1,3,4
	t_{SLEW10}	'10' Fast Slew Rate	0.8	1.7	2.7	V/ns	1,3,4
	t_{SLEW11}	'11' Fastest Slew Rate	0.9	1.8	2.8	V/ns	1,3,4
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' Slowest Slew Rate	0.9	1.7	2.6	V/ns	1,3,4
	t_{SLEW01}	'01' Slow Slew Rate	1.1	2.2	3.3	V/ns	1,3,4
	t_{SLEW10}	'10' Fast Slew Rate	1.3	2.3	3.5	V/ns	1,3,4
	t_{SLEW11}	'11' Fastest Slew Rate	1.5	2.6	4	V/ns	1,3,4
Duty Cycle	d_{t1}	VT = VDDO/2	40	50.3	60	%	1
Pin to Pin Skew	t_{skew}	VT = VDDO/2		n/a		ps	1
Jitter, Peak period jitter	t_{jpeak}	VT = VDDO/2		64	\pm 150	ps	1

Electrical Characteristics—3V66

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f			66.66		MHz	2,3
Synthesis error	ppm _{SSoff}	Spread off		0		ppm	1,2,5
	ppm _{SSon}	Spread on		-150		ppm	1,2,5
Output High Voltage	V_{OH}	VDDO = 3.3V, I_{OH} = -1 mA	2.2			V	1
Output Low Voltage	V_{OL}	VDDO = 3.3V, I_{OL} = 1 mA			0.4	V	1
Slew Rate VDDO = 3.3V	t_{SLEW00}	'00' Slowest Slew Rate	1.3	2.1	3	V/ns	1,3,4
	t_{SLEW01}	'01' Slow Slew Rate	1.5	2.3	3.2	V/ns	1,3,4
	t_{SLEW10}	'10' Fast Slew Rate	1.7	2.4	3.4	V/ns	1,3,4
	t_{SLEW11}	'11' Fastest Slew Rate	1.9	2.6	3.9	V/ns	1,3,4
Duty Cycle	d_{t1}	VT = VDDO/2	40	48.2	60	%	1
Pin to Pin Skew	t_{skew}	VT = VDDO/2		69.5	120	ps	1
Jitter, Peak period jitter	t_{jpeak}	VT = VDDO/2, SS off		53.6	\pm 150	ps	1
Jitter, Cycle to cycle	$t_{jcc-cyc}$	VT = VDDO/2		68	100	ps	1

Electrical Characteristics–FPGACLK

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f	FS(1:0) = 00		33.33		MHz	2,3
		FS(1:0) = 01		16.67		MHz	2,3
		FS(1:0) = 10		8.33		MHz	2,3
		FS(1:0) = 11		4.17		MHz	2,3
Synthesis error	ppm _{SSoff}	Spread off		0		ppm	1,2,5
	ppm _{SSon}	Spread on		-150		ppm	1,2,5
Output High Voltage	V _{OH}	VDDO = 3.3V, I _{OH} = -1 mA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 3.3V, I _{OL} = 1 mA			0.4	V	1
Output High Voltage	V _{OH}	VDDO = 2.5V, I _{OH} = -100 μA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 2.5V, I _{OL} = 100 μA			0.4	V	1
Slew Rate VDDO = 2.5V	t _{SLEW00}	'00' Slowest Slew Rate	0.5	1.1	1.9	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	0.7	1.4	2.3	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	0.8	1.6	2.4	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	0.9	1.7	2.5	V/ns	1,3,4
Slew Rate VDDO = 3.3V	t _{SLEW00}	'00' Slowest Slew Rate	1	1.6	2.3	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	1.4	2.1	3.1	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	1.5	2.3	3.4	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	1.6	2.6	3.8	V/ns	1,3,4
Duty Cycle	d _{t1}	VT = VDDO/2	40	49.2	60	%	1
Pin to Pin Skew	t _{skew}	VT = VDDO/2		n/a		ps	1
Jitter, Peak period jitter	t _{jpeak}	VT = VDDO/2, SS off		32	±150	ps	1
Jitter, Cycle to cycle	t _{jcy-c-cyc}	VT = VDDO/2		45	100	ps	1

Electrical Characteristics–FLEXCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency MODE1 = 0	f	FS(1:0)_1.5 = 00		30.00		MHz	2,3
		FS(1:0)_1.5 = 01		48.00		MHz	2,3
		FS(1:0)_1.5 = 10		24.00		MHz	2,3
		FS(1:0)_1.5 = 11		12.00		MHz	2,3
Clock Frequency MODE1 = 1	f	FS(1:0)_1.5 = 00		33.33		MHz	2,3
		FS(1:0)_1.5 = 01		16.67		MHz	2,3
		FS(1:0)_1.5 = 10		8.33		MHz	2,3
		FS(1:0)_1.5 = 11		4.167		MHz	2,3
Synthesis error	ppm _{SSoff}	MODE0 or MODE1 with SS/off		0		ppm	1,2,5
	ppm _{SSon}	MODE1 with SS/on		-150		ppm	1,2,5
Output High Voltage	V _{OH}	VDDO = 3.3V, I _{OH} = -1 mA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 3.3V, I _{OL} = 1 mA			0.4	V	1
Output High Voltage	V _{OH}	VDDO = 2.5V, I _{OH} = -100 μA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 2.5V, I _{OL} = 100 μA			0.4	V	1
Slew Rate VDDO = 2.5V	t _{SLEW00}	'00' Slowest Slew Rate	0.5	1.2	2.2	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	0.7	1.6	2.6	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	0.8	1.7	2.7	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	1	1.9	2.8	V/ns	1,3,4
Slew Rate VDDO = 3.3V	t _{SLEW00}	'00' Slowest Slew Rate	1	1.8	2.7	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	1.5	2.3	3.2	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	1.7	2.5	3.5	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	1.8	2.8	3.9	V/ns	1,3,4
Duty Cycle	d _{t1}	VT = VDDO/2	40	49.2	60	%	1
Pin to Pin Skew	t _{skew}	VT = VDDO/2		n/a		ps	1
Jitter, Peak period jitter	t _{jpeak}	VT = VDDO/2		34	±150	ps	1
Jitter, Cycle to cycle	t _{jcy-c-cyc}	VT = VDDO/2		52	100	ps	1

Electrical Characteristics–26M

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f			26.00		MHz	2,3
Synthesis error	ppm			0		ppm	1,2,5
Output High Voltage	V _{OH}	VDDO = 3.3V, I _{OH} = -1 mA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 3.3V, I _{OL} = 1 mA			0.4	V	1
Output High Voltage	V _{OH}	VDDO = 2.5V, I _{OH} = -100 μA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 2.5V, I _{OL} = 100 μA			0.4	V	1
Slew Rate VDDO = 2.5V	t _{SLEW00}	'00' Slowest Slew Rate	0.5	1.2	2.2	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	0.7	1.6	2.7	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	0.8	1.8	2.8	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	0.9	1.9	2.9	V/ns	1,3,4
Slew Rate VDDO = 3.3V	t _{SLEW00}	'00' Slowest Slew Rate	1	1.5	2.8	V/ns	1,3,4
	t _{SLEW01}	'01' Slow Slew Rate	1.3	1.9	3.3	V/ns	1,3,4
	t _{SLEW10}	'10' Fast Slew Rate	1.4	2.0	3.6	V/ns	1,3,4
	t _{SLEW11}	'11' Fastest Slew Rate	1.6	2.2	4	V/ns	1,3,4
Duty Cycle	d _{t1}	VT = VDDO/2	40	49.2	60	%	1
Pin to Pin Skew	t _{skew}	VT = VDDO/2		n/a		ps	1
Jitter, Long Term	t _{TIE}	TIE over any 10us interval, V _T = VDDO/2		0.6	1	ns	1
Jitter, Cycle to cycle	t _{JCYC-CYC}	VT = VDDO/2		79	200	ps	1

Electrical Characteristics–GTX125M

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Clock frequency	f			125.00		ns	2,3
Synthesis error	ppm			0		ppm	1,2,5
Output High Voltage	V _{OH}	VDDO = 2.5V, I _{OH} = -100 μA	2.2			V	1
Output Low Voltage	V _{OL}	VDDO = 2.5V, I _{OL} = 100 μA			0.3	V	1
Slew Rate VDDO = 2.5V	t _{SLEW}	Measured between 0.7V and 1.7 V	1.5	2.1	3	V/ns	1,6
Duty Cycle	d _{t1}	VT = VDDO/2	47	50	53	%	1
Pin to Pin Skew	t _{skew}	VT = VDDO/2		n/a		ps	1
Jitter, Peak period jitter	t _{Jpeak}	VT = VDDO/2		56	±150	ps	1

Notes for single-ended outputs

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Frequency specifications are guaranteed assuming that REF_25 is at 25MHz

³ At default SMBus settings

⁴ 0.8V and 2.0V thresholds.

⁵ This is the frequency error with respect to the crystal frequency. If the crystal is +25ppm, an output with 0ppm synthesis error will be +25ppm, too.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
		ACK
Data Byte Count = X		ACK
Beginning Byte N		ACK
O	X Byte	O
O		O
O		O
Byte N + X - 1		ACK
P	stoP bit	

Note: SMBUS address = C2/C3

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
		ACK
RT	Repeat starT	
Slave Address		
RD	ReaD	
		ACK
ACK		Data Byte Count=X
		Beginning Byte N
O	X Byte	O
O		O
O		O
O		O
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

SMBus Table: Frequency Select and MODE Readback Registers

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	FS1_1.5	Frequency Select Readback	R	See Table 3		Latch w/pd
Bit 6	FS0_1.5	Frequency Select Readback	R			Latch w/pd
Bit 5	MODE1	Mode 1 Readback	R			Latch w/pd
Bit 4	MODE0	Mode 0 Readback	R	See Table 2		Latch w/pd
Bit 3	FPGA FS1	FPGACLK Freq. Select	RW	See Table 4.		0
Bit 2	FPGA FS0	FPGACLK Freq. Select	RW			0
Bit 1	Reserved					0
Bit 0	Power Down Configuration	Forces "cold" start during assertion of PD#	RW	Resets Smbus registers to Power up Default and Relatches All Latched inputs.	Normal PD# mode, all SMBus values are maintained as long as power rails are maintained.	1

Notes:

1. Latch w/pd means an input latched on first assertion of CKPWRGD pin that also has an internal pull down.
2. Byte 0, bit 0 must only be set to 0 in conjunction with Byte 1, bit 7 set to 0.

SMBus Table: PD# Run Mode Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PD# RUN EN	Enables PD# Run Funct.	RW	No outputs run in PD#	PD# Run Enabled	1
Bit 6	REF_25 RUN	REF_25 Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 5	3V66_1 RUN	3V66_1 Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 4	3V66_0 RUN	3V66_0 Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 3	FPGACLK RUN	FPGACLK Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 2	GTX125M RUN	GTX125M Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 1	FLEXCLK RUN	FLEXCLK Runs in PD#	RW	Does not run in PD#	Runs in PD#	1
Bit 0	26M RUN	26M Runs in PD#	RW	Does not run in PD#	Runs in PD#	1

SMBus Table: Output Enable Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	REF_25 OE	Output Enable	RW	Disable	Enable	1
Bit 6	FLEXCLK OE	Output Enable	RW	Disable	Enable	1
Bit 5	Reserved					1
Bit 4	FPGACLK OE	Output Enable	RW	Disable	Enable	1
Bit 3	26M OE	Output Enable	RW	Disable	Enable	1
Bit 2	3V66_1 OE	Output Enable	RW	Disable	Enable	1
Bit 1	3V66_0 OE	Output Enable	RW	Disable	Enable	1
Bit 0	GTX125M	Output Enable	RW	Disable	Enable	1

SMBus Table: Output Enable Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					1
Bit 4	SRC3 OE	Output Enable	RW	Disable	Enable	1
Bit 3	SRC2 OE	Output Enable	RW	Disable	Enable	1
Bit 2	SRC1 OE	Output Enable	RW	Disable	Enable	1
Bit 1	SRC0 OE	Output Enable	RW	Disable	Enable	1
Bit 0	SATA OE	Output Enable	RW	Disable	Enable	1

SMBus Table: Spread Control Register

Byte 4	Name	Control Function		0	1	Default
Bit 7		Reserved				1
Bit 6		Reserved				1
Bit 5		Reserved				1
Bit 4		Reserved				1
Bit 3		Reserved				1
Bit 2	SS1	PLL A Spread Amount	RW	See Table 1		0
Bit 1	SS0	PLL A Spread Amount	RW	See Table 1		0
Bit 0	SS_EN_1.5	PLL A Spread Enable	RW	Spread OFF	Spread ON	Latch input w/pd

SMBus Table: Output Voltage Override Register

Byte 5	Name	Control Function		0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4	V Detect Override	En. SW Override of HW V Detect	RW	Hardware Detect	Software Override	0
Bit 3	26M V Set	26M VDDO Override	RW	3.3V	2.5V	0
Bit 2	FLEXCLK V Set	FLEXCLK VDDO Override	RW	3.3V	2.5V	0
Bit 1	FPGACLK V Set	FPGACLK VDDO Override	RW	3.3V	2.5V	0
Bit 0	REF_25 V Set	REF_25 VDDO Override	RW	3.3V	2.5V	0

SMBus Table: Output Voltage Detect Readback Register

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4		Reserved				1
Bit 3	26M V Detect	26M VDDO Detect	R	3.3V	2.5V	Latch
Bit 2	FLEXCLK V Detect	FLEXCLK VDDO Detect	R	3.3V	2.5V	Latch
Bit 1	FPGACLK V Detect	FPGACLK VDDO Detect	R	3.3V	2.5V	Latch
Bit 0	REF_25 V Detect	REF_25 VDDO Detect	R	3.3V	2.5V	Latch

SMBus Table: Revision and Vendor ID Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = ICS/IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Reserved Register

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7		Reserved				0
Bit 6		Reserved				0
Bit 5		Reserved				0
Bit 4		Reserved				0
Bit 3		Reserved				0
Bit 2		Reserved				0
Bit 1		Reserved				0
Bit 0		Reserved				0

SMBus Table: Byte Count Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is 0A = 10 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			1
Bit 0	BC0		RW			0

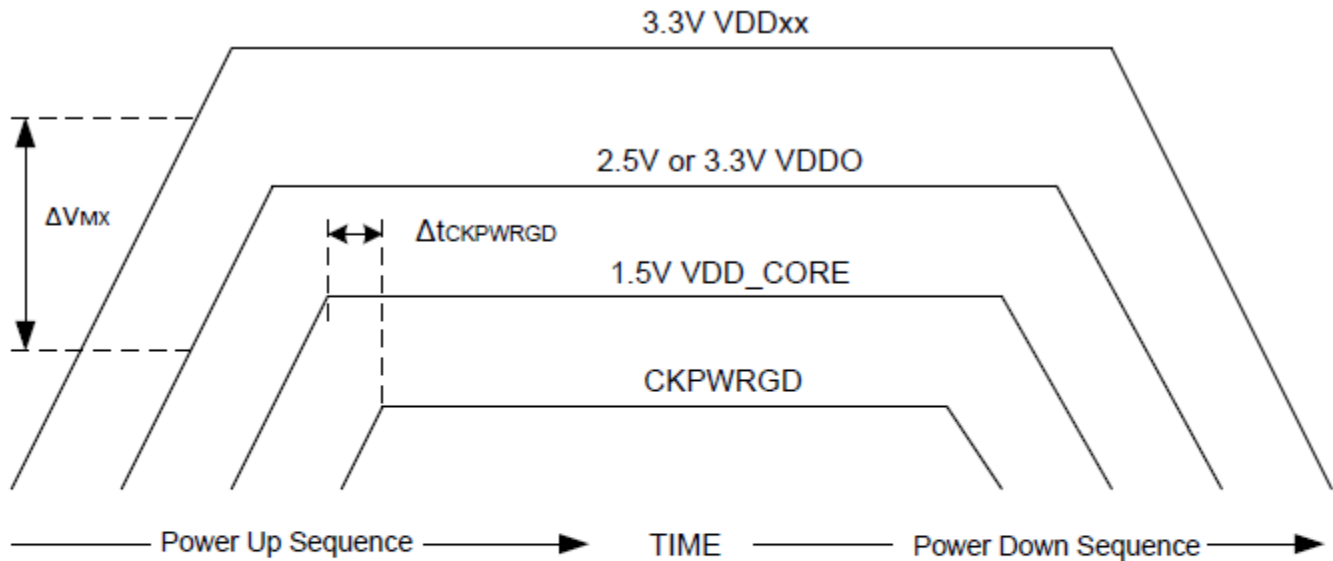
SMBus Table: Slew Rate Control Register

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	26M SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 6			RW	10 = Fast	11 = Fastest	1
Bit 5	REF_25 SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 4			RW	10 = Fast	11 = Fastest	1
Bit 3	FLEXCLK SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 2			RW	10 = Fast	11 = Fastest	1
Bit 1	FPGACK SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 0			RW	10 = Fast	11 = Fastest	1

SMBus Table: Slew Rate Control Register

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	SATA SLEW	Differential Slew Rate	RW	0=Slow	1=Fast	1
Bit 6	SRC SLEW	Differential Slew Rate	RW	0=Slow	1=Fast	1
Bit 5	Reserved					1
Bit 4	Reserved					1
Bit 3	3V66_1 SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 2			RW	10 = Fast	11 = Fastest	0
Bit 1	3V66_0 SLEW	Slew Rate Control	RW	00 = Slowest	01 = Slow	1
Bit 0			RW	10 = Fast	11 = Fastest	0

Power Sequencing



Notes:

1. The maximum difference (ΔV_{MX}) between any two voltages is 0.7V if the lower power supply is powered up first.
2. There are no timing requirements between the higher and lower voltages if the higher voltages power up first.
3. The minimum time before CKPWGRD can be set ($\Delta t_{CKPWGRD} = 0$) is 0 sec from the last power supply that is powered up.

Recommended Crystal Characteristics (3225 package)

PARAMETER	VALUE	UNITS	NOTES
Frequency	25	MHz	1
Resonance Mode	Fundamental	-	1
Frequency Tolerance @ 25°C	±20	PPM Max	1
Frequency Stability, ref @ 25°C Over Operating Temperature Range	±20	PPM Max	1
Temperature Range (commercial)	0~70	°C	1
Temperature Range (industrial)	-40~85	°C	2
Equivalent Series Resistance (ESR)	50	Ω Max	1
Shunt Capacitance (C ₀)	7	pF Max	1
Load Capacitance (C _L)	8	pF Max	1
Drive Level	0.3	mW Max	1
Aging per year	±5	PPM Max	1

Notes:

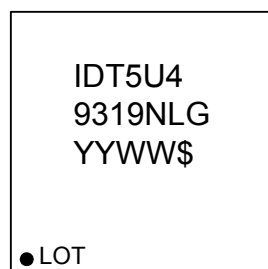
1. IDT 603-25-150JA4C or FOX 603-25-150 .
2. For I-temp, IDT 603-25-150JA4I or FOX 603-25-261.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP.	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG48	19	°C/W	1
	θ_{Jb}	Junction to Base		0.47	°C/W	1
	θ_{JA0}	Junction to Air, still air		30	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		23.1	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		19.8	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		18.5	°C/W	1

¹ePad soldered to board

Marking Diagram

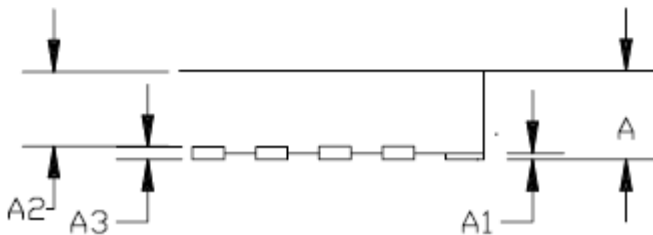
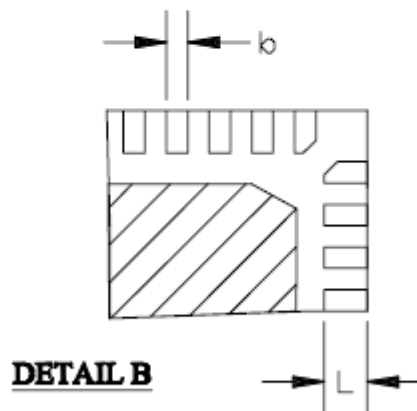
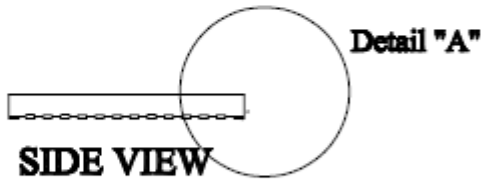
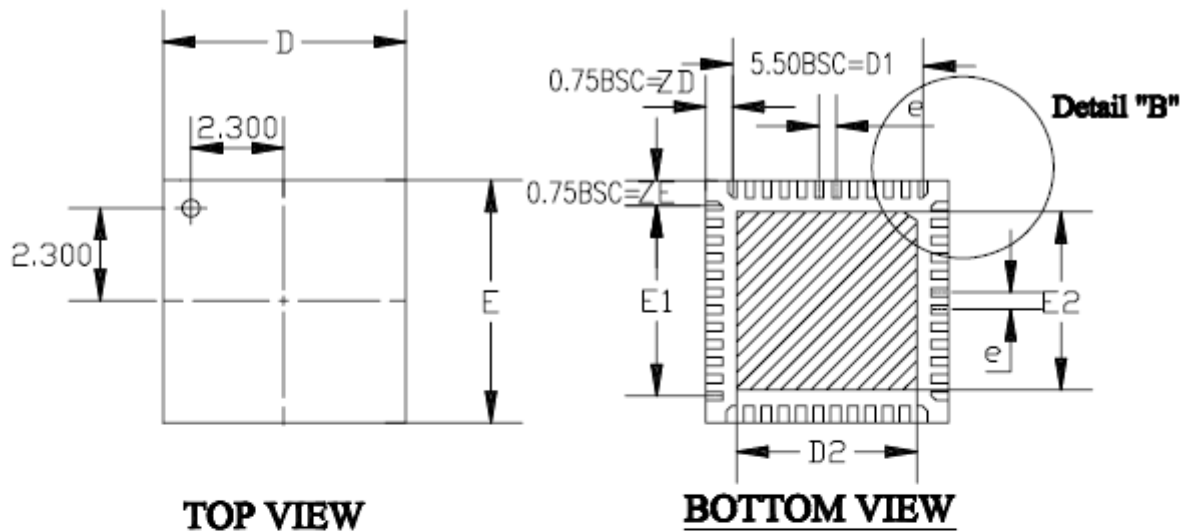


Notes:

1. 'G' after the two-letter package code denotes RoHS compliant package.
2. 'YYWW' is the last two digits of the year and week that the part was assembled.
3. '\$' denotes assembly mark code.
4. 'LOT' is the lot number.

Package Outline and Package Dimensions (NLG48)

(IDT PSC-4203-02, Options P1 and Z1)



DETAIL A

EPAD OPTION:

SYMBOL	P1		
	MIN	NOM	MAX
D2	5.50	5.65	5.80
E2	5.50	5.65	5.80

LEAD OPTION:

SYMBOL	Z1		
	MIN	NOM	MAX
L	0.35	0.40	0.45
L1			
L2			

COMMON DIMENSION

SYMBOL	DIMENSION		
D	7.00 BSC		
E	7.00 BSC		
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
L	SEE LEAD OPTION		
e	0.50 BSC		
N	48		
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.2 REF		
b	0.18	0.25	0.30

Ordering Information

Part	Order Number	Shipping Packaging	Package	Temperature
5U49319NLG	5U49319NLG	Trays	48-pin VFQFPN	0 to +70° C
5U49319NLG8	5U49319NLG8	Tape and Reel	48-pin VFQFPN	0 to +70° C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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Revision History

Rev.	Issue Date	Initiator	Description	Page #
A	10/24/2013	RDW	Initial release	
B	11/1/2013	RDW	Corrected Power Connections table which had pin 14/15 swapped.	3
C	11/8/2013	RDW	Change color coding for pins 14-16 and 17-19 to indicate they are separate power groups.	2
D	4/30/2014	RDW	1. Updated Electrical Tables 2. Move to Final.	

IDT5U49319

VERY LOW POWER CLOCK FOR FREESCALE MCU'S

SYNTHESIZERS

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