LOW SKEW 1 TO 4 CLOCK BUFFER

IDT5T30553

Description

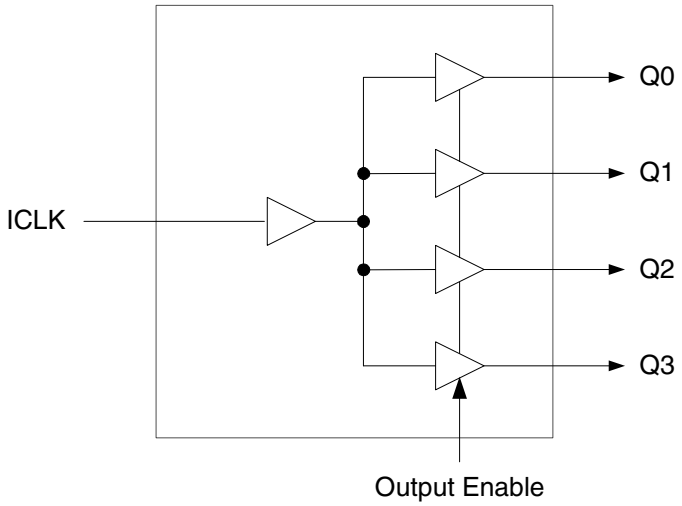
The IDT5T30553 is a low skew, single input to four output, clock buffer.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

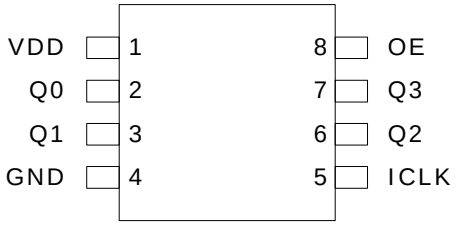
Features

- Extremely low skew outputs (50 ps maximum)
- Packaged in 8-pin SOIC – Pb-free, RoHS compliant
- Low power CMOS technology
- Operating voltages of 2.5 V to 3.3 V
- Output Enable pin tri-states outputs
- Commercial (0 to +70°C) and Industrial (-40°C to +85°C) temperature ranges

Block Diagram



Pin Assignment



8-pin SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to +2.5 V or +3.3 V.
2	Q0	Output	Clock output 0.
3	Q1	Output	Clock output 1.
4	GND	Power	Connect to ground.
5	ICLK	Input	Clock input.
6	Q2	Output	Clock Output 2.
7	Q3	Output	Clock Output 3.
8	OE	Input	Output Enable. Tri-states outputs when low. Connect to VDD for normal operation.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD on pin 1 and GND on pin 4, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the IDT5T30553 is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5T30553. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
Output Enable and All Outputs	-0.5V to VDD+0.5 V
ICLK	-0.5V to VDD+0.5V
Ambient Operating Temperature (industrial)	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+2.375		+3.465	V

DC Electrical Characteristics

VDD=2.5 V ±5%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, OE	V_{IH}		1.8		VDD	V
Input Low Voltage, OE	V_{IL}				0.7	V
Output High Voltage	V_{OH}	I_{OH} = -16 mA	2			V
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.4	V
Operating Supply Current	IDD	No load, 135 MHz		25		mA
Nominal Output Impedance	Z_O			20		Ω
Input Capacitance	C_{IN}	ICLK, OE pin		5		pF
Short Circuit Current	I_{OS}			±28		mA

DC Electrical Characteristics (continued)

VDD=3.3 V ±5% , Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage, OE	V_{IH}		2		VDD	V
Input Low Voltage, OE	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -12 mA	VDD-0.4			V
Operating Supply Current	IDD	No load, 135 MHz		35		mA
Nominal Output Impedance	Z_O			20		Ω
Input Capacitance	C_{IN}	ICLK, OE pin		5		pF
Short Circuit Current	I_{OS}			±50		mA

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

VDD = 2.5 V ±5%, Ambient Temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		1.0	1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		1.0	1.5	ns
Additive Period Jitter					1	ps
Propagation Delay	Note 1		2.2	3	5	ns
Output to Output Skew	Note 2	Rising edges at VDD/2		0	50	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85°C, unless stated otherwise

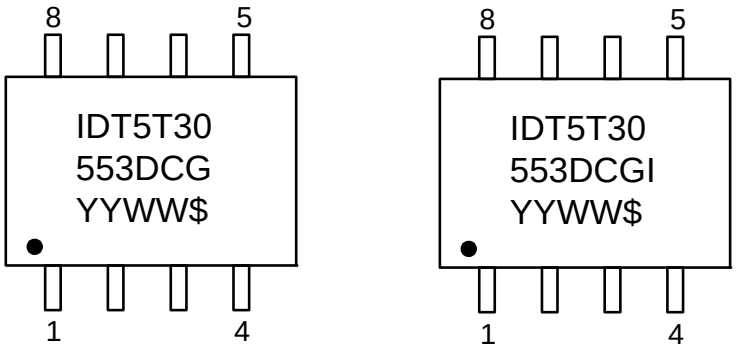
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, C_L=15 pF		0.6	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, C_L=15 pF		0.6	1.0	ns
Propagation Delay	Note 1		2.0	2.4	4	ns
Additive Period Jitter					1	ps
Output to Output Skew	Note 2	Rising edges at VDD/2		0	50	ps
Device to Device Skew		Rising edges at VDD/2			500	ps

Notes: 1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagrams

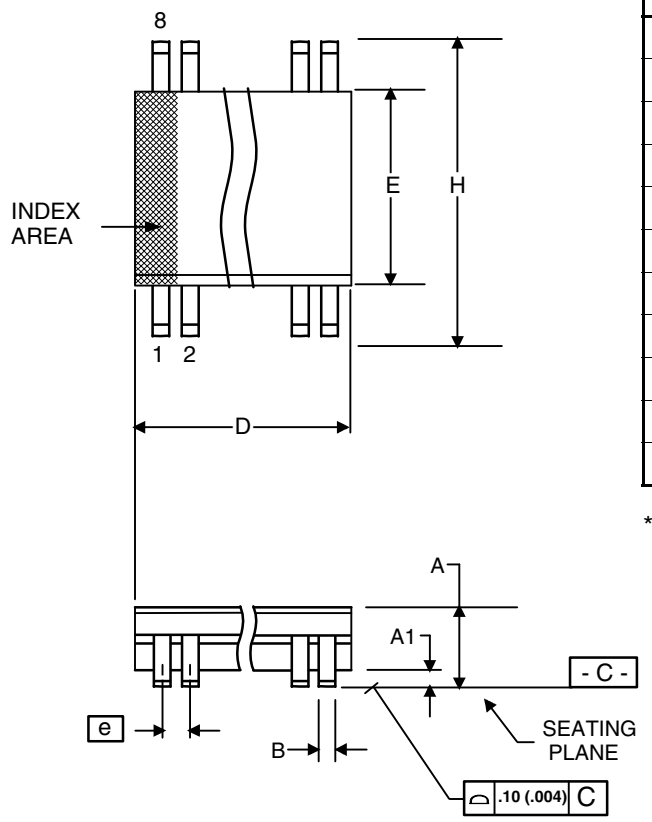


Notes:

1. “$” is the mark code.
2. YYWW is the last two digits of the year and week that the part was assembled.
3 “G” after the two-letter package code denotes RoHS compliant package.
4. “I” denotes industrial temperature range device.
5. Bottom marking: country of origin.

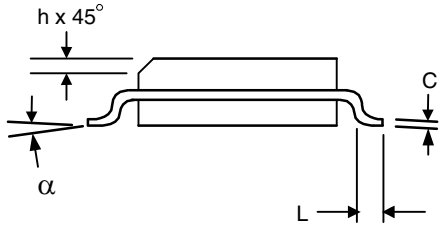
Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5T30553DCG	see page 6	Tubes	8-pin SOIC	0 to +70 °C
5T30553DCG8		Tape and Reel	8-pin SOIC	0 to +70 °C
5T30553DCGI		Tubes	8-pin SOIC	-40 to +85 °C
5T30553DCGI8		Tape and Reel	8-pin SOIC	-40 to +85 °C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

Rev.	Originator	Date	Description of Change
B	P. Keyashian	02/17/09	Added industrial temp ordering information.
C	P. Keyashian	09/02/09	Added “Additive Period Jitter” spec.
D	V. Chaudry	03/22/12	Added marking diagrams and notes
E	A. Tsui	06/21/12	Change Operating Voltage specs from 3.15V Min/3.45V Max to 3.135V Min/3.465V Max
F	S. Sharma	12/10/13	Updated max rating for ICLK voltage to be “-0.5V to VDD+0.5V”

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.