

Description

The ICS553 is a low skew, single input to four output, clock buffer. Part of IDT's ClockBlocks™ family, this is our lowest skew, small clock buffer.

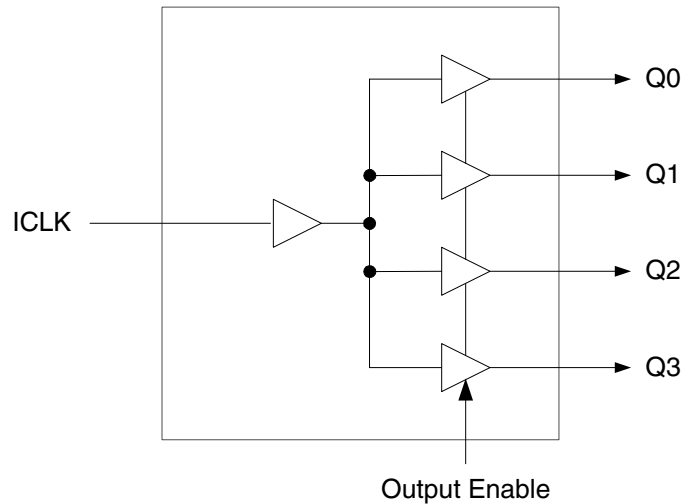
See the ICS552-02 for a 1 to 8 low skew buffer. For more than eight outputs, see the MK74CBxxx Buffalo™ series of clock drivers.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact us for all of your clocking needs.

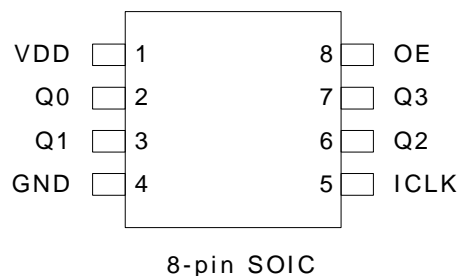
Features

- Extremely low skew outputs (50 ps maximum)
- Packaged in 8-pin SOIC
- Pb (lead) free package
- Low power CMOS technology
- Operating voltages of 2.5 V to 5 V
- Output Enable pin tri-states outputs
- 5 V tolerant input clock
- Commercial (0 to +70°C) and Industrial (-40 to +85°C) temperature ranges available

Block Diagram



Pin Assignment



Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | VDD | Power | Connect to +2.5 V, +3.3 V or +5.0 V. |
| 2 | Q0 | Output | Clock output 0. |
| 3 | Q1 | Output | Clock output 1. |
| 4 | GND | Power | Connect to ground. |
| 5 | ICLK | Input | Clock input, 5 V tolerant input. |
| 6 | Q2 | Output | Clock Output 2. |
| 7 | Q3 | Output | Clock Output 3. |
| 8 | OE | Input | Output Enable. Tri-states outputs when low. Connect to VDD for normal operation. |

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 1 and GND on pin 4, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the ICS553 is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15 ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS553. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| Output Enable and All Outputs | -0.5 V to VDD+0.5 V |
| ICLK | -0.5 V to 5.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70° C |
| Ambient Operating Temperature (industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|--------|------|-------|-------|
| Ambient Operating Temperature (commercial) | 0 | | +70 | ° C |
| Ambient Operating Temperature (industrial) | -40 | | +85 | ° C |
| Power Supply Voltage (measured in respect to GND) | +2.375 | | +5.25 | V |

DC Electrical Characteristics

VDD=2.5 V ±5%, Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|-----------|------|-----------|-------|
| Operating Voltage | VDD | | 2.375 | | 2.625 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | VDD/2+0.5 | | 5.5 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | VDD/2-0.5 | V |
| Input High Voltage, OE | V _{IH} | | 1.8 | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.7 | V |
| Output High Voltage | V _{OH} | I _{OH} = -16 mA | 2 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 16 mA | | | 0.4 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 25 | | mA |
| Nominal Output Impedance | Z _O | | | 20 | | Ω |
| Input Capacitance | C _{IN} | ICLK, OE pin | | 5 | | pF |
| Short Circuit Current | I _{OS} | | | ±28 | | mA |

DC Electrical Characteristics (continued)

VDD=3.3 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|-----------------|--------------------------|-----------|------|-----------|-------|
| Operating Voltage | VDD | | 3.15 | | 3.45 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | VDD/2+0.7 | | 5.5 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | VDD/2-0.7 | V |
| Input High Voltage, OE | V _{IH} | | 2 | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.4 | V |
| Output High Voltage (CMOS Level) | V _{OH} | I _{OH} = -12 mA | VDD-0.4 | | | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 35 | | mA |
| Nominal Output Impedance | Z _O | | | 20 | | Ω |
| Input Capacitance | C _{IN} | ICLK, OE pin | | 5 | | pF |
| Short Circuit Current | I _{OS} | | | ±50 | | mA |

VDD=5 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|----------------------------------|-----------------|--------------------------|---------|------|---------|-------|
| Operating Voltage | VDD | | 4.75 | | 5.25 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | VDD/2+1 | | 5.5 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | VDD/2-1 | V |
| Input High Voltage, OE | V _{IH} | | 2 | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.8 | V |
| Output High Voltage | V _{OH} | I _{OH} = -35 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 35 mA | | | 0.4 | V |
| Output High Voltage (CMOS Level) | V _{OH} | I _{OH} = -12 mA | VDD-0.4 | | | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 45 | | mA |
| Nominal Output Impedance | Z _O | | | 20 | | Ω |
| Input Capacitance | C _{IN} | ICLK, OE pin | | 5 | | pF |
| Short Circuit Current | I _{OS} | | | ±80 | | mA |

Notes: 1. Nominal switching threshold is VDD/2

AC Electrical Characteristics

VDD = 2.5 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------|-----------------|-------------------------------------|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =15 pF | | 1.0 | 1.5 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.8 V, C _L =15 pF | | 1.0 | 1.5 | ns |
| Propagation Delay | Note 1 | | 2.2 | 3 | 5 | ns |
| Additive Period Jitter | | | | | 1 | ps |
| Output to Output Skew | Note 2 | Rising edges at VDD/2 | | 0 | 50 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 500 | ps |

VDD = 3.3 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------|-----------------|-------------------------------------|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =15 pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.8 V, C _L =15 pF | | 0.6 | 1.0 | ns |
| Propagation Delay | Note 1 | | 2.0 | 2.4 | 4 | ns |
| Additive Period Jitter | | | | | 1 | ps |
| Output to Output Skew | Note 2 | Rising edges at VDD/2 | | 0 | 50 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 500 | ps |

VDD = 5 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|------------------------|-----------------|-------------------------------------|------|------|------|-------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.8 to 2.0 V, C _L =15 pF | | 0.3 | 0.7 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.8 V, C _L =15 pF | | 0.3 | 0.7 | ns |
| Propagation Delay | Note 1 | | 1.8 | 2.5 | 4 | ns |
| Additive Period Jitter | | | | | 1 | ps |
| Output to Output Skew | Note 2 | Rising edges at VDD/2 | | 0 | 50 | ps |
| Device to Device Skew | | Rising edges at VDD/2 | | | 500 | ps |

Notes: 1. With rail to rail input clock

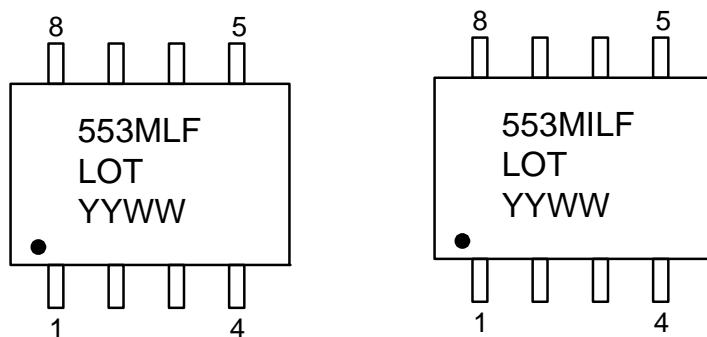
2. Between any 2 outputs with equal loading.

3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 140 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | °C/W |

Marking Diagrams

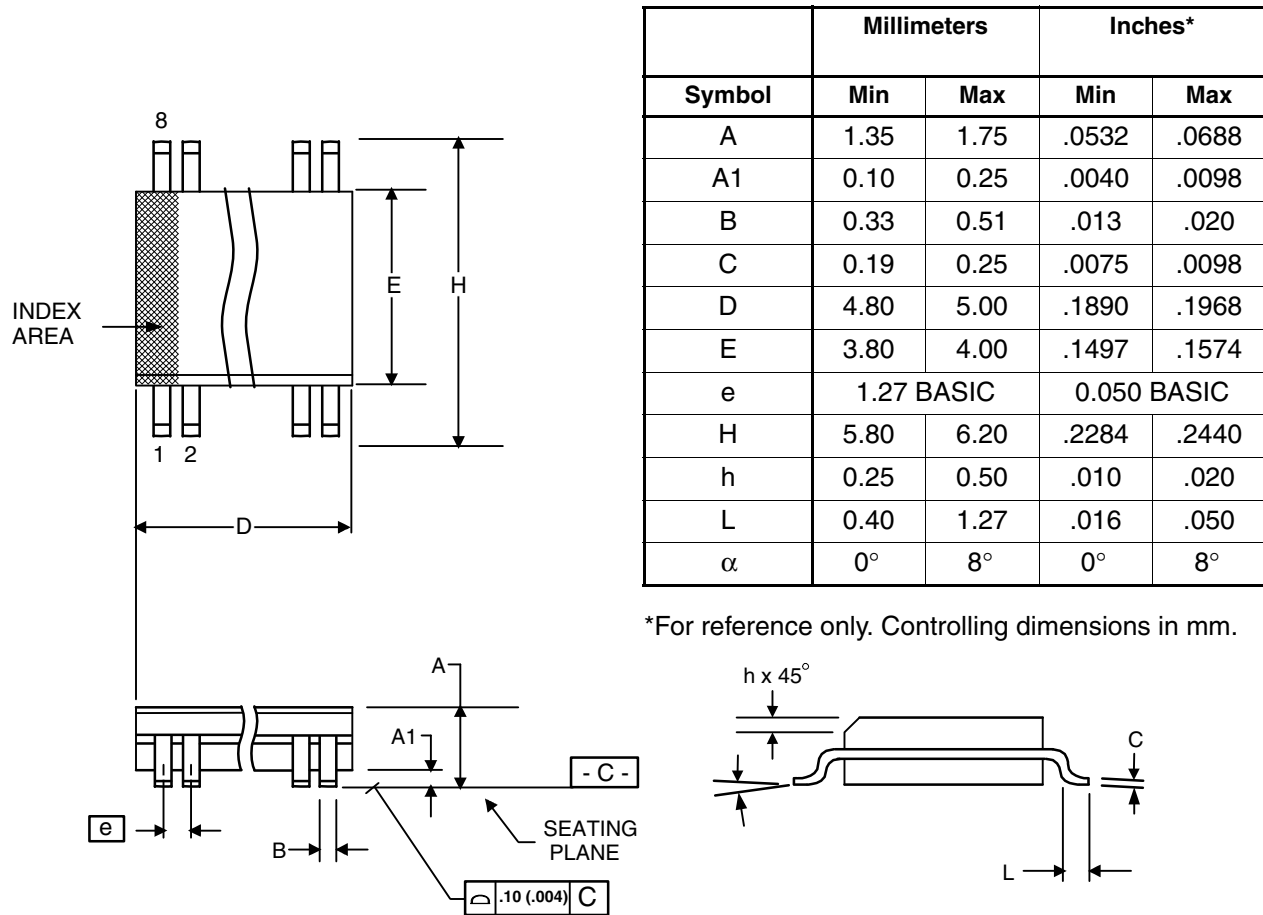


Notes:

1. "LOT" is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "LF" denotes RoHS compliant package.
4. "I" denotes industrial temperature range device.
5. Bottom marking: country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------|--------------------|------------|----------------|
| 553MLF | 553MLF | Tubes | 8-pin SOIC | 0 to +70° C |
| 553MLFT | 553MLF | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 553MILF | 553MILF | Tubes | 8-pin SOIC | -40 to +85 ° C |
| 553MILFT | 553MILF | Tape and Reel | 8-pin SOIC | -40 to +85 ° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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ICS553

LOW SKEW 1 TO 4 CLOCK BUFFER

FAN OUT BUFFER

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