Description

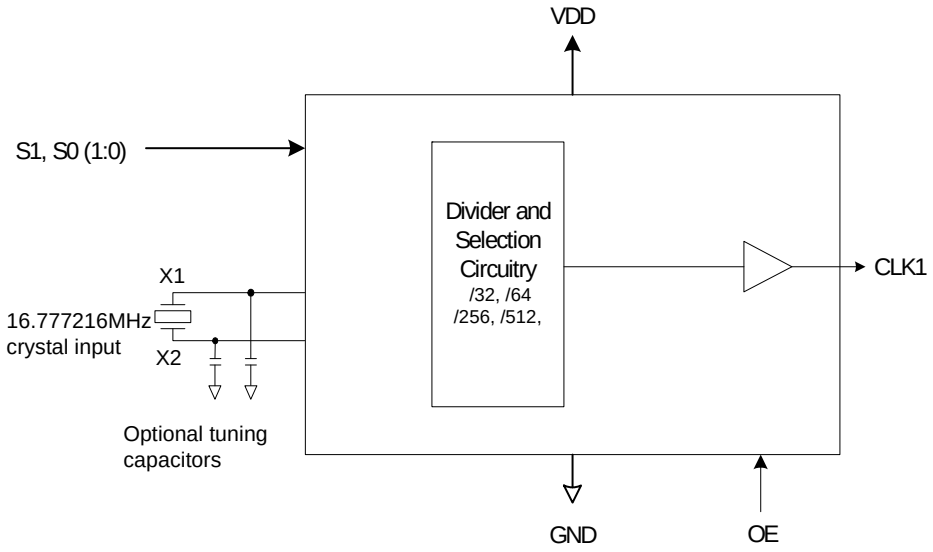
The ICS544-01 is crystal oscillator module IC with divide by 512 frequency output. It employs a 16.777216 MHz fundamental frequency crystal source oscillator to generate 32.768 kHz output crystal oscillator output. In addition a divide by 256, 64 and 32 options are also provided through select pins. The chip has an OE pin that tri-states the output and stops the oscillator circuits.

The ICS544-01 is a member of IDT's ClockBlocks™ family of clock building blocks. See the ICS541 and ICS542 for other clock dividers, and the ICS501, 502, 511, 512, and 525 for clock multipliers.

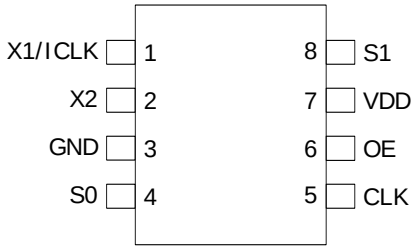
Features

- Packaged in 8-pin SOIC
- Pb-free package
- IDT's lowest cost clock divider
- Easy to use with other generators and buffers
- Input crystal at 16.777216MHz
- Output clock duty cycle of 45/55
- Output Enable
- Advanced, low-power CMOS process
- Operating voltage of 2.25 V to 3.6 V
- Does not degrade phase noise - no PLL
- Available in industrial temperature range

Block Diagram



Pin Assignment



8-pin (150 mil) SOIC

Clock Divider Table

S1	S0	CLK
0	0	Input/32
0	1	Input/64
1	0	Input/256
1	1	Input/512

0 = connect directly to ground

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Crystal input.
2	X2	Xo	Connect to crystal for crystal input and leave open for clock input.
3	GND	Power	Connect to ground.
4	S0	Input	Select 0 for output clock. Connect to GND or VDD, per divider table above. Internal pull-up resistor.
5	CLK	Output	Clock output per table above. Internal Pull down resistor.
6	OE	Input	Output Enable.Tri-states output clock when low. Also shuts down the oscillator circuit. Internal pull-up resistor. OE=1 normal operation.
7	VDD	Power	Connect to 2.25 V to 3.6 V.
8	S1	Input	Select 1 for output clock. Connect to GND or VDD, per divider table above. Internal pull-up resistor.

External Components

Series Termination Resistor

Ω

Ω

Ω

On chip capacitors
connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value (in pf) of these crystal caps equal (C_L-12)*2 in this equation, C_L=crystal load capacitance in pf. For example, for a crystal with a 16 pF load cap, each external crystal cap would be 8 pF. [(16-12)x2]=8.

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS544-01 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS544-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS544-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70° C
Ambient Operating Temperature (industrial)	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	° C
Ambient Operating Temperature (industrial)	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	2.25		3.6	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 2.25 V to 3.6 V, C_L=15pF ±5%**, Ambient Temperature -40° C to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.25		3.6	V
Input High Voltage	V_{IH}	S0, S1, OE, ICLK	0.7VDD			V
Input Low Voltage	V_{IL}	S0, S1, OE, ICLK			0.3VDD	V
Output High Voltage	V_{OH}	I_{OH} = -2 mA	VDD-0.4	VDD-0.15		V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA		0.15	0.4	V
Operating Supply Current	I_{DD}	VDD =2.25 V - 2.75 V		0.3	0.6	mA
Operating Supply Current	I_{DD}	VDD= 2.75 V - 3.6 V		0.5	1	mA
Standby Current	I_{SB}	OE=0			10	ua
Short Circuit Current	I_{OS}			±40		mA
Input Capacitance	C_{IN}	S0, S1, OE		4		pF
Nominal Output Impedance	Z_O	at VDD/2		20		Ω
Internal Pull-up Resistor	Rpup	OE, S1, S0		420		kΩ

AC Electrical Characteristics

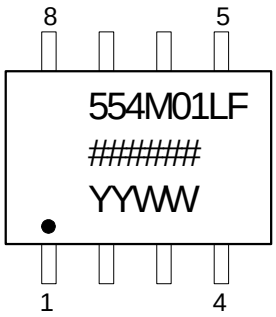
Unless stated otherwise, **VDD = 2.25 V to 3.6 V±5%**, **C_L=15pF ±5%,** Ambient Temp -40° C to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency, clock input		VDD = 3.3 V	0	16.777216		MHz
Output Rise Time	t_{OR}	0.1VDD to 0.9VDD		0.2	1	µs
Output Fall Time	t_{OF}	0.9VDD to 0.1VDD		0.2	1	µs
Duty Cycle		at VDD/2	45	49 to 51	55	%
Output Enable Delay Time	t_{OE}	OE going high to CLK output valid			2	µs
Output Disable Delay Time	t_{OD}	OE going low to CLK output invalid			2	µs

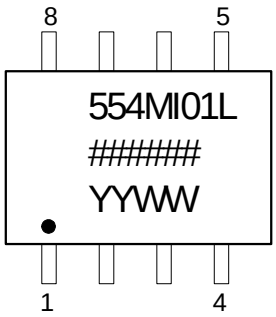
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram (ICS554M-01LF)



Marking Diagram (ICS554MI-01LF)

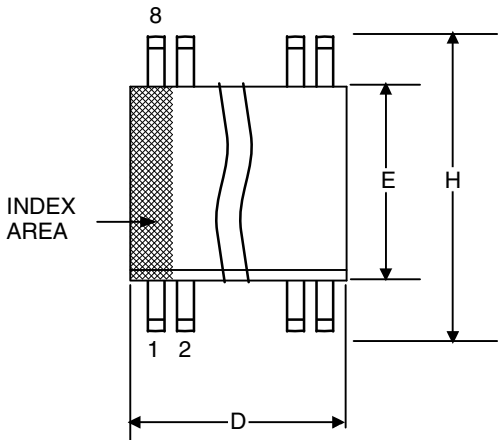


Notes:

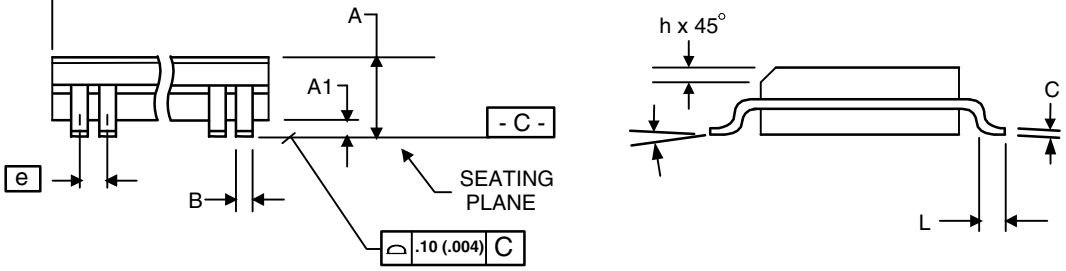
1. ###### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “L” or “LF” denotes Pb (lead) free package.
4. “I” denotes industrial temperature range.
5. Bottom Marking: (origin)
   Origin = country of origin if not USA.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
544M-01LF	544M01LF	Tubes	8-pin SOIC	0 to +70° C
544M-01LFT	544M01LF	Tape and Reel	8-pin SOIC	0 to +70° C
544MI-01LF	544MI01L	Tubes	8-pin SOIC	-40 to +85° C
544MI-01LFT	544MI01L	Tape and Reel	8-pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

CLOCK DIVIDER

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.