CLOCK SLICER USER CONFIGURABLE PECL INPUT ZDB ICS527-04

Description

The ICS527-04 Clock Slicer is the most flexible way to generate an output clock from an input clock with zero skew. The user can easily configure the device to produce nearly any output clock that is multiplied or divided from the input clock. The part supports non-integer multiplications and divisions. Using Phase-Locked Loop (PLL) techniques, the device accepts an input clock up to 200 MHz and produces an output clock up to 160 MHz.

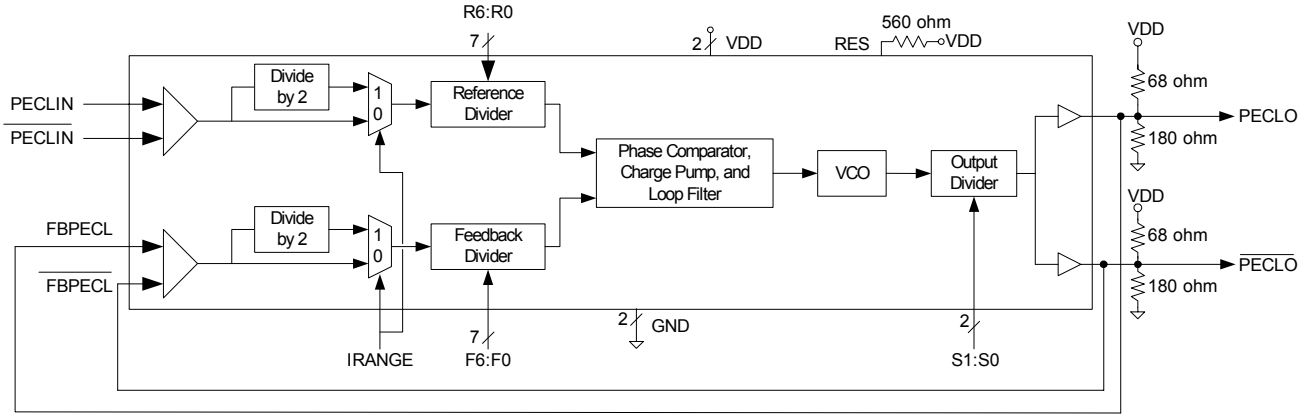
The ICS527-04 aligns rising edges on PECLIN with FBPECL at a ratio determined by the reference and feedback dividers.

For other PECL output clocks, see the ICS507-01, ICS525-03, or the MK3707. For PECL in and CMOS out, see the ICS527-02. For CMOS in and PECL out with zero delay, use the ICS527-03.

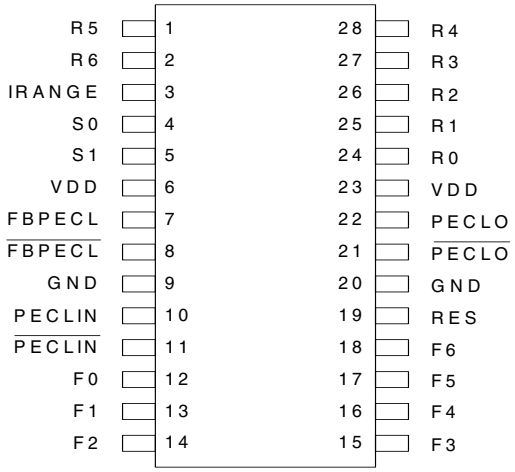
Features

- Packaged as 28-pin SSOP (150 mil body)
- Synchronizes fractional clocks rising edges
- CMOS in to PECL out
- PECL in to PECL out
- Pin selectable dividers
- Zero input to output skew
- User determines the output frequency - no software needed
- Slices frequency or period
- Input clock frequency of 1.5 MHz - 200 MHz
- Output clock frequencies up to 160 MHz
- Very low jitter
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



28-pin (150 mil) SSOP

Output Frequency and Output Divider Table

S1 Pin 5	S0 Pin 4	Output Frequency (MHz) PECLO Output Pair
0	0	10 - 80
0	1	5 - 40
1	0	2.5 - 20
1	1	20 -160

IRANGE Setting Table

IRANGE	Criteria
0	if (FBPECL < 80 MHz) and (PECLIN < 80 MHz)
1	if (FBPECL $\geq$ 80 MHz) or (PECLIN $\geq$ 80 MHz)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1 - 2 24 - 28	R5, R6, R0-R4	Input	Reference divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up.
3	IRANGE	Input	Set for proper frequency range of input clocks. See table above.
4 - 5	S0, S1	Input	Select pins for output frequency range. See table above. Internal pull-up.
6, 23	VDD	Power	Connect to +3.3 V.
7	FBPECL	Input	PECL feedback input to PLL.
8	$\overline{\text{FBPECL}}$	Input	$\overline{\text{PECL}}$ feedback input to PLL.
9, 20	GND	Power	Connect to ground
10	PECLIN	Input	PECL input clock.
11	$\overline{\text{PECLIN}}$	Input	Complementary PECL input clock.
12 - 18	F0-F6	Input	Feedback divider word input pins determined by user. Forms a binary number from 0 to 127. Internal pull-up
19	RES	BIAS	Resistor connection to VDD for setting level of PECL outputs.
21	$\overline{\text{PECLO}}$	Output	Complementary PECL output.
22	PECLO	Output	PECL output. Rising edge aligns with PECLIN when connected directly to FBPECL.

External Components

Decoupling Capacitors

The ICS527-04 requires two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. They must be connected close to the device to minimize lead inductance. The output levels can be adjusted for different output and load impedances. Refer to application note MAN09 for more information on the RES and resistor network values for the output clocks.

PECL Termination Networks

The PECLO to FBPECL and $\overline{\text{PECLO}}$ to $\overline{\text{FBPECL}}$ connections should be made directly underneath the device, unless feedback is being routed through other devices. The resistor divider networks should be placed as close to the outputs as possible.

Typical 50 Ω termination is shown in the Block Diagram on page 1. For other termination schemes, see MAN09.pdf.

Eliminating the Delay Through Buffers or Other Components

More complicated feedback schemes can be used, such as incorporating low skew, multiple output buffers in the feedback path. An example of this is given later in the datasheet. The fundamental property of the ICS527-04 is that it aligns rising edges on CLKIN and FBPECL at a ratio determined by the reference and feedback dividers. This means that any delay in the feedback path will cause the PECL output edge to lead PECLIN by the delay amount. So, by taking the PECL output from another device as the input to FBPECL, the delay through the other device can be eliminated.

Setting the Clock Slicer

Use IRANGE to select the input frequency range. If either the PECLIN or FBPECL pair frequencies are greater than (or equal to) 80 MHz, connect IRANGE to VDD, or let it float. If both frequencies are less than 80 MHz, connect IRANGE to ground.

Choose S1 and S0 from the table on page 2, depending on the output frequency.

Finally, the divider settings should be selected. Following is a description of how the dividers should be set.

Determining ICS527-04 Divider Settings

The user has full control in setting the desired output clock over the range shown in the table on page 2. The user should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout, so that the ICS527-04 automatically produces the correct clock when all components are soldered. It is also possible to connect the inputs to parallel I/O ports in order to switch frequencies. The configuration inputs: IRANGE, S1, S0, R6...0, F6...0 are compatible with CMOS or TTL levels.

The output of the ICS527-04 can be determined by the following simple equation:

$$\text{FB Frequency} = \text{Input Frequency} \times \frac{\text{FDW} + 2}{\text{RDW} + 2}$$

Where:

Reference Divider Word (RDW) = 0 to 127
Feedback Divider Word (FDW) = 0 to 127
FB Frequency is the same as the output frequency

Additionally, the following operating ranges should be observed:

$$300\text{kHz} < \frac{\text{Input Frequency}}{\text{RDW} + 2}$$

S1 and S0 should be selected depending on the output frequency. The table on page 2 gives the ranges.

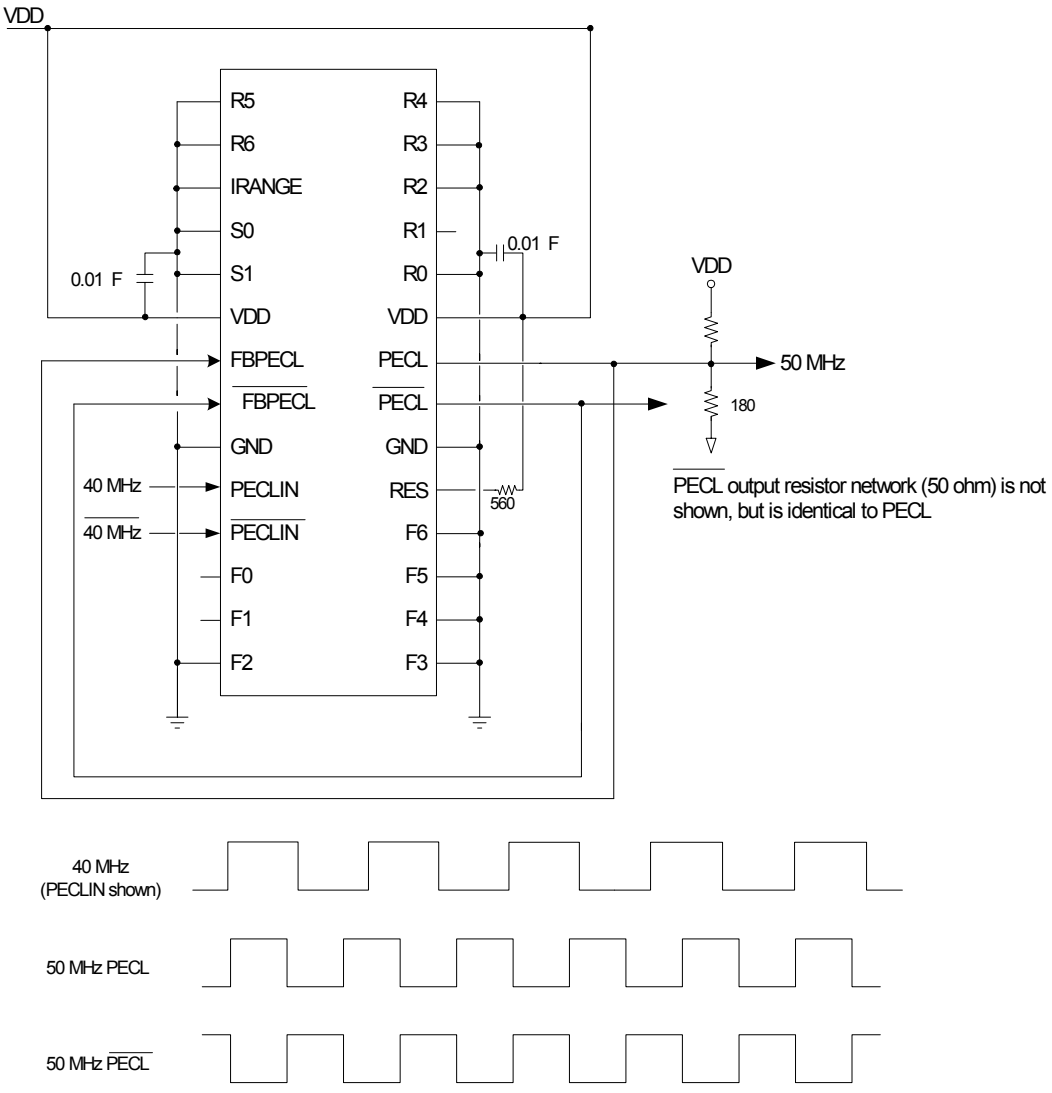
The dividers are expressed as integers. For example, if a 50 MHz output on CLK1 is desired from a 40 MHz input, the reference divider word (RDW) should be 2 and the feedback divider word (FDW) should be 3 which gives the required 5/4 multiplication. If multiple choices

of dividers are available, then the lowest numbers should be used. In this example, the output divide (OD) should be selected to be 2. Then R6:R0 is 0000010, F6:F0 is 0000011 and S1:S0 is 00.

If you need assistance determining the optimum divider settings, please send an e-mail to ics-mk@icst.com with the desired input clock and the desired output frequency.

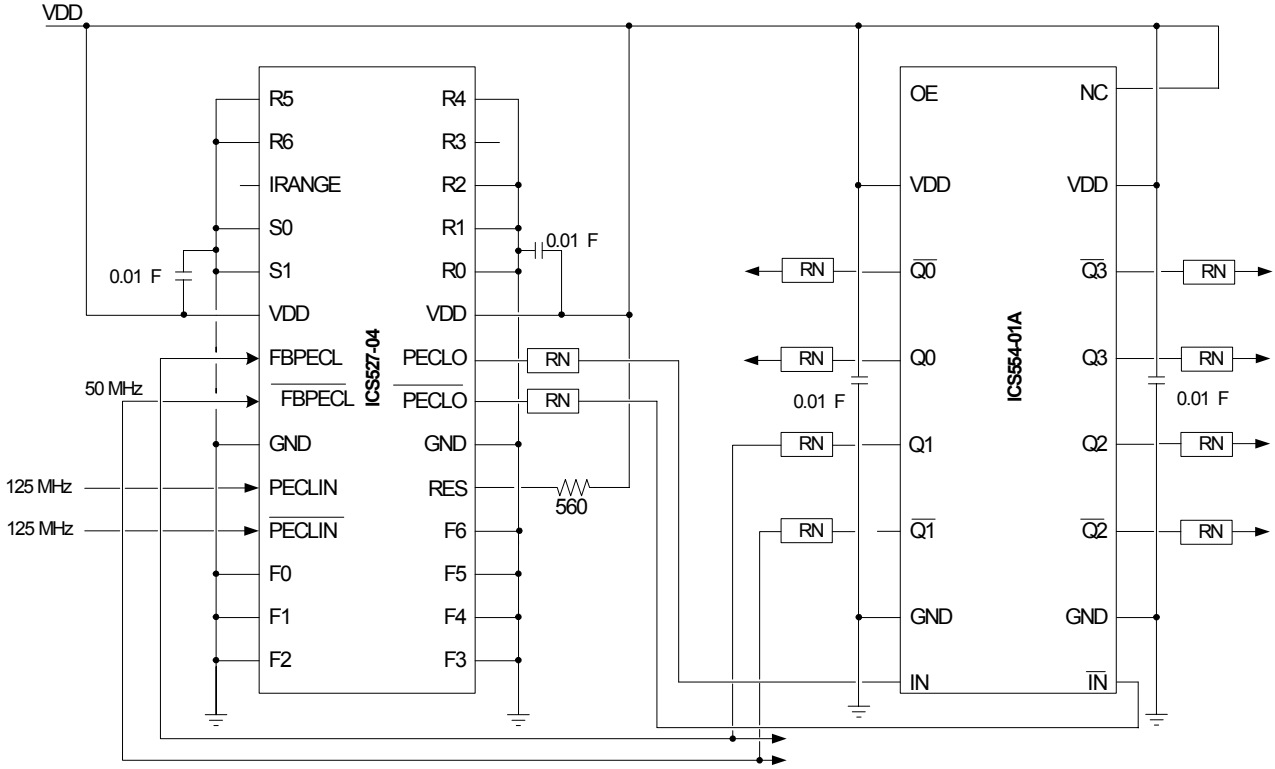
Typical Example

The following connection diagram shows the implementation of the example from the previous section. This will generate a 50 MHz clock synchronously with a 40 MHz input. The layout diagram below will produce the waveforms shown on the bottom of the example.

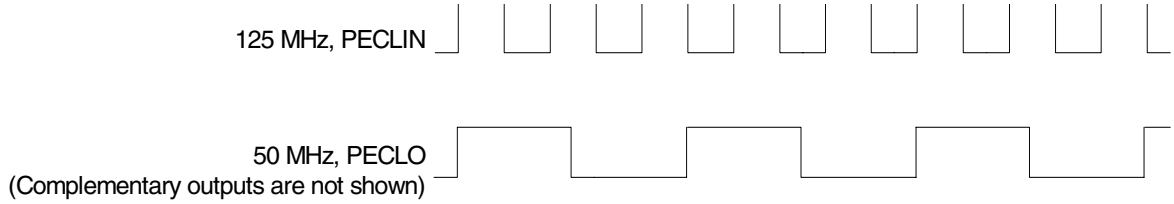


Multiple Output Example

In this example, an input clock of 125 MHz is used. Four low skew copies of 50 MHz PECL are required aligned to the 125 MHz input clock. The following solution uses the ICS554-01A, which is a 1 to 4 PECL buffer with low pin to pin skew.



The layout design above produces the waveforms shown below.



Using the equation for selecting dividers gives:

$$50\ \text{MHz} = 125\ \text{MHz} * \frac{(\text{FDW} + 2)}{(\text{RDW} + 2)}$$

If FDW = 0, then RDW = 3. This gives the required divide-by-5 function. Setting pin IRANGE = 1 (by leaving it unconnected and using the internal pull-up) allows a higher speed input clock like the 125 MHz. The FBPECL pair pins are connected to the Q1 outputs (chosen arbitrarily) of the ICS554. This aligns all the outputs of the ICS554 with the 125 MHz input since the ICS527-04 aligns rising edges on the PECLIN and FBPECL pins.

In this example, the resistor network needed for each PECLO output is represented by the RN boxes.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) PECL termination networks should be located as close to the outputs as possible.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS527-04. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS527-04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Peak to Peak Input Voltage		Pins 7, 8, 10, 11	0.3		1	V
Common Mode Range		Pins 7, 8, 10, 11	VDD-1.4		VDD-0.6	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Operating Supply Current	IDD	15 MHz in, 60 MHz out, no load		8		mA
Input Capacitance	C_{IN}			4		pF
On-chip pull-up resistor	R_{PU}	configuration inputs		270		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}		1.5		200	MHz
Output Frequency, CLK1	F_{OUT}	0 to +70° C	4		160	MHz
Output Duty Cycle	t_{OD}		45	50	55	%
Absolute Clock Period Jitter	t_{ja}	Deviation from mean		± 90		ps
One sigma Clock Period Jitter	t_{js}			40		ps
Input to output skew	t_{IO}	PECLIN to PECLO, Note 1	-250		250	ps
Device to device skew	t_{pi}	Common CLKIN, measured at FBPECL			500	ps

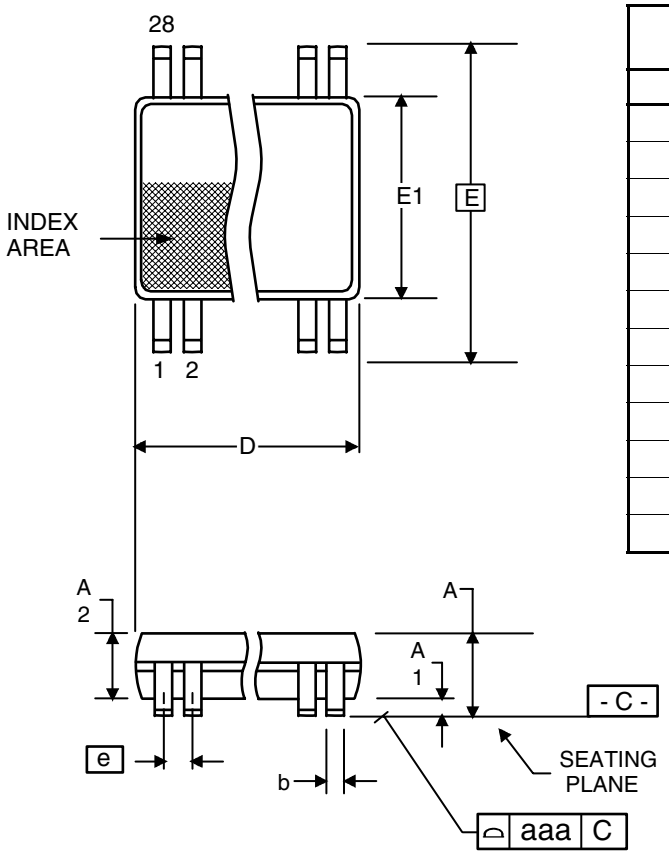
Note 1: Assumes clocks with same rise time, measured from rising edges at VDD/2.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		100		°C/W
	θ_{JA}	1 m/s air flow		80		°C/W
	θ_{JA}	3 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body, 0.025 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
527R-04LF	527R-04LF	Tubes	28-pin SSOP	0 to +70° C
527R-04LFT	527R-04LF	Tape and Reel	28-pin SSOP	0 to +70° C

"LF" denotes Pb free packaging, RoHS compliant

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.