

Description

The ICS525-01/02 are the most flexible way to generate a high-quality, high-accuracy, high-frequency clock output from an inexpensive crystal or clock input. The user can configure the device to produce nearly any output frequency from any input frequency by grounding or floating the select pins. Neither microcontroller, software, nor device programmer are needed to set the frequency. Using Phase-Locked Loop (PLL) techniques, the device accepts a standard fundamental mode, inexpensive crystal to produce output clocks up to 250 MHz. It can also produce a highly accurate output clock from a given input clock, keeping them frequency locked together.

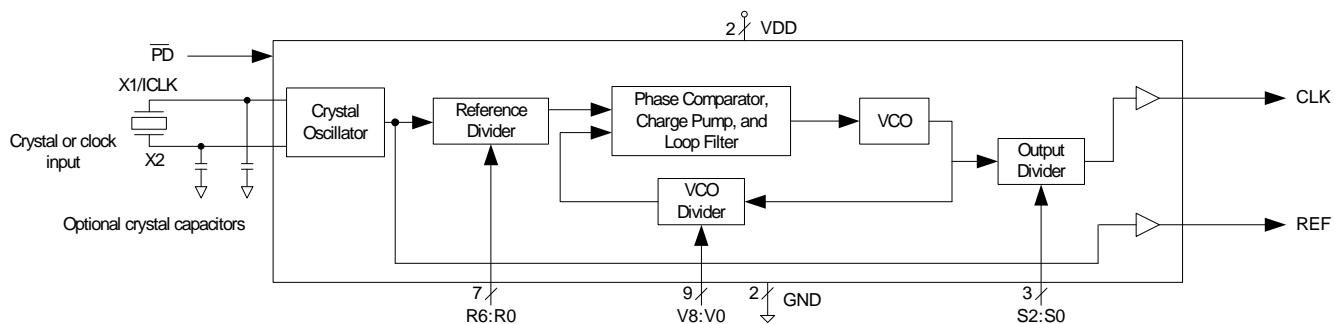
For similar capability with a serial interface, use the ICS307. For simple multipliers to produce common frequencies, refer to the ICS50x family of parts, which are smaller and more cost effective.

These products are intended for clock generation. They have low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed. For applications which require defined input to output timing, use the ICS527-01.

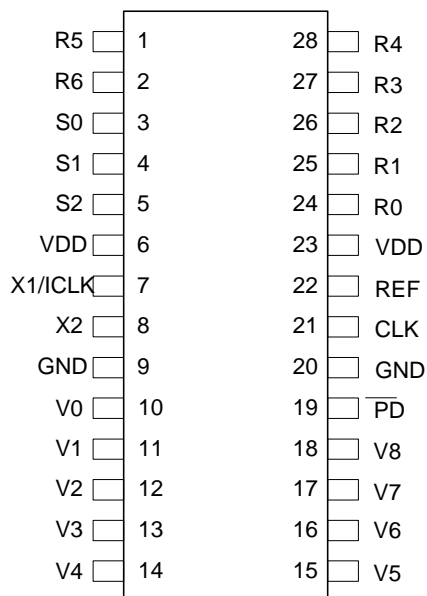
Features

- Packaged as 28-pin SSOP (150 mil body)
- Industrial and commercial versions available in Pb (lead) free package
- User determines the output frequency by setting all internal dividers
- Eliminates need for custom oscillators
- No software needed
- Online calculator determines register settings
- Pull-ups on all select inputs
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Very low jitter
- Duty cycle of 45/55 up to 200 MHz
- Operating voltage of 3.0 V or 5.5 V
- Ideal for oscillator replacement
- Industrial temperature version available
- For Zero Delay, refer to the ICS527

Block Diagram



Pin Assignment



ICS525-01/-02

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1, 2, 24-28	R5, R6, R0-R4	I(PU)	Reference divider word input pins determined by user. Forms a binary number from 0 to 127.
3, 4, 5	S0, S1, S2	I(PU)	Select pins for output divider determined by user. See table on page 3
6, 23	VDD	Power	Connect to VDD.
7	X1/ICLK	X1	Crystal connection. Connect to a parallel resonant fundamental crystal or input clock.
8	X2	X2	Crystal connection. Connect to a crystal or leave unconnected for clock.
9, 20	GND	Power	Connect to ground.
10 - 18	V0 - V8	I(PU)	VCO divider word input pins determined by user. Forms a binary number from 0 to 511.
19	PD	Input	Power-down. Active low. Turns off entire chip when low. Clock outputs tri-stated.
21	CLK	Output	Output clock determined by status of R0-R6, V-V8, S0-S2, and input frequency.
22	REF	Output	Reference output. Buffered crystal oscillator (or clock) output.

KEY: I(PU) = Input with internal pull-up resistor; X1, X2 = crystal connections

ICS525-01 Output Frequency and Output Divider Table

S2 Pin 5	S1 Pin 4	S0 Pin 3	CLK Output Divider	Output Frequency Range (MHz)			
				VDD = 5 V		VDD = 3.3 V	
				0 - 70°C	-40 to +85°C	0 - 70°C	-40 to +85°C
0	0	0	10	3–26	3–23	3–18	3–16
0	0	1	2	15–160	15–140	15–100	15–90
0	1	0	8	3.75–40	3.75–36	3.75–25	3.75–22
0	1	1	4	7.5–80	7.5–72	7.5–50	7.5–45
1	0	0	5	6–50	6–45	6–34	6–30
1	0	1	7	4–40	4–36	4–26	4–23
1	1	0	9	3.3–33.3	3.3–30	3.3–20	3.3–18
1	1	1	6	5–53	5–47	5–27	5–24

ICS525-02 Output Frequency and Output Divider Table

S2 Pin 5	S1 Pin 4	S0 Pin 3	CLK Output Divider	Output Frequency Range (MHz)	
				VDD = 5 V	VDD = 3.3 V
				-40 to +85°C	
0	0	0	6	5–67	5–40
0	0	1	2	15–200	15–120
0	1	0	8	3.75–50	3.75–30
0	1	1	4	7.5–100	7.5–60
1	0	0	5	6–80	6–48
1	0	1	7	4–57	4–34
1	1	0	1	30–250	30–200
1	1	1	3	10–133	10–80

External Components/Crystal Selection

Decoupling Capacitors

The ICS525-01/02 requires two 0.01µF decoupling capacitors to be connected between VDD and GND, one on each side of the chip. The capacitor must be connected close to the device to minimize lead inductance.

External Resistors

A 33Ω series termination resistor should be used on the CLK and REF pins.

Crystal Load Capacitors

The approximate total on-chip capacitance for a crystal is 16 pF, so a parallel resonant, fundamental mode crystal with this value of load (correlation) capacitance should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors may be connected from each of the pins X1 and X2 to Ground as shown in the block diagram. The value (in pF) of these crystal caps should be $(CL - 16) \cdot 2$, where CL is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Determining the Output Frequency

Users have full control in setting the desired output frequency over the range shown in the tables on pages 3-4. To replace a standard oscillator, users should connect the divider select input pins directly to ground (or VDD, although this is not required because of internal pull-ups) during Printed Circuit Board layout. The ICS525 will automatically produce the correct frequency when all components are soldered. It is also possible to connect the inputs to parallel I/O ports to switch frequencies. By choosing dividers carefully, the number of inputs which need to be changed can be minimized. Observe the restrictions on allowed values of VDW and RDW.

Configuration Pin Settings

The output of the ICS525 can be determined by the following simple equation:

$$\text{CLK Frequency} = \text{Input Frequency} \times 2^{\frac{(\text{VDW} + 8)}{(\text{RDW} + 2)}} \cdot \text{OD}$$

Where:

Reference Divider Word (RDW) = 0 to 127 (0 not permitted for ICS525-01)

VCO Divider Word (VDW) = 0 to 511 (0, 1, 2, 3 not permitted for ICS525-01)

Output Divider (OD) = values on pages 3-4

Also, the following operating ranges should be observed:

1. The output frequency must be in the ranges listed on pages 3-4.
2. The phase detector frequency must be above 200 kHz.

$$200\text{kHz} < \frac{\text{InputFrequency}}{(\text{RDW} + 2)}$$

Since all of the inputs have pull-up resistors, it is only necessary to ground the pins that need to be set to zero.

Which Part to Use?

The ICS525-01 is the original configurable clock.

The ICS525-02 has a higher maximum output frequency and a slightly different set of output dividers.

To determine the best combination of VCO, reference, and output divide, use the ICS525 Calculator on our web site.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS525-01/02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial	0 to +70°C
Ambient Operating Temperature, Industrial	-40 to +85°C
Storage Temperature	-65°C to 150°C
Junction Temperature	125°C
Soldering Temperature	260°C (max. of 10 seconds)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Operating Supply Current	IDD	60 MHz out, no load, 15 MHz crystal, ICS525-01/02 only		8		mA
Operating Supply Current, Power-down	IDD	Pin 19 = 0, Note 1		4		μA
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Input High Voltage, X1/ICLK only	V _{IH}	ICLK (pin7)	VDD/2+1	VDD/2		V
Input Low Voltage, X1/ICLK only	V _{IL}	ICLK (pin7)		VDD/2	VDD/2-1	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	VDD-0.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.4	V
Short Circuit Current		CLK and REF outputs		±55		mA
Input Capacitance	C _{IN}	V, R, S pins and pin 19		4		pF
On-chip Pull-up Resistor	R _{PU}	V, R, S pins and pin 19		270		kΩ

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 3.3\text{ V}$

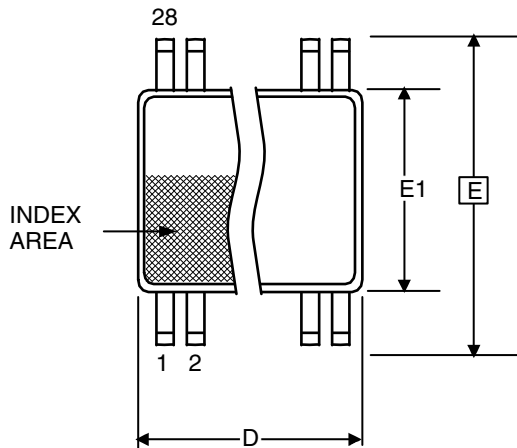
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Crystal input	5		27	MHz
		Clock input	2		50	MHz
Output Clock Rise Time		0.8 to 2.0 V		1		ns
Output Clock Fall Time		2.0 to 0.8 V		1		ns
Output Clock Duty Cycle, OD = 2, 4, 6, 8, or 10		At $V_{DD}/2$	45	49 to 51	55	%
Output Clock Duty Cycle, OD = 3, 5, 7, or 9		At $V_{DD}/2$	40		60	%
Output Clock Duty Cycle, OD = 1 (-02 only)		At $V_{DD}/2$	35		65	
Power-down Time, PD low to clocks stopped					50	ns
Power-up Time, PD high to clocks stable					10	ms
Absolute Clock Period Jitter, ICS525-01, Note 2	t_{ja}	Deviation from mean		± 140		ps
One Sigma Clock Period Jitter, ICS525-01, Note 2	t_{js}	One Sigma		45		ps
Absolute Clock Period Jitter, ICS525-02, Note 2	t_{ja}	Deviation from mean		± 85		ps
One Sigma Clock Period Jitter, ICS525-02, Note 2	t_{js}	One Sigma		30		ps

NOTE 1: Phase relationship between input and output can change at power-up. For a fixed phase relationship, see the ICS527.

NOTE 2: For 16 MHz, 100 MHz output. Use the -02 for lowest jitter.

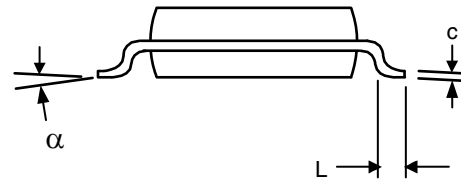
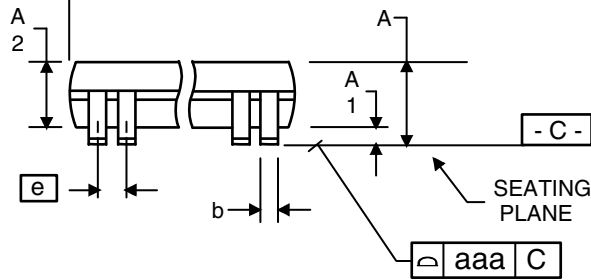
Package Outline and Package Dimensions (28-pin SSOP, 150 mil Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



Symbol	Millimeters		Inches*	
	Min	Max	Min	Max
A	1.35	1.75	.053	.069
A1	0.10	0.25	.0040	.010
A2	--	1.50	--	.059
b	0.20	0.30	.008	.012
C	0.18	0.25	.007	.010
D	9.80	10.00	.386	.394
E	5.80	6.20	.228	.244
E1	3.80	4.00	.150	.157
e	0.635 Basic		0.025 Basic	
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
525-01RLF	ICS525-01RLF	Tubes	28-pin SSOP	0 to +70°C
525-01RLFT	ICS525-01RLF	Tape and Reel	28-pin SSOP	0 to +70°C
525-01RILF	ICS525-01RILF	Tubes	28-pin SSOP	-40 to +85°C
525-01RILFT	ICS525-01RILF	Tape and Reel	28-pin SSOP	-40 to +85°C
525R-02LF	ICS525R-02LF	Tubes	28-pin SSOP	0 to +70°C
525R-02LFT	ICS525R-02LF	Tape and Reel	28-pin SSOP	0 to +70°C
525R-02ILF	ICS525R-02ILF	Tubes	28-pin SSOP	-40 to +85°C
525R-02ILFT	ICS525R-02ILF	Tape and Reel	28-pin SSOP	-40 to +85°C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

Revision History

Rev. U – removed -11 and -12 references/parts from datasheet. The devices are obsolete.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.