

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 1.0ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- $V_{CC} = 3.3V \pm 0.3V$
- Available in SSOP, SOIC, and QSOP packages

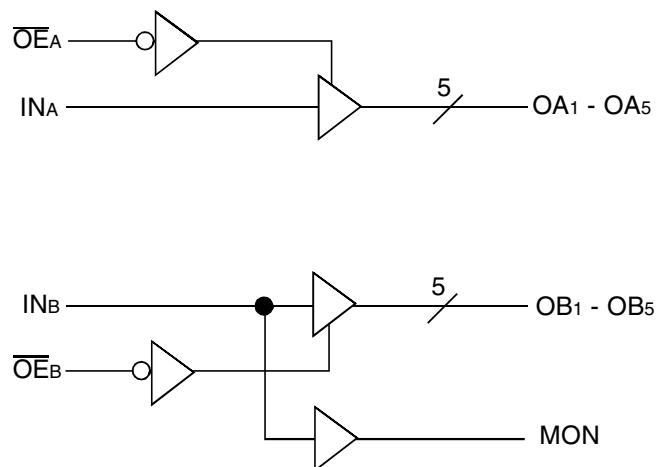
DESCRIPTION:

The FCT3805B is a 3.3 volt, non-inverting clock driver built using advanced dual metal CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805B offers low capacitance inputs with hysteresis.

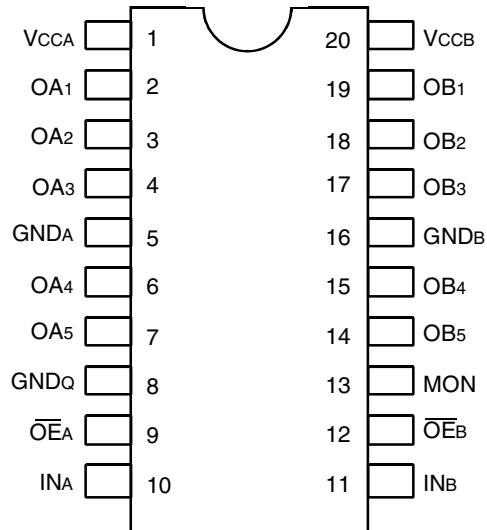
The FCT3805B is designed for high speed clock distribution where signal quality and skew are critical. The FCT3805B also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

For more information on using the FCT3805B with two different input frequencies on bank A and B, please see AN-236.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V _{IN} = 0V	4.5	6	pF
COUT	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
OEA, OEB	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAn, OBn	Clock Outputs
MON	Monitor Output

FUNCTION TABLE⁽¹⁾

Inputs		Outputs	
OEA, OEB	INA, INB	OAn, OBn	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:

1. H = HIGH
L = LOW
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3V \pm 0.3V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	5.5	—	V
	Input HIGH Level (I/O pins)		2	—	$V_{CC} + 0.5$	—	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5V$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	μA
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}	(3-State Output Pins)		$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18mA$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3V, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5V^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3V, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5V^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	—	—	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8mA$	$2.4^{(5)}$	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 0.1mA$	—	—	0.2	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16mA$	—	0.2	0.4	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24mA$	—	0.3	0.5	
I_{OFF}	Input Power Off Leakage	$V_{CC} = 0V, V_{IN} = 4.5V$		—	—	± 1	μA
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND} \text{ or } V_{CC}$		—	0.1	10	μA
I_{CCH}				—	—	—	—
I_{CCZ}				—	—	—	—

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V, +25^\circ\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. $V_{OH} = V_{CC} - 0.6V$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 0.6V$ ⁽³⁾		—	10	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $OEA = OEB = \text{GND}$ Per Output Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.035	0.06	mA/MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_O = 25\text{MHz}$ 50% Duty Cycle $OEA = OEB = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.9	1.6	mA
		$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.9	1.6		
		$V_{CC} = \text{Max.}$ Outputs Open $f_O = 50\text{MHz}$ 50% Duty Cycle $OEA = OEB = \text{GND}$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	20	$33^{(5)}$	
		$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	20	$33^{(5)}$		

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 3.3V$, $+25^\circ\text{C}$ ambient.

3. Per TTL driven input ($V_{IN} = V_{CC} - 0.6V$); all other inputs at V_{CC} or GND .

4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_O N_O)$

I_{CC} = Quiescent Current (I_{CCL} , I_{CCH} and I_{CCZ})

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.6V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_O = Output Frequency

N_O = Number of Outputs at f_O

All currents are in millamps and all frequencies are in megahertz.

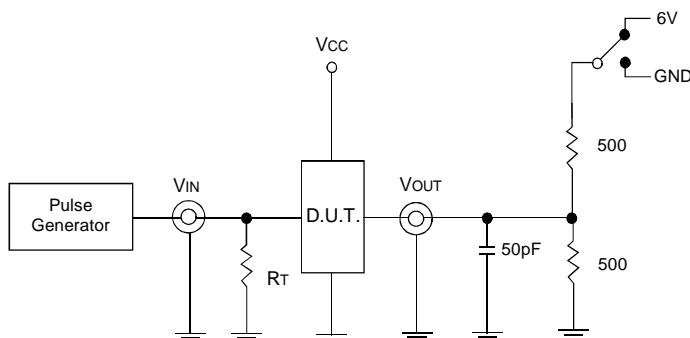
SWITCHING CHARACTERISTICS OVER OPERATING RANGE ^(3,4)

Symbol	Parameter	Conditions ⁽¹⁾	Commercial		Industrial		Unit
			Min. ⁽²⁾	Max.	—	—	
t_{PLH}	Propagation Delay INA to OAn, INB to OBr	$CL = 50\text{pF}$ $RL = 500\Omega$	1.5	5	1.5	5.2	ns
t_{PHL}			—	2	—	2	ns
t_R	Output Rise Time		—	2	—	2	ns
t_F	Output Fall Time		—	0.5	—	0.6	ns
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	1	—	1	ns
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($ t_{PHL} - t_{PLH} $)		—	1.2	—	1.2	ns
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		1.5	6	1.5	6	ns
t_{PZL}	Output Enable Time OEA to OAn, OEB to OBr		1.5	5	1.5	5	ns
t_{PHZ}	Output Disable Time OEA to OAn, OEB to OBr						

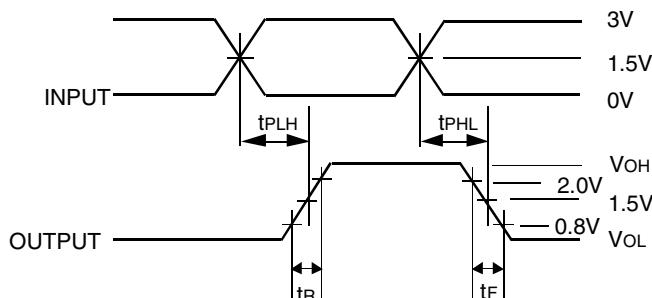
NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH} , t_{PHL} , $t_{SK(I)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC} , operating temperature and process parameters. These propagation delay limits do not imply skew.

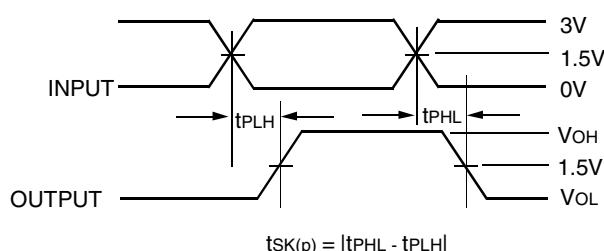
TEST CIRCUITS AND WAVEFORMS



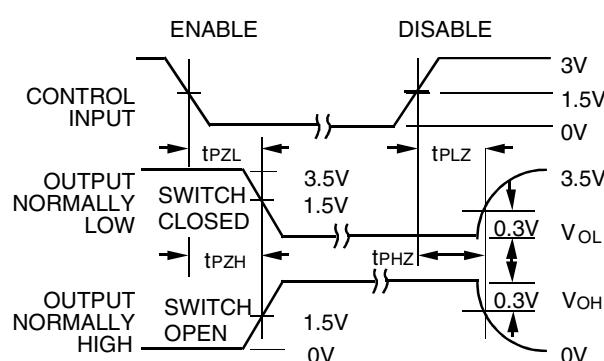
Test Circuits for All Outputs



Package Delay



Pulse Skew - $t_{SK}(p)$



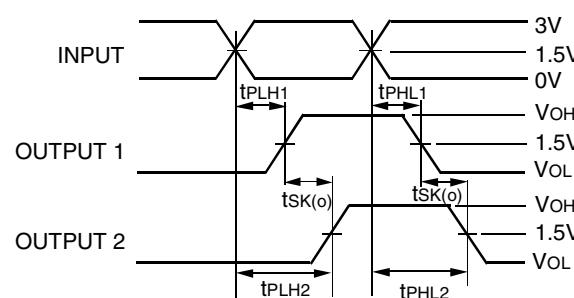
Output Skew - $t_{SK}(X)$

SWITCH POSITION

Test	Switch
Disable LOW	6V
Enable LOW	GND
Disable HIGH	GND
Enable HIGH	6V

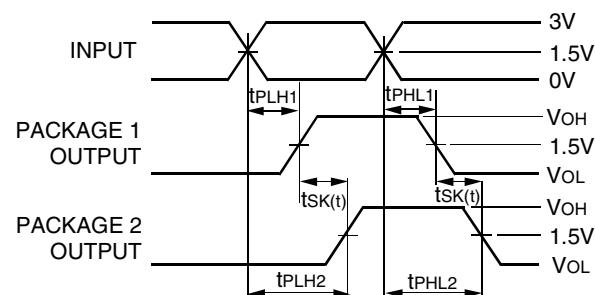
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



$$t_{SK}(o) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - $t_{SK}(o)$



$$t_{SK}(t) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Package Skew - $t_{SK}(t)$

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION

49FCT	XXXX	X	X		
Device Type		Package	Package		
				Blank	Commercial (0°C to +70°C)
				I	Industrial (-40°C to +85°C)
				SOG	SOIC - Green
				PYG	SSOP - Green
				QG	QSOP - Green
			3805B		Non-Inverting 3.3V Buffer/Clock Driver

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