QUAD PLL FOR DTV

ICS487-25

Description

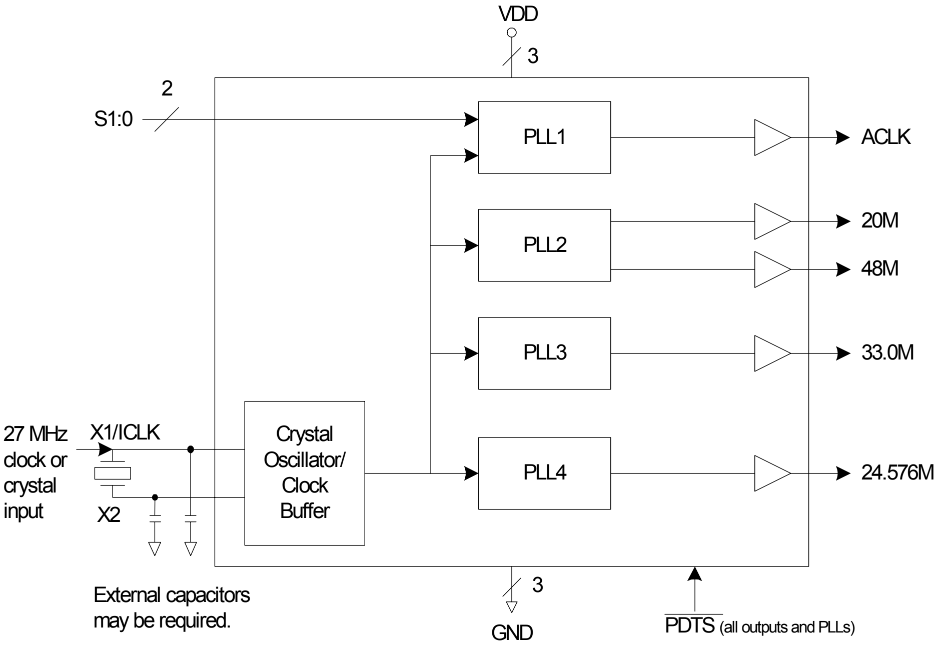
The ICS487-25 generates five high-quality, high-frequency clock outputs. It is designed to replace crystals and crystal oscillators in DTV applications. Using IDT's patented Phase Locked Loop (PLL) techniques, the device runs from a lower frequency crystal or clock input.

Because there is zero ppm frequency synthesis error on the audio clocks, the audio will remain locked to the video.

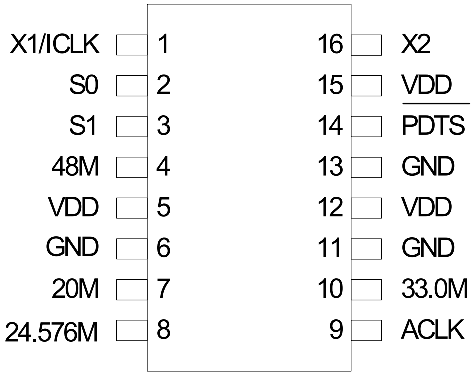
Features

- Packaged in 16-pin TSSOP (Pb-free)
- Replaces multiple crystals and oscillators
- Input crystal or clock frequency of 27 MHz
- Zero ppm frequency synthesis error
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



16 pin (173 mil) TSSOP

ACLK Output Selection Table

S1	S0	ACLK (MHz)
0	0	18.432
0	1	16.9344
1	0	12.288
1	1	18.432

Note: When S1 and S0 are switched, all other output clocks will remain stable throughout the transition.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	Input	Crystal connection. Connect to 27 MHz crystal or clock input.
2	S0	Input	Select pin 0. Determines ACLK output frequency per table above. Internal pull up resistor.
3	S1	Input	Select pin 1. Determines ACLK output frequency per table above. Internal pull up resistor.
4	48M	Output	48 MHz clcok output. Weak internal pull-down when tri-state.
5	VDD	Power	Connect to +3.3 V.
6	GND	Power	Connect to ground.
7	20M	Output	20 MHz clock output. Weak internal pull-down when tri-state.
8	24.576M	Output	24.576 MHz clock output. Weak internal pull-down when tri-state.
9	ACLK	Output	Audio clock output. Determined by table above. Weak internal pull-down when tri-state
10	33.0M	Output	33.0 MHz clock output. Weak internal pull-down when tri-state.
11	GND	Power	Connect to ground.
12	VDD	Power	Connect to +3.3 V.
13	GND	Power	Connect to ground.
14	$\overline{\text{PDTS}}$	Input	Powers down entire chip and tri-states outputs when low. Internal pull-up resistor.
15	VDD	Power	Connect to +3.3 V.
16	X2	Input	Connect to 27 MHz crystal or float for clock input.

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS487-25 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between each VDD and the PCB ground plane.

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitors should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitors and VDD pins. The PCB trace to VDD pins should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS487-25. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS487-25. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C

Item	Rating
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.135	+3.3	+3.465	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.135	3.3	3.465	V
Supply Current	IDD	No load, $\overline{\text{PDTS}}$=1		35		mA
Power Down Current	IDDPD	No load, $\overline{\text{PDTS}}$=0		20		µA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}	Clock outputs		±70		mA
Input Capacitance, inputs	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
Internal Pull-up Resistor	R_{PU}	S1, S0, $\overline{\text{PDTS}}$ pins		360		kΩ
Internal Pull-down Resistor	R_{PD}	Clock outputs		510		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			27		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		1.2		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1.0		ns
Output Clock Duty Cycle		at VDD/2, Note 1	45	50	55	%
Absolute Clock Period Jitter		Note 1		±175		ps
Frequency Synthesis Error		All outputs		0		ppm
Output Enable Time	t_{OE}	$\overline{\text{PDTS}}$ high to output locked to ±1%		250		µs
Output Disable Time	t_{OD}	$\overline{\text{PDTS}}$ low to tri-state		20		ns
Audio Clock Stabilization Time		Time from a change in S1 or S0 until output stable within ±1%		50		µs

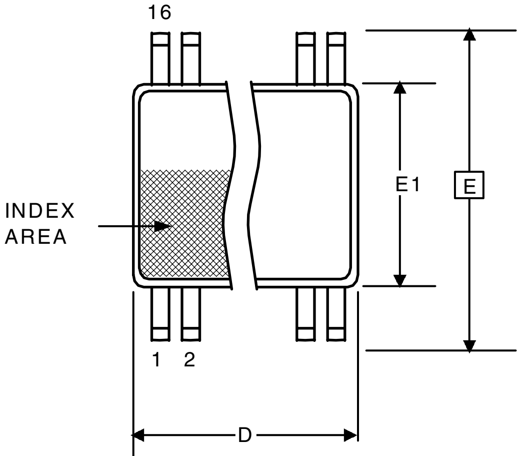
Note 1: Measured with a 15 pF load.

Thermal Characteristics

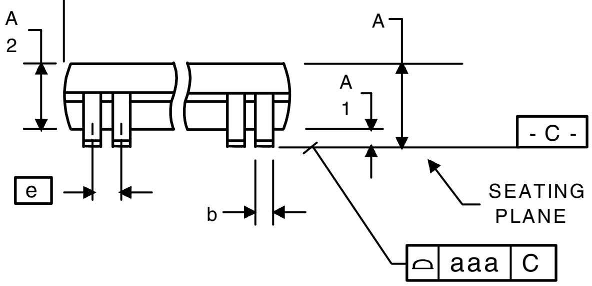
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		° C/W
	θ_{JA}	1 m/s air flow		70		° C/W
	θ_{JA}	3 m/s air flow		68		° C/W
Thermal Resistance Junction to Case	θ_{JC}			37		° C/W

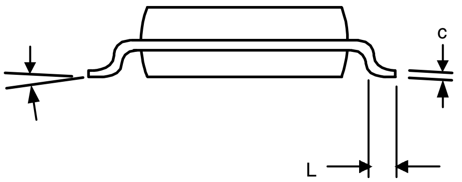
Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters Min	Millimeters Max	Inches Min	Inches Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004





Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
487G-25LF	487G-25LF (1st line) YYWW$$ (3rd line)	Tubes	16-pin TSSOP	0 to +70 °C
487G-25LFT		Tape and Reel	16-pin TSSOP	0 to +70 °C

"LF" suffix to the part number denotes Pb free configuration and RoHS compliant.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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