To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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DESCRIPTION
The 2SK3484 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES
• Low on-state resistance
  \( R_{DS(on)} = 125 \, \text{mΩ} \, \text{MAX. (} V_{GS} = 10 \, \text{V,} \, I_{0} = 8 \, \text{A)} \)
  \( R_{DS(on)} = 148 \, \text{mΩ} \, \text{MAX. (} V_{GS} = 4.5 \, \text{V,} \, I_{0} = 8 \, \text{A)} \)
• Low \( C_{iss} = 900 \, \text{pF TYP.} \)
• Built-in gate protection diode
• TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS (\( T_{A} = 25^\circ \text{C} \))
- Drain to Source Voltage (\( V_{DS} = 0 \, \text{V} \)) \( V_{DSS} \)
- Gate to Source Voltage (\( V_{DS} = 0 \, \text{V} \)) \( V_{GSS} \)
- Drain Current (DC) (\( T_{C} = 25^\circ \text{C} \)) \( I_{D} \)
- Drain Current (pulse) \( I_{D(pulse)} \)
- Total Power Dissipation (\( T_{C} = 25^\circ \text{C} \)) \( P_{T1} \)
- Total Power Dissipation (\( T_{A} = 25^\circ \text{C} \)) \( P_{T2} \)
- Channel Temperature \( T_{ch} \)
- Storage Temperature \( T_{stg} \)
- Single Avalanche Current \( I_{AS} \)
- Single Avalanche Energy \( E_{AS} \)

Notes
1. \( PW \leq 10 \, \mu s, \, \text{Duty Cycle} \leq 1\% \)
2. Starting \( T_{ch} = 25^\circ \text{C}, \, V_{DD} = 50 \, \text{V,} \, R_{G} = 25 \, \Omega, \, V_{GS} = 20 \rightarrow 0 \, \text{V} \)

THERMAL RESISTANCE
- Channel to Case Thermal Resistance \( R_{th(ch-C)} \)
- Channel to Ambient Thermal Resistance \( R_{th(ch-A)} \)

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## ELECTRICAL CHARACTERISTICS (T_A = 25°C)

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<td>Gate Leakage Current</td>
<td>I_GS</td>
<td>V_GS = ±20 V, V_DS = 0 V</td>
<td>±10 μA</td>
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<td>Gate Cut-off Voltage</td>
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<td>1.5 V</td>
<td>2.0 V</td>
<td>2.5 V</td>
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<tr>
<td>Forward Transfer Admittance</td>
<td>y_fs</td>
<td>V_DS = 10 V, I_D = 8 A</td>
<td>4.7 S</td>
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<tr>
<td>Drain to Source On-state Resistance</td>
<td>R_DS(on)1</td>
<td>V_GS = 10 V, I_D = 8 A</td>
<td>100 mΩ</td>
<td></td>
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<tr>
<td></td>
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<td>V_GS = 4.5 V, I_D = 8 A</td>
<td>110 mΩ</td>
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<tr>
<td>Input Capacitance</td>
<td>C_Iss</td>
<td>V_DS = 10 V</td>
<td>900 pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>C_Oss</td>
<td>V_DS = 0 V</td>
<td>110 pF</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>C_rss</td>
<td>f = 1 MHz</td>
<td>50 pF</td>
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<td></td>
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<tr>
<td>Turn-on Delay Time</td>
<td>t_d(on)</td>
<td>V_DD = 50 V, I_D = 8 A</td>
<td>9.0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time</td>
<td>t_r</td>
<td>V_GS = 10 V</td>
<td>5.0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off Delay Time</td>
<td>t_d(off)</td>
<td>R_G = 0 Ω</td>
<td>30 ns</td>
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<td></td>
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<td>Fall Time</td>
<td>t_f</td>
<td></td>
<td>4.0 ns</td>
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<td></td>
<td></td>
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<tr>
<td>Total Gate Charge</td>
<td>Q_G</td>
<td>V_DD = 80 V</td>
<td>20 nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate to Source Charge</td>
<td>Q_Os</td>
<td>V_DS = 10 V</td>
<td>3.0 nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate to Drain Charge</td>
<td>Q_OID</td>
<td>I_D = 16 A</td>
<td>5.0 nC</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Body Diode Forward Voltage</td>
<td>V_F(S-D)</td>
<td>I_F = 16 A, V_GS = 0 V</td>
<td>1.0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>t_rr</td>
<td>I_F = 16 A, V_GS = 0 V</td>
<td>60 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Recovery Charge</td>
<td>Q_rr</td>
<td>di/dt = 100 A/μs</td>
<td>122 nC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note**

**TEST CIRCUIT 1** AVALANCHE CAPABILITY

**TEST CIRCUIT 2** SWITCHING TIME

**TEST CIRCUIT 3** GATE CHARGE
SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

L - Inductive Load - mH
IAS - Single Avalanche Current - A

IAS = 10 A

VDD = 50 V
RG = 25 Ω
VGS = 20 → 0 V
Starting Tch = 25˚C

EAS = 10 mJ

SINGLE AVALANCHE ENERGY
DERATING FACTOR

Energy Derating Factor - %

Starting Tch - Starting Channel Temperature - ºC

VDD = 50 V
RG = 25 Ω
VGS = 20 → 0 V
IAS ≤ 10 A
PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

- 1. Gate
- 2. Drain
- 3. Source
- 4. Fin (Drain)

2) TO-252 (MP-3Z)

Note: The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT

Remark: The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.
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