

2SK1527-E1-E

500V - 40A - MOS FET
High Speed Power Switching

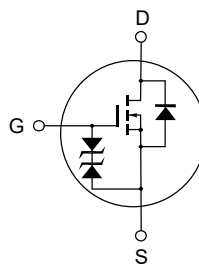
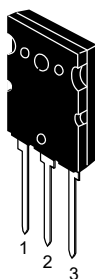
R07DS1196EJ0200
Rev.2.00
Feb.4.2022

Features

- Low on-resistance
 $R_{DS(on)} = 0.12 \Omega$ typ. (at $I_D = 20 A$, $V_{GS} = 10 V$, $T_a = 25^\circ C$)
- High speed switching
- Low drive current
- Suitable for switching regulator and DC-DC converter
- Quality grade: Standard

Outline

RENESAS Package code: PRSS0003ZN-A, PRSS0003ZC-A
(Package name: TO-264A, TO-264)



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$ Notes1	160	A
Body-drain diode reverse drain current	I_{DR}	40	A
Channel dissipation	P_{ch} Notes2	250	W
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

Note: Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$

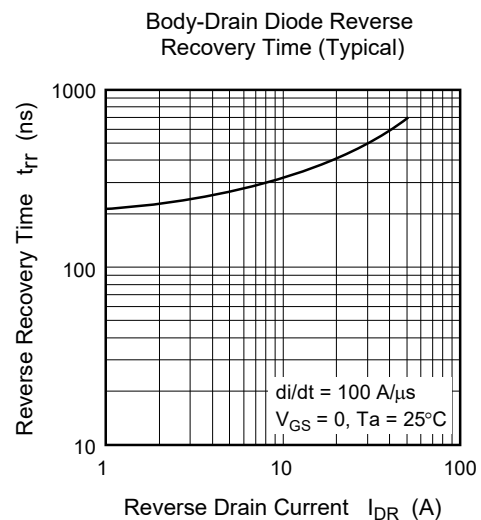
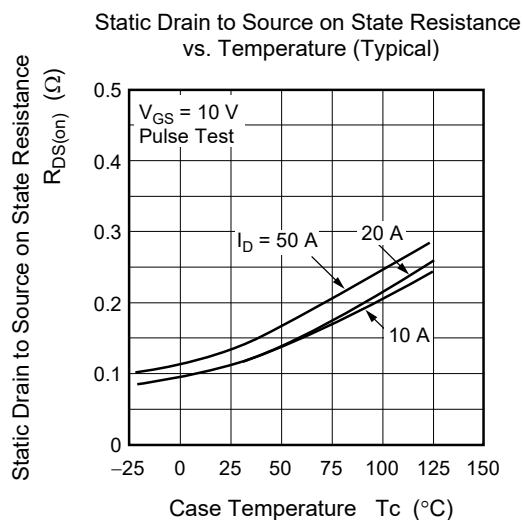
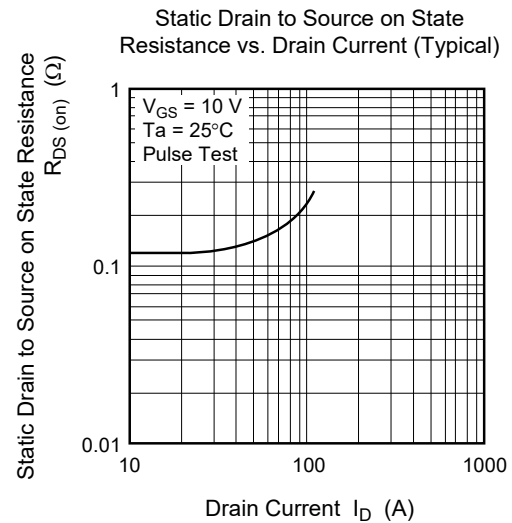
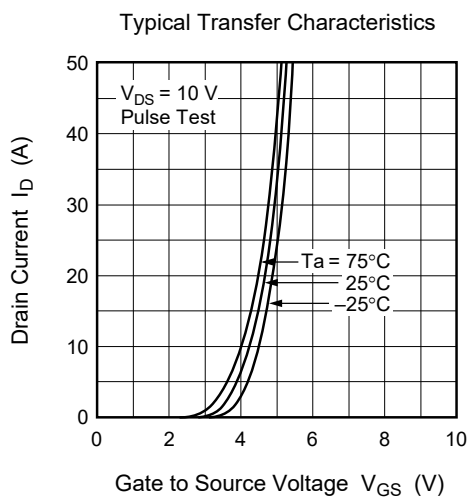
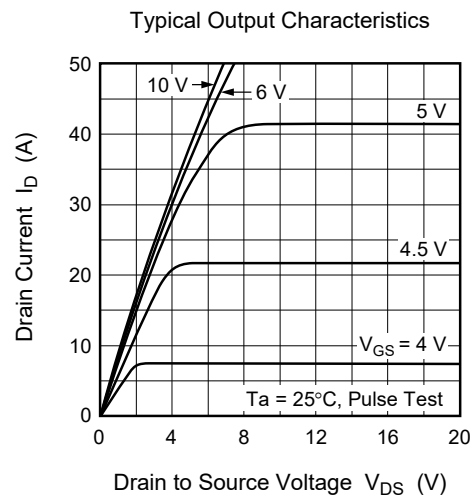
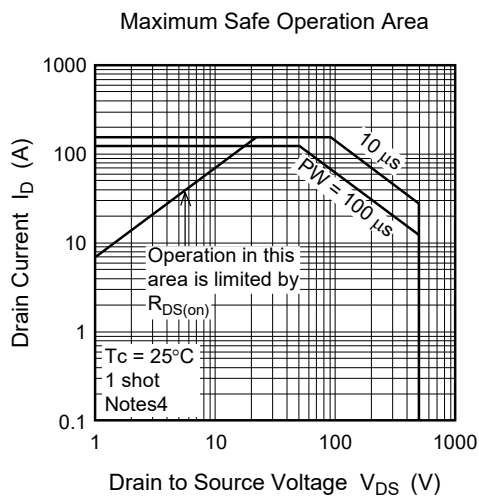
Electrical Characteristics

(Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 30	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	μA	$V_{DS} = 400 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.0	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = 20 \text{ A}$, $V_{GS} = 10 \text{ V}$ Notes3
Forward transfer admittance	$ y_{fs} $	20	30	—	S	$I_D = 20 \text{ A}$, $V_{DS} = 10 \text{ V}$ Notes3
Input capacitance	C_{iss}	—	5800	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	1430	—	pF	
Reverse transfer capacitance	C_{rss}	—	150	—	pF	
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$I_D = 20 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 1.5 \text{ }\Omega$
Rise time	t_r	—	175	—	ns	
Turn-off delay time	$t_{d(off)}$	—	420	—	ns	
Fall time	t_f	—	160	—	ns	
Body-drain diode forward voltage	V_{DF}	—	1.2	—	V	$I_F = 40 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	600	—	ns	$I_F = 40 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 3. Pulse test

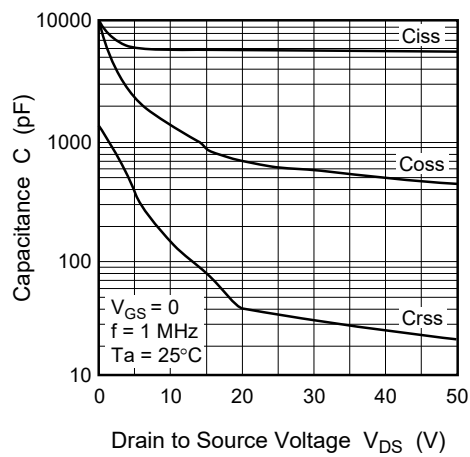
Main Characteristics



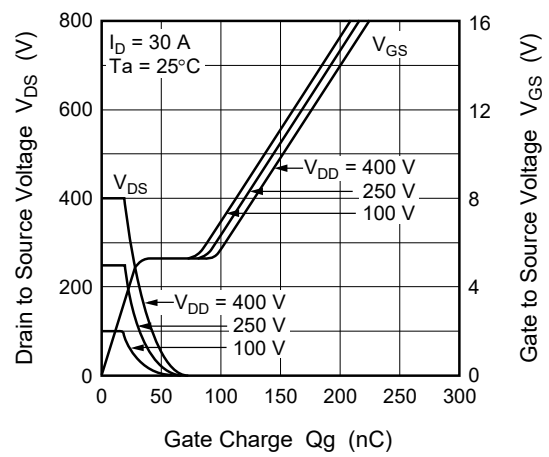
Notes: 4. Designed target value on Renesas measurement condition. (Not tested)

Renesas recommends that operating conditions are designed according to a document "Power MOS FET · IGBT Attention of Handling Semiconductor Devices".

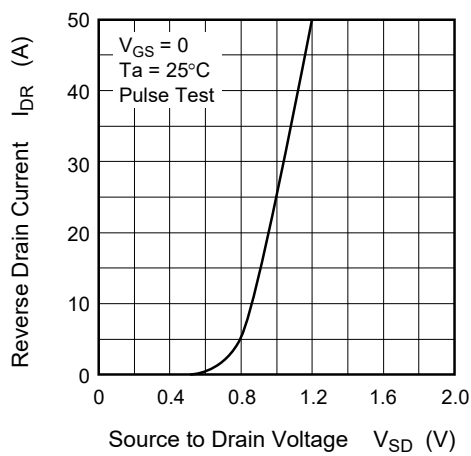
Typical Capacitance vs.
Drain to Source Voltage

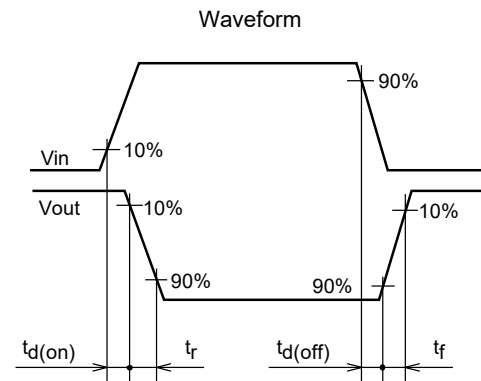
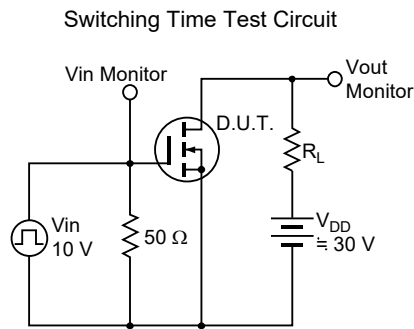
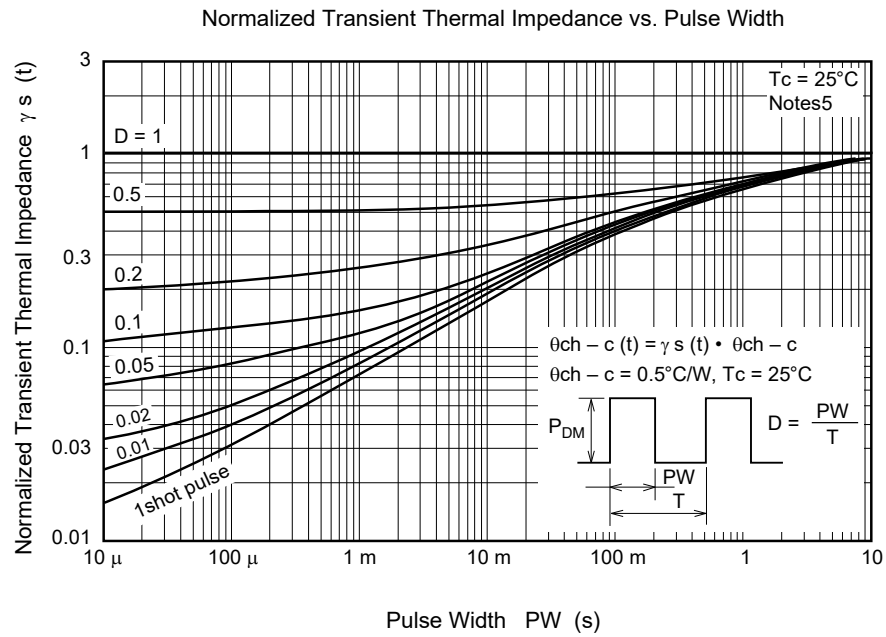


Dynamic Input Characteristics (Typical)



Reverse Drain Current vs.
Source to Drain Voltage (Typical)





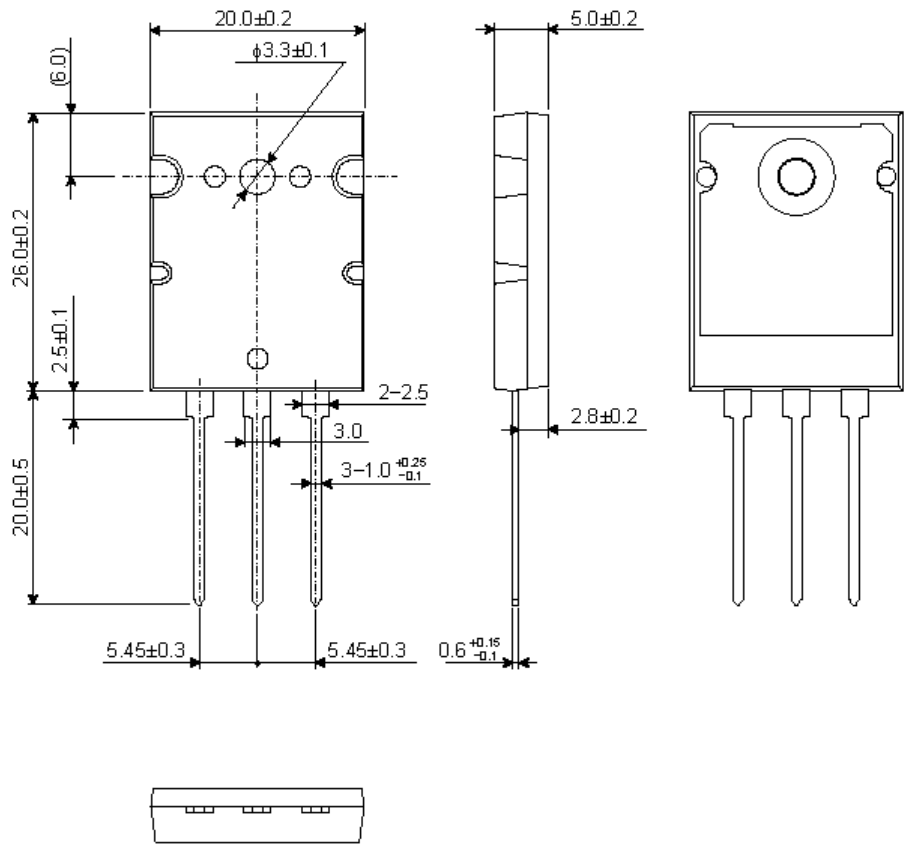
Notes: 5. Designed target value on Renesas measurement condition. (Not tested)

Package Dimensions

ASSEMBLED IN CHINA

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
TO-264A	—	PRSS0003ZN-A	TO-264A	9.7

Unit: mm

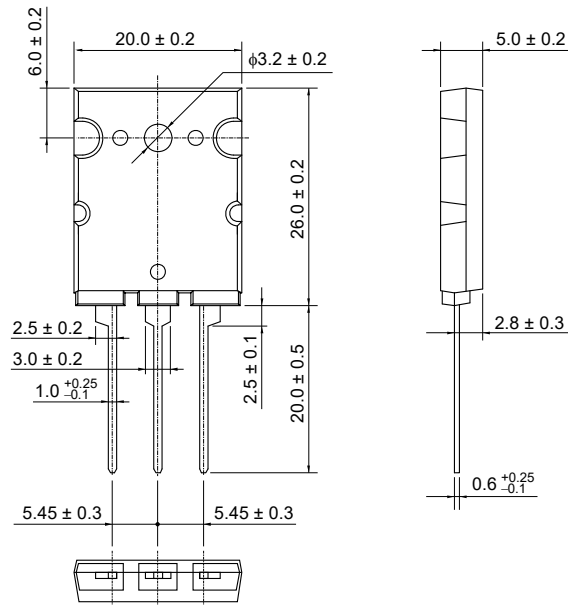


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ASSEMBLED IN KOREA

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
TO-264	—	PRSS0003ZC-A	TO-264S	9.48g

Unit: mm



Ordering Information

Orderable Part No.	Quantity	Shipping Container
2SK1527-E1-E#T2	25 pcs	Tube

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