To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR

2SJ649

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The 2SJ649 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

• Low on-state resistance:
  \[ R_{DS(on)} = 48 \, \text{m} \Omega \, \text{MAX.} \quad (V_{GS} = -10 \, \text{V}, \, I_D = -10 \, \text{A}) \]
  \[ R_{DS(on)} = 75 \, \text{m} \Omega \, \text{MAX.} \quad (V_{GS} = -4.0 \, \text{V}, \, I_D = -10 \, \text{A}) \]

• Low input capacitance:
  \[ C_{iss} = 1900 \, \text{pF TYP.} \quad (V_{DS} = -10 \, \text{V}, \, V_{GS} = 0 \, \text{V}) \]

• Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

- Drain to Source Voltage (VGS = 0 V) \( V_{DSS} \)
- Gate to Source Voltage (VDS = 0 V) \( V_{GSS} \)
- Drain Current (DC) (TC = 25°C) \( I_{D(DC)} \)
- Drain Current (pulse) \( I_{D(pulse)} \)
- Total Power Dissipation (TC = 25°C) \( P_T \)
- Total Power Dissipation (TA = 25°C) \( P_T \)
- Channel Temperature \( T_{ch} \)
- Storage Temperature \( T_{stg} \)
- Single Avalanche Current \( I_{AS} \)
- Single Avalanche Energy \( E_{AS} \)

Notes 1. PW ≤ 10 \( \mu \)s, Duty Cycle ≤ 1%
2. Starting \( T_{ch} = 25^\circ \text{C}, \, V_{DD} = -30 \, \text{V}, \, R_G = 25 \, \Omega, \, V_{GS} = -20 \rightarrow 0 \, \text{V} \)

ORDERING INFORMATION

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## ELECTRICAL CHARACTERISTICS (T_A = 25°C)

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<td>nC</td>
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<td></td>
<td></td>
<td>V</td>
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<tr>
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<td>t_r</td>
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<td>49</td>
<td></td>
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<td>Reverse Recovery Charge</td>
<td>Q_rr</td>
<td>di/dt = 100 A/µs</td>
<td>100</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
</tbody>
</table>

**Note** Pulsed: PW ≤ 350 µs, Duty Cycle ≤ 2%

### TEST CIRCUIT 1 AVALANCHE CAPABILITY

![TEST CIRCUIT 1 AVALANCHE CAPABILITY](image1)

### TEST CIRCUIT 2 SWITCHING TIME

![TEST CIRCUIT 2 SWITCHING TIME](image2)

### TEST CIRCUIT 3 GATE CHARGE

![TEST CIRCUIT 3 GATE CHARGE](image3)
TYPICAL CHARACTERISTICS (TA = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

FORWARD BIAS SAFE OPERATING AREA

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

SWITCHING CHARACTERISTICS

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT
SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

- $I_{AS1} = -20$ A
- $I_{AS2} = -10$ A
- $E_{AS1} = 40$ mJ
- $E_{AS2} = 100$ mJ
- $V_{DD} = -30$ V
- $R_G = 25$ Ω
- $V_{GS} = -20 \rightarrow 0$ V
- Starting $T_{ch} = 25°C$

SINGLE AVALANCHE ENERGY DERATING FACTOR

- $V_{DD} = -30$ V
- $R_G = 25$ Ω
- $V_{GS} = -20 \rightarrow 0$ V
- $I_{AS} \leq -20$ A
- Starting $T_{ch} = 25°C$

Energy Derating Factor - %

Starting $T_{ch} = \text{Starting Channel Temperature} - °C$

L - Inductive Load - H
PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)

EQUIVALENT CIRCUIT

Remark  The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.
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