IS-2981RH, IS-2981EH

Radiation Hardened 8-Channel Source Driver

FN4869
Rev 1.00
Jun 24, 2013

The Radiation Hardened IS-2981RH, IS-2981EH are monolithic devices designed for use in high-side switching applications that benefit from separate grounds for the logic and loads. The devices have a 5V to 80V operating supply voltage range and is capable of sourcing -200mA continuously from each output. The outputs are controlled by active-high inputs and may be paralleled to increase the drive current. The output clamp diodes prevent device damage, when switching inductive loads.

Constructed with the Intersil bonded wafer, dielectrically isolated HVTDLM process, these single event latch-up immune devices have been specifically designed to provide highly reliable performance in harsh radiation environments. They are fully guaranteed for 100krad(Si) high dose rate and 50krad(Si) low dose rate total dose performance through wafer-by-wafer radiation testing, and are production tested over the full military temperature range.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-00520. A "hot-link" is provided on our homepage for downloading

Features

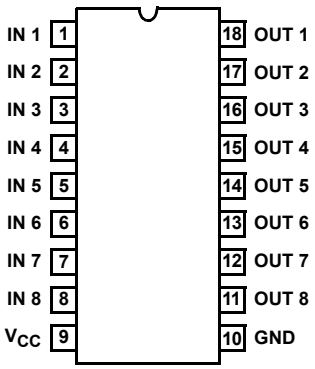
- Electrically screened to SMD # 5962-00520
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - Single event latch-up immune DI process
  - High dose rate . . . . . 100krad(Si)
  - Low dose rate . . . . . 50krad(Si)
- Input voltage range . . . . . 0.0V to V_{CC} (20V max)
- Supply voltage range . . . . . 5V to 80V
- Turn-on delay time . . . . . 2µs (max)
- Turn-off delay time . . . . . 11µs (max)
- Output clamp diode, V_F . . . . . -1.75V (max)

Applications

- Drivers for various loads
  - Relays, solenoids and motors
- Reliable replacement of discrete solutions
- Interfacing between low-level logic and high-current loads

Pin Configuration

IS1-2981RH-Q, IS1-2981EH-Q
(CDIP2-T18)
TOP VIEW



Ordering Information

ORDERING NUMBER (Note 3)	INTERNAL MKT.NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R0052001VVC	IS1-2981RH-Q	Q 5962R00 52001VVC	-55 to +125	18 Ld SBDIP	D18.3
5962R0052002VVC	IS1-2981EH-Q	Q 5962R00 52002VVC	-55 to +125	18 Ld SBDIP	D18.3
5962R0052001QVC	IS1-2981RH-8	Q 5962R00 52001QVC	-55 to +125	18 Ld SBDIP	D18.3
5962R0052001V9A	IS0-2981RH-Q		-55 to +125	Die	
5962R0052002V9A	IS0-2981EH-Q		-55 to +125	Die	D18.3
IS1-2981RH/PROTO	IS1-2981RH/PROTO	IS1-2981RH/PROTO	-55 to +125	18 Ld SBDIP	D18.3

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for IS-2981RH, IS-2981EH. For more information on MSL, please see tech brief TB363.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table on page 2 must be used when ordering.

Die Characteristics

DIE DIMENSIONS:

2667µm x 5131µm (105 mils x 202 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

INTERFACE MATERIALS

Glassivation

Type: Nitride (Si_3N_4) over Silox (SiO_2)
Nitride Thickness: 4.0kÅ ± 1.0kÅ
Silox Thickness: 12.0kÅ ± 4.0kÅ

Metallization

Top Metal 2: Ti/AlCu
Thickness: 1.6µm ± 0.02µm
Metal 1: Ti/AlCu
Thickness: 0.8µm ± 0.01µm

Substrate

HVTDLM, Bonded Wafer, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Must be tied to GND.

ADDITIONAL INFORMATION

Worst Case Current Density

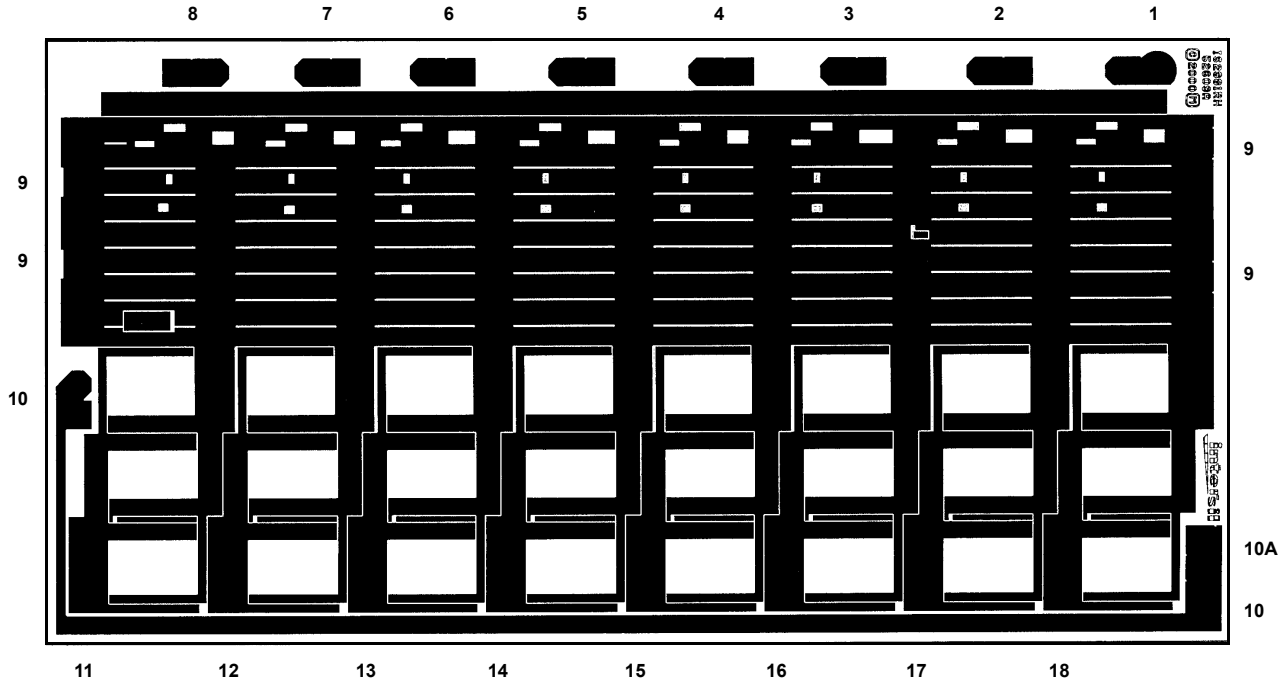
$<1.0 \times 10^5$ A/cm^2

Transistor Count

68

Metallization Mask Layout

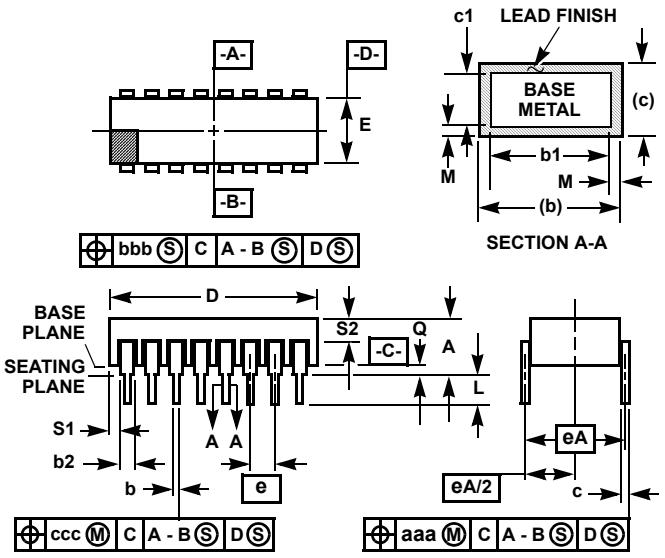
IS-2981RH, IS-2981EH



NOTES:

4. Pad numbers correspond to package pin functions.
5. Bond to all four pad 9 locations for V_{CC} current sharing purposes.
6. Bond to both pad 10 locations for GND current sharing purposes.
7. Pad 10A is not used in die applications.
8. Die backside must be connected to GND.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D18.3 MIL-STD-1835 CDIP2-T18 (D-6, CONFIGURATION C)
18 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		8

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