# TRIPLE PLL FIELD PROG. SPREAD SPECTRUM CLOCK SYNTHESIZER   ICS281

## Description

The ICS281 field programmable spread spectrum clock synthesizer generates up to three high-quality, high-frequency clock outputs including multiple reference clocks from a low-frequency crystal input. It is designed to replace crystals, crystal oscillators and stand alone spread spectrum devices in most electronic systems.

Using IDT's VersaClock$^{TM}$ software to configure PLLs and outputs, the ICS281 contains a One-Time Programmable (OTP) ROM for field programmability. Programming features include input/output frequencies, spread spectrum amount and eight selectable configuration registers.
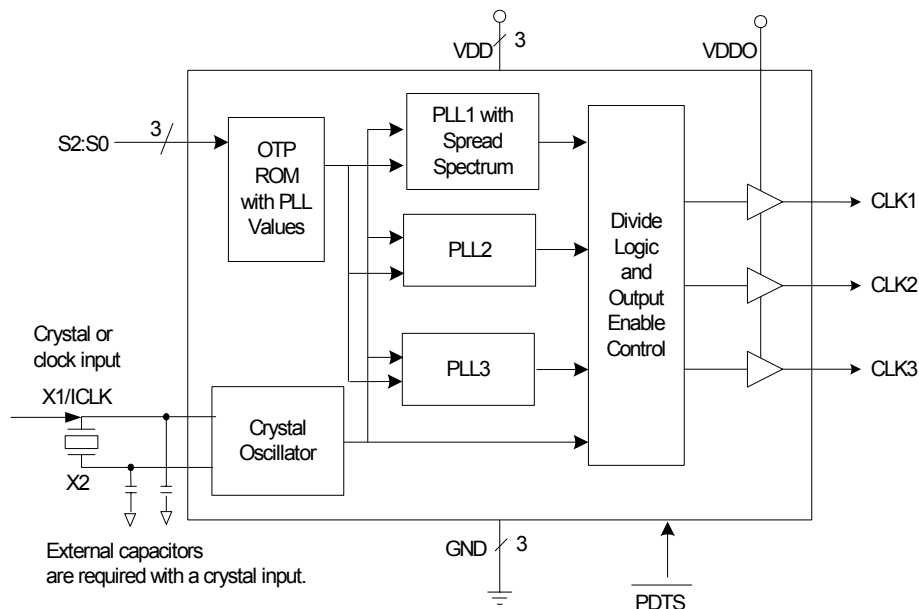
Using Phase-Locked Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal, or clock. It can replace multiple crystals and oscillators, saving board space and cost.

The ICS281 is also available in factory programmed custom versions for high-volume applications.
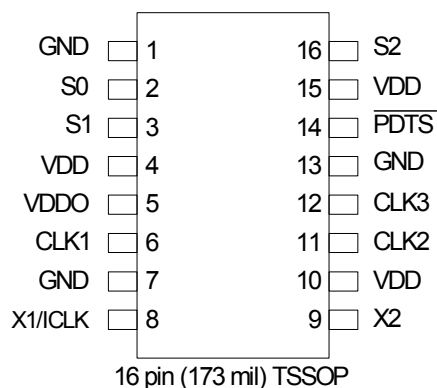
## Features

- Packaged as 16-pin TSSOP – Pb-free, RoHS compliant
- Eight addressable registers
- Replaces multiple crystals and oscillators
- Output frequencies up to 200 MHz at 3.3 V
- Configurable Spread Spectrum Modulation
- Input crystal frequency of 5 to 27 MHz
- Input clock frequency of 3 to 166 MHz
- Up to three reference outputs
- Operating voltages of 3.3 V
- VDDO output control from 1.8 V to 3.3 V
- Controllable output drive levels
- Advanced, low-power CMOS process

## Block Diagram

## Pin Assignment

```
GND    ▢  1      16 ▢   S2
 S0    ▢  2      15 ▢   VDD
 S1    ▢  3      14 ▢   PDTS
VDD    ▢  4      13 ▢   GND
VDDO   ▢  5      12 ▢   CLK3
CLK1   ▢  6      11 ▢   CLK2
GND    ▢  7      10 ▢   VDD
X1/ICLK ▢ 8       9 ▢   X2
```

16 pin (173 mil) TSSOP

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | GND | Power | Connect to ground. |
| 2 | S0 | Input | Select pin 0. Internal pull-up resistor. |
| 3 | S1 | Input | Select pin 1. Internal pull-up resistor. |
| 4 | VDD | Power | Connect to +3.3 V. |
| 5 | VDDO | Power | Power supply for outputs. |
| 6 | CLK1 | Output | Output clock 1. Weak internal pull-down when tri-state. |
| 7 | GND | Power | Connect to ground. |
| 8 | X1 | XI | Crystal input. Connect this pin to a crystal or external input clock. |
| 9 | X2 | XO | Crystal Output. Connect this pin to a crystal. Float for clock input. |
| 10 | VDD | Power | Connect to +3.3 V. |
| 11 | CLK2 | Output | Output clock 2. Weak internal pull-down when tri-state. |
| 12 | CLK3 | Output | Output clock 3. Weak internal pull-down when tri-state. |
| 13 | GND | Power | Connect to ground. |
| 14 | $\overline{\text{PDTS}}$ | Input | Power-down tri-state. Powers down entire chip and tri-states clock outputs when low. Internal pull-up resistor. |
| 15 | VDD | Power | Connect to +3.3 V. |
| 16 | S2 | Input | Select pin 2. Internal pull-up resistor. |

# External Components

The ICS281 requires a minimum number of external components for proper operation.

## Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

## Decoupling Capacitors

As with any high-performance mixed-signal IC, the ICS281 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias on the decoupling circuit.

## Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal ($C_L$ -6 pF)*2. In this equation, $C_L$= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

## ICS281 Configuration Capabilities

The architecture of the ICS281 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 1024 and N = 1 to 32,895.

The ICS281 also provides separate output divide values, from 2 through 63, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

$$OutputFreq = REFFreq \cdot \frac{M}{N}$$

## Output Drive Control

The ICS281 has two output drive settings. For VDDO=VDD, low drive should be selected when outputs are less than 100 MHz. High drive should be selected when outputs are greater than 100 MHz.

For VDDO<2.8 V, high drive should be selected for all output frequencies.

(Consult the AC Electrical Characteristics for output rise and fall times for each drive option.)

## IDT VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

## Spread Spectrum Modulation

The ICS281 utilizes frequency modulation (FM) to distribute energy over a range of frequencies. By modulating the output clock frequencies, the device effectively lowers energy across a broader range of frequencies; thus, lowering a system's electromagnetic interference (EMI). The modulation rate is the time from transitioning from a minimum frequency to a maximum frequency and then back to the minimum.

Spread Spectrum Modulation can be applied as either "center spread" or "down spread". During center spread modulation, the deviation from the target frequency is equal in the positive and negative directions. The effective average frequency is equal to the target frequency. In applications where the clock is driving a component with a maximum frequency rating, down spread should be applied. In this case, the maximum frequency, including modulation, is the target frequency. The effective average frequency is less than the target frequency.

The ICS281 operates in both center spread and down spread modes. For center spread, the frequency can be modulated between ±0.125% to ±2.0%. For down spread, the frequency can be modulated between -0.25% to -4.0%.

Both output frequency banks will utilize identical spread spectrum percentage deviations and modulation rates, if a common VCO frequency can be identified.

### Spread Spectrum Modulation Rate

The spread spectrum modulation frequency applied to the output clock frequency may occur at a variety of rates. For applications requiring the driving of "down-circuit" PLLs, Zero Delay Buffers, or those adhering to PCI standards, the spread spectrum modulation rate should be set to 30-33 kHz. For other applications, a 120 kHz modulation option is available.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS281. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Supply Voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Storage Temperature | | -65 | | 150 | °C |
| Soldering Temperature | Max 10 seconds | | | 260 | °C |
| Junction Temperature | | | | 125 | °C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature (ICS281PG/PGLF) | 0 | | +70 | °C |
| Ambient Operating Temperature (ICS281PGI/PGILF) | -40 | | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.135 | +3.3 | +3.465 | V |
| Power Supply Ramp Time | | | 4 | ms |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.135 | | 3.465 | V |
| VDDO Voltage | | | 1.80 | | VDD | V |
| Operating Supply Current Input High Voltage | IDD | Config. Dependent - See VersaClock$^{TM}$ Estimates | | | | mA |
| | | Three 33.3333 MHz outs, VDD=VDDO=3.3V; $\overline{PDTS}$ = 1, no load, Note 1 | | 20 | | mA |
| | | $\overline{PDTS}$ = 0, no load, Note 1 | | 500 | | μA |
| Input High Voltage | V$_{IH}$ | S2:S0 | VDD/2+1 | | | V |
| Input Low Voltage | V$_{IL}$ | S2:S0 | | | 0.4 | V |
| Input High Voltage, $\overline{PDTS}$ | V$_{IH}$ | | VDD-0.5 | | | V |
| Input Low Voltage, $\overline{PDTS}$ | V$_{IL}$ | | | | 0.4 | V |
| Input High Voltage | V$_{IH}$ | ICLK | VDD/2+1 | | | V |
| Input Low Voltage | V$_{IL}$ | ICLK | | | VDD/2-1 | V |
| Output High Voltage (CMOS High) | V$_{OH}$ | I$_{OH}$ = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | V$_{OH}$ | I$_{OH}$ = -8 mA (Low Drive); I$_{OH}$ = -12 mA (High Drive) | 2.4 VDDO-0.4 | | | V |
| Output Low Voltage | V$_{OL}$ | I$_{OL}$ = 8 mA (Low Drive); I$_{OL}$ = 12 mA (High Drive) | | | 0.4 | V |
| Short Circuit Current | I$_{OS}$ | Low Drive | | ±40 | | mA |
| | | High Drive | | ±70 | | |
| Nom. Output Impedance | Z$_O$ | | | 20 | | Ω |
| Internal pull-up resistor | R$_{PUS}$ | S2:S0, $\overline{PDTS}$ | | 190 | | kΩ |
| Internal pull-down resistor | R$_{PD}$ | CLK outputs | | 120 | | kΩ |
| Input Capacitance | C$_{IN}$ | Inputs | | 4 | | pF |

Note 1: Example with 25 MHz crystal input, three unloaded 33.$\overline{3}$ MHz outputs and VDD = VDDO = 3.3 V.

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

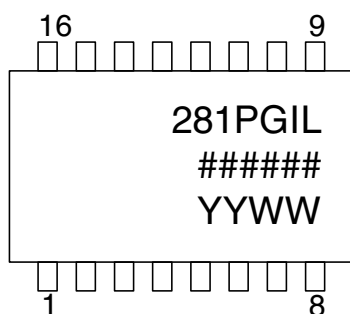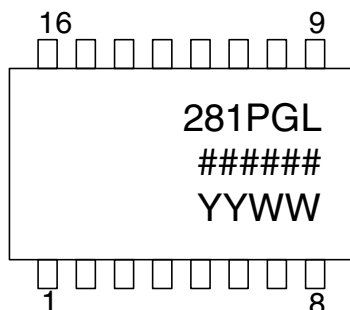| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $F_{IN}$ | Fundamental crystal | 5 | | 27 | MHz |
| | | Clock input | 3 | | 166 | MHz |
| Output Frequency | | VDDO=VDD | 0.314 | | 200 | MHz |
| | | 1.8 V≤VDDO≤2.8 V | 0.314 | | 150 | MHz |
| Output Rise/Fall Time | $t_{OF}$ | 80% to 20%, high drive, Note 1 | | 1.0 | | ns |
| Output Rise/Fall Time | $t_{OF}$ | 80% to 20%, low drive, Note 1 | | 2.0 | | ns |
| Output Rise/Fall Time | $t_{OF}$ | 80% to 20%, high drive, 1.8 V≤VDDO≤2.8 Note 2 | | 2.0 | | ns |
| Duty Cycle | | Note 2 | 40 | 49-51 | 60 | % |
| Output Frequency Synthesis Error | | Configuration Dependent | | TBD | | ppm |
| Power-up Time | | PLL lock-time from power-up | | 4 | 10 | ms |
| | | $\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum Off | | 0.6 | 2 | ms |
| | | $\overline{PDTS}$ goes high until stable CLK output, Spread Spectrum On | | 4 | 7 | ms |
| One Sigma Clock Period Jitter | | Configuration Dependent | | 50 | | ps |
| Maximum Absolute Jitter | $t_{ja}$ | Deviation from Mean. Configuration Dependent | | ±200 | | ps |

Note 1: Measured with 15 pF load.

Note 2: Duty Cycle is configuration dependent. Most configurations are min 45% / max 55%.

## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 78 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 70 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 68 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 37 | | °C/W |

## Marking Diagrams

16                    9

```
281PGL
######
YYWW
```

1                      8

16                    9

```
281PGIL
######
YYWW
```
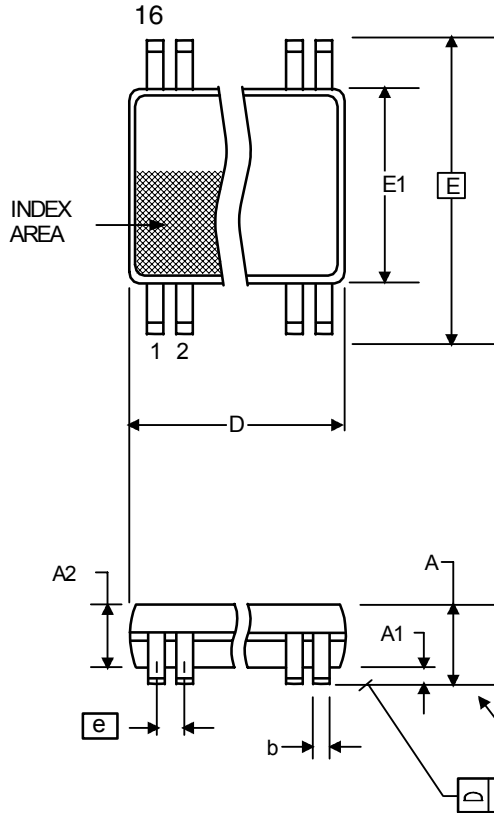
1                      8

Notes:

1. ###### is the lot number.

2. YYWW is the last two digits of the year and week that the part was assembled.

3. "I" denotes industrial temperature range (if applicable).

4. "L" denotes Pb (lead) free package.

5. Bottom marking: country of origin.

## Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | — | 1.20 | — | .047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| C | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 4.90 | 5.10 | 0.193 | 0.201 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | .018 | .030 |
| α | 0° | 8° | 0° | 8° |
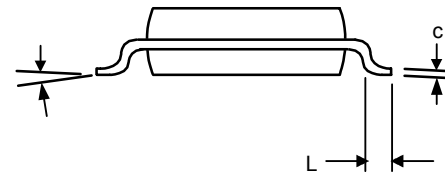
## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 281PGLF | see page 7 | Tubes | 16-pin TSSOP | 0 to +70°C |
| 281PGILF | | Tubes | 16-pin TSSOP | -40 to +85°C |
| 281G-XXLF | | Tubes | 16-pin TSSOP | 0 to +70°C |
| 281GI-XXLF | | Tubes | 16-pin TSSOP | -40 to +85°C |
| 281G-XXLFT | | Tape and Reel | 16-pin TSSOP | 0 to +70°C |
| 281GI-XXLFT | | Tape and Reel | 16-pin TSSOP | -40 to +85°C |

**"LF" suffix to the part number deontes the Pb-Free configuration, RoHS compliant.**

**The281G-XXLF and 281GI-XXLF are factory programmed versions of the 281PGLF and 281PGILF. A unique "-XX" suffix is assigned by the factory for each custom configuration, and a separate data sheet is kept on file. For more information on custom part numbers programmed at the factory, please contact your local IDT sales and marketing representative.**

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