2305

3.3V Zero-Delay Clock Buffer

Description

The 2305 is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero-delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10MHz to 133MHz.

The 2305 is an 8-pin version of the 2309. The 2305 accepts one reference input and drives out five low skew clocks. The -1H version of this device operates up to 133MHz frequency and has a higher drive than the -1 device. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the 2305 enters power down. In this mode, the device draws less than 25μA, the outputs are tri-stated, and the PLL is not running, resulting in a significant reduction of power.

The 2305 is characterized for both industrial and commercial operation.

Features

- Phase-Lock Loop clock distribution
- 10MHz to 133MHz operating frequency
- Distributes one clock input to one bank of five outputs
- Zero input-output delay
- Output skew < 250ps
- Low jitter < 200ps cycle-to-cycle
- 2305-1 for Standard drive
- 2305-1H for High drive
- No external RC network required
- Operates at 3.3V VDD
- Power-down mode
- Available in SOIC/TSSOP packages

Applications

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay designs

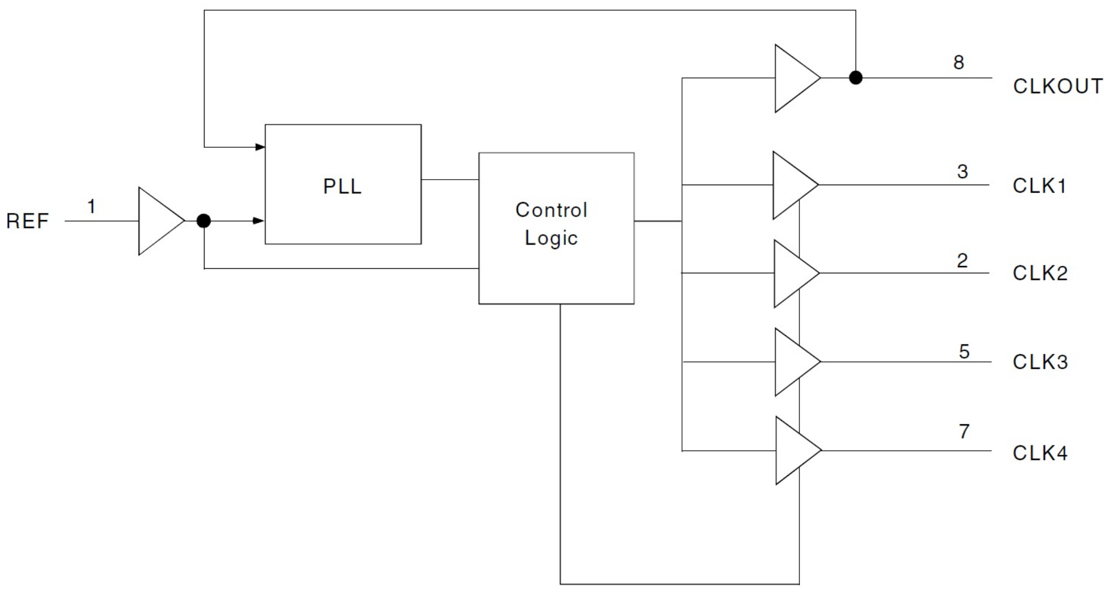


Figure 1. 2305 Functional Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments

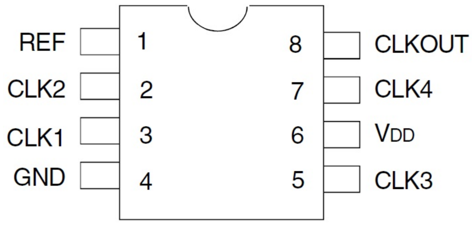


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	REF	In	Input reference clock, 5 Volt tolerant input.
2	CLK2[1]	Out	Output clock.
3	CLK1[1]	Out	Output clock.
4	GND	Ground	Ground.
5	CLK3[1]	Out	Output clock.
6	VDD	Power	3.3V supply.
7	CLK4[1]	Out	Output clock.
8	CLKOUT[1]	Out	Output clock, internal feedback on this pin.

1. Weak pull-down on all outputs.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Maximum	Unit
Supply Voltage Range, V_{DD}	-0.5 to +4.6	V
Input Voltage Range (REF), V_I [1]	-0.5 to +5.5	V
Input Voltage Range (except REF), V_I	-0.5 to VDD+0.5	V
Input Clamp Current, I_{IK} (V_I < 0)	-50	mA
Continuous Output Current, I_O (V_O = 0 to V_{DD})	±50	mA
Continuous Current, V_{DD} or GND	±100	mA
Maximum Power Dissipation, T_A = 55°C (in still air)[2]	0.7	W
Storage Temperature Range, T_{STG}	-65 to +150	°C
Commercial Temperature Range	0 to +70	°C
Industrial Temperature Range	-40 to +85	°C

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

2.2 Recommended Operating Conditions

Table 1. Recommended Operating Conditions – Commercial

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	3	3.6	V
Operating Temperature (ambient temperature), T_A	0	+70	°C
Load Capacitance < 100MHz, C_L	-	30	pF
Load Capacitance 100MHz – 133MHz, C_L	-	10	
Input Capacitance, C_{IN}	-	7	pF

Table 2. Recommended Operating Conditions – Industrial

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	3	3.6	V
Operating Temperature (ambient temperature), T_A	-40	+85	°C
Load Capacitance < 100MHz, C_L	-	30	pF
Load Capacitance 100MHz – 133MHz, C_L	-	10	
Input Capacitance, C_{IN}	-	7	pF

2.3 Electrical Specifications– Commercial

Table 3. DC Electrical Characteristics – Commercial

Parameter	Symbol	Conditions		Minimum	Maximum	Unit
Input LOW Voltage Level	V_{IL}	-		-	0.8	V
Input HIGH Voltage Level	V_{IH}	-		2	-	V
Input LOW Current	I_{IL}	V_{IN} = 0V		-	50	µA
Input HIGH Current	I_{IH}	$V_{IN} = V_{DD}$		-	100	µA
Output LOW Voltage	V_{OL}	Standard drive	I_{OL} = 8mA	-	0.4	V
		High drive	I_{OL} = 12mA (-1H)			
Output HIGH Voltage	V_{OH}	Standard drive	I_{OH} = -8mA	2.4	-	V
		High drive	I_{OH} = -12mA (-1H)			
Power Down Current	I_{DD_PD}	REF = 0MHz		-	12	µA
Supply Current	I_{DD}	Unloaded outputs at 66.66MHz		-	32	mA

Table 4. Switching Characteristics (2305-1) – Commercial [1][2]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	t1	10pF Load	10	-	133	MHz
		30pF Load	10	-	100	
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
Rise Time	t3	Measured between 0.8V and 2V	-	-	2.5	ns
Fall Time	t4	Measured between 0.8V and 2V	-	-	2.5	ns
Output to Output Skew	t5	All outputs equally loaded	-	-	250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	t6	Measured at $V_{DD}/2$	-	0	±350	ps
Device-to-Device Skew	t7	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	-	0	700	ps
Cycle-to-Cycle Jitter, peak–peak	t_J	Measured at 66.66MHz, loaded outputs	-	-	200	ps
PLL Lock Time	t_{LOCK}	Stable power supply, valid clock presented on REF pin	-	-	1	ms

1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

Table 5. Switching Characteristics (2305-1H) – Commercial [1][2]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	t1	10pF Load	10	-	133	MHz
		30pF Load	10	-	100	
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 50MHz	45	50	55	%
Rise Time	t3	Measured between 0.8V and 2V	-	-	1.5	ns
Fall Time	t4	Measured between 0.8V and 2V	-	-	1.5	ns
Output to Output Skew	t5	All outputs equally loaded	-	-	250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	t6	Measured at V_{DD}/2	-	0	±350	ps
Device-to-Device Skew	t7	Measured at V_{DD}/2 on the CLKOUT pins of devices	-	0	700	ps
Output Slew Rate		Measured between 0.8V and 2V using Test Circuit #2	1	-	-	V/ns
Cycle-to-Cycle Jitter, peak–peak	t_J	Measured at 66.66MHz, loaded outputs	-	-	200	ps
PLL Lock Time	t_{LOCK}	Stable power supply, valid clock presented on REF pin	-	-	1	ms

1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

2.4 Electrical Specifications – Industrial

Table 6. DC Electrical Characteristics – Industrial

Parameter	Symbol	Conditions		Minimum	Maximum	Unit
Input LOW Voltage Level	V_{IL}	-		-	0.8	V
Input HIGH Voltage Level	V_{IH}	-		2	-	V
Input LOW Current	I_{IL}	V_{IN} = 0V		-	50	µA
Input HIGH Current	I_{IH}	V_{IN} = V_{DD}		-	100	µA
Output LOW Voltage	V_{OL}	Standard drive	I_{OL} = 8mA	-	0.4	V
		High drive	I_{OL} = 12mA (-1H)			
Output HIGH Voltage	V_{OH}	Standard drive	I_{OH} = -8mA	2.4	-	V
		High drive	I_{OH} = -12mA (-1H)			
Power Down Current	I_{DD_PD}	REF = 0MHz		-	25	µA
Supply Current	I_{DD}	Unloaded outputs at 66.66MHz		-	35	mA

Table 7. Switching Characteristics (2305-1) – Industrial[1][2]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	t1	10pF Load	10	-	133	MHz
		30pF Load	10	-	100	
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
Rise Time	t3	Measured between 0.8V and 2V	-	-	2.5	ns
Fall Time	t4	Measured between 0.8V and 2V	-	-	2.5	ns
Output to Output Skew	t5	All outputs equally loaded	-	-	250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	t6	Measured at V_{DD}/2	-	0	±350	ps
Device-to-Device Skew	t7	Measured at V_{DD}/2 on the CLKOUT pins of devices	-	0	700	ps
Cycle-to-Cycle Jitter, peak–peak	t_J	Measured at 66.66MHz, loaded outputs	-	-	200	ps
PLL Lock Time	t_{LOCK}	Stable power supply, valid clock presented on REF pin	-	-	1	ms

1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

Table 8. Switching Characteristics (2305-1H) – Industrial [1][2]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output Frequency	t1	10pF Load	10	-	133	MHz
		30pF Load	10	-	100	
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 66.66MHz	40	50	60	%
Duty Cycle = t2 ÷ t1	-	Measured at 1.4V, F_{OUT} = 50MHz	45	50	55	%
Rise Time	t3	Measured between 0.8V and 2V	-	-	1.5	ns
Fall Time	t4	Measured between 0.8V and 2V	-	-	1.5	ns
Output to Output Skew	t5	All outputs equally loaded	-	-	250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	t6	Measured at V_{DD}/2	-	0	±350	ps
Device-to-Device Skew	t7	Measured at V_{DD}/2 on the CLKOUT pins of devices	-	0	700	ps
Output Slew Rate		Measured between 0.8V and 2V using Test Circuit #2	1	-	-	V/ns
Cycle-to-Cycle Jitter, peak–peak	t_J	Measured at 66.66MHz, loaded outputs	-	-	200	ps
PLL Lock Time	t_{LOCK}	Stable power supply, valid clock presented on REF pin	-	-	1	ms

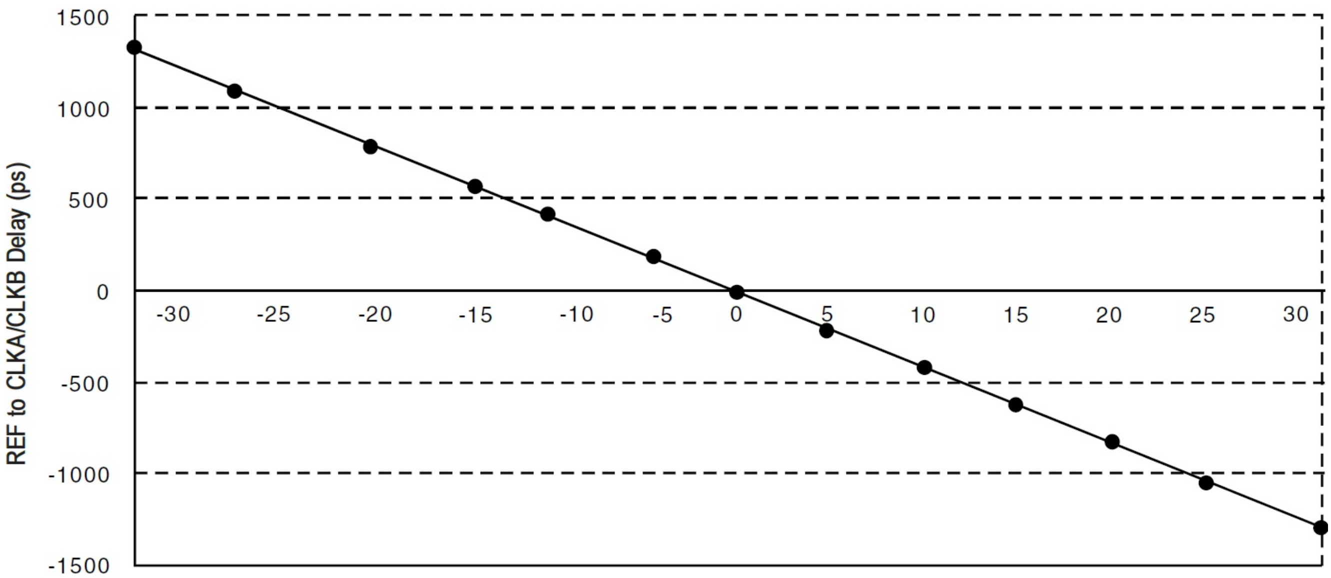
1. REF Input has a threshold voltage of V_{DD}/2.
2. All parameters specified with loaded outputs.

3. Zero-Delay and Skew Control

All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay. The Output Load Difference diagram illustrates the PLLs relative loading with respect to the other outputs that can adjust the Input-Output (I/O) Delay.

For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. If I/O Delay adjustments are needed, use the Output Load Difference diagram to calculate loading differences between the CLKOUT pin and other outputs. For zero output-to-output skew, all outputs must be loaded equally.

REF TO CLKA/CLKB RELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS



OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS (pF)

4. Switching Waveforms

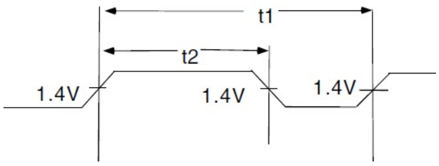


Figure 3. Duty Cycle Timing

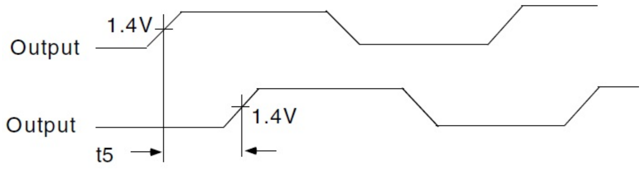


Figure 4. Output-to-Output Skew

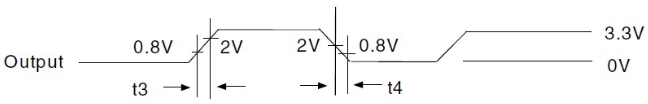


Figure 5. All Outputs Rise/Fall Time

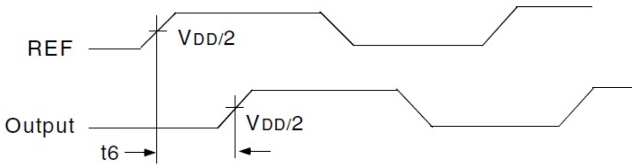


Figure 6. Input-to-Output Propagation Delay

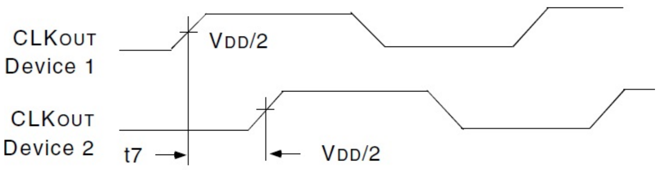


Figure 7. Device-to-Device Skew

5. Test Circuits

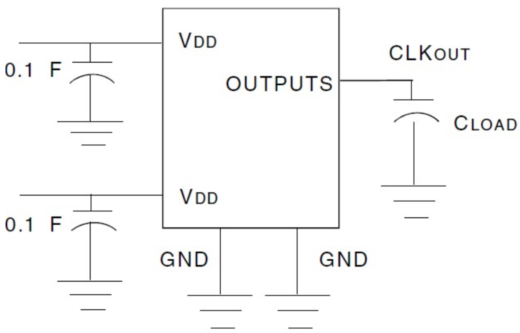


Figure 8. Test Circuit 1 (all parameters except t8)

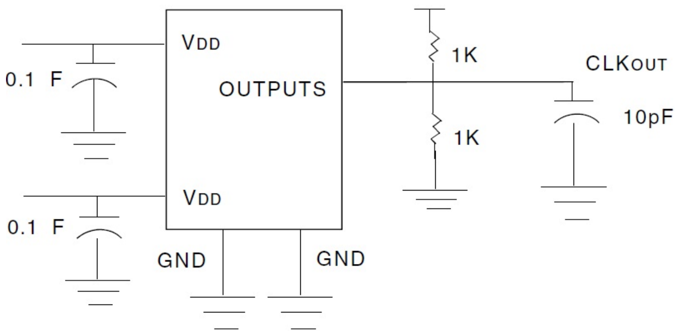


Figure 9. Test Circuit 2 (t8, Output Slew Rate on -1H devices)

6. Typical Duty Cycle and IDD Trends for 2305-1

- Duty cycle is taken from a typical chip measurement at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current and where:
  n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz).

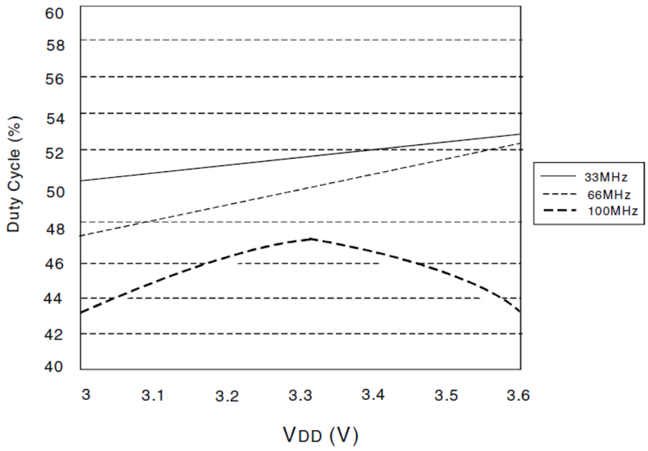


Figure 10. Duty Cycle vs VDD (30pF loads over frequency – 3.3V, 25°C)

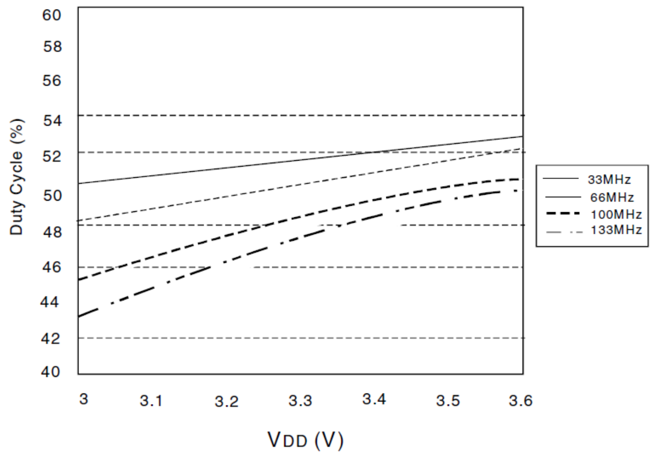


Figure 11. Duty Cycle vs VDD (10pF loads over frequency – 3.3V, 25°C)

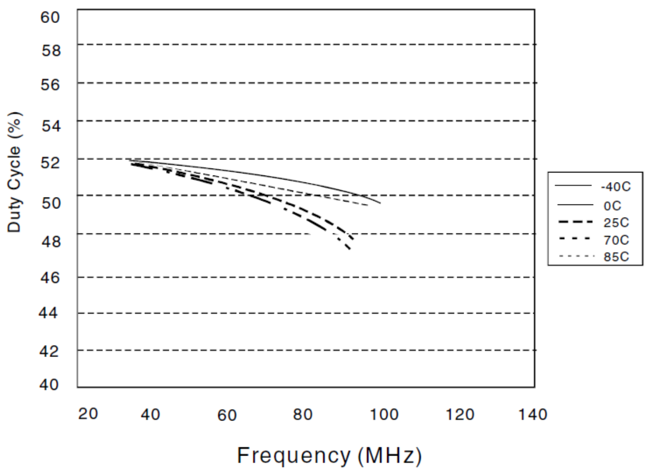


Figure 12. Duty Cycle vs Frequency (30pF loads over temperature – 3.3V)

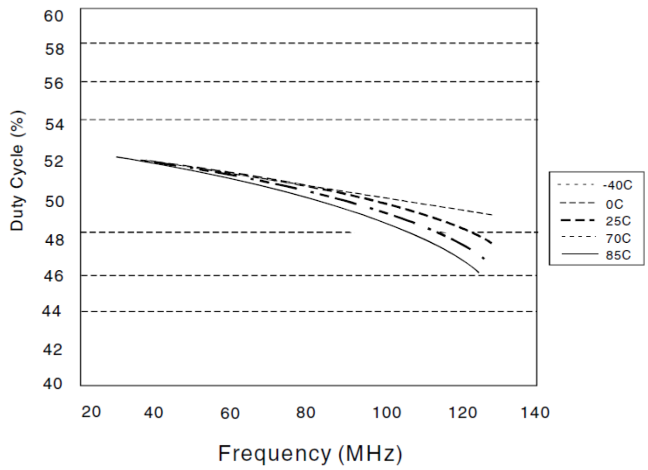


Figure 13. Duty Cycle vs Frequency (10pF loads over temperature – 3.3V)

- Duty cycle is taken from a typical chip measurement at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current and where: n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz).

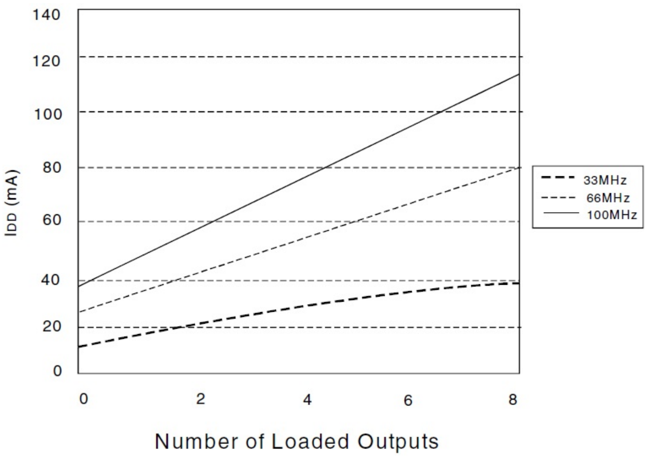


Figure 14. IDD vs Number of Loaded Outputs (for 30pF loads over frequency – 3.3V, 25°C)

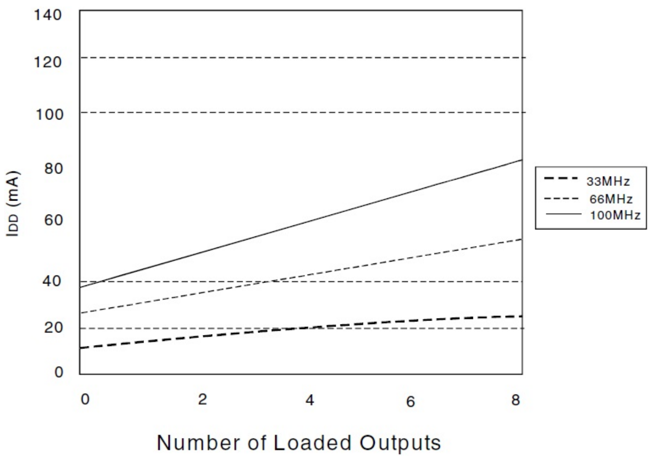


Figure 15. IDD vs Number of Loaded Outputs (for 10pF loads over frequency – 3.3V, 25°C)

7. Typical Duty Cycle and IDD Trends for 2305-1H

- Duty cycle is taken from a typical chip measurement at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current and where: n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz).

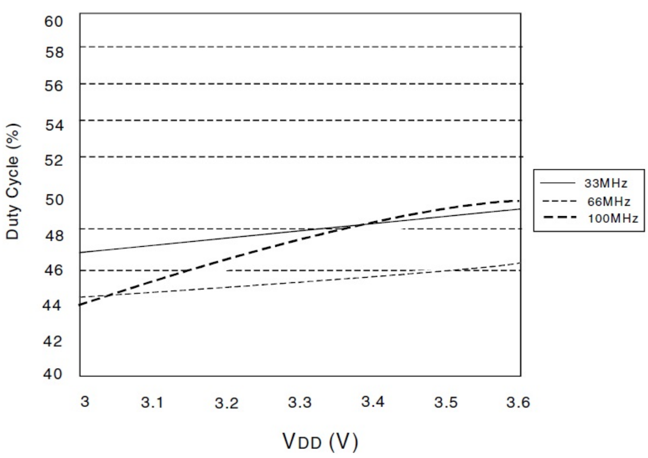


Figure 16. Duty Cycle vs VDD (30pF loads over frequency – 3.3V, 25°C)

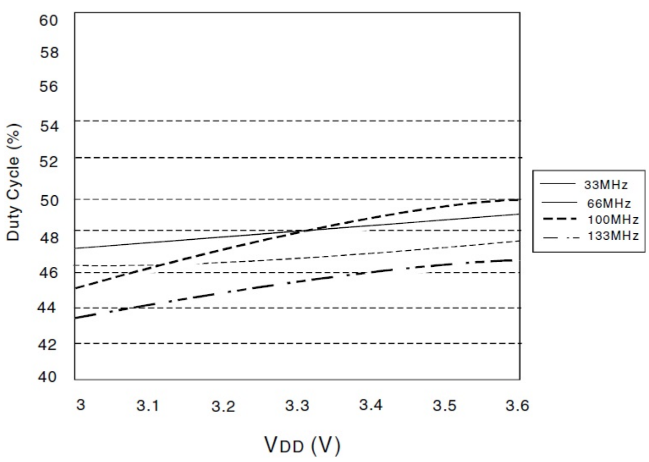


Figure 17. Duty Cycle vs VDD (10pF loads over frequency – 3.3V, 25°C)

- Duty cycle is taken from a typical chip measurement at 1.4V.
- I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current and where:
  n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz).

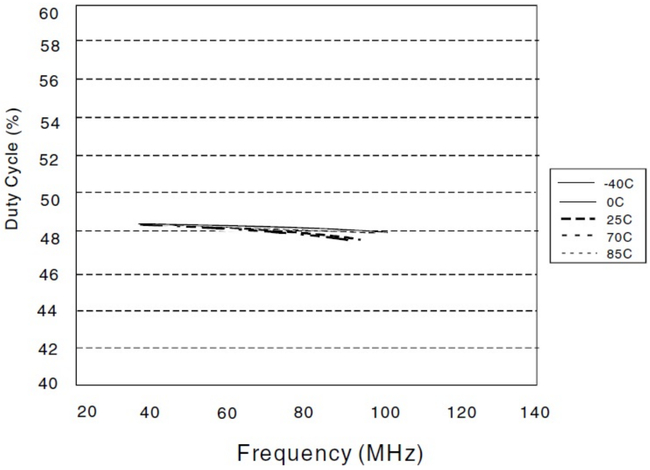


Figure 18. Duty Cycle vs Frequency (30pF loads over temperature – 3.3V)

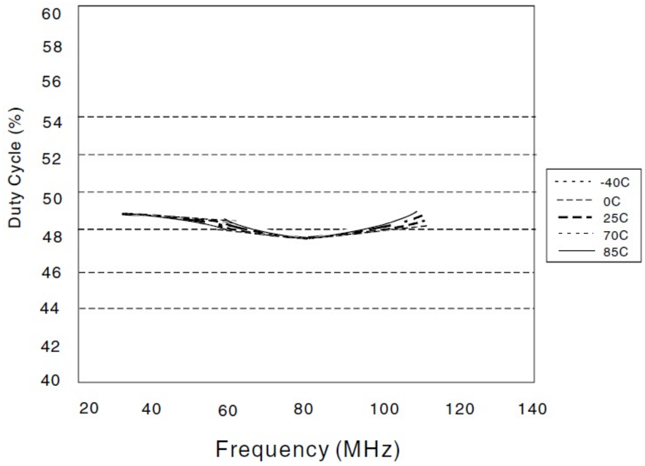


Figure 19. Duty Cycle vs Frequency (10pF loads over temperature – 3.3V)

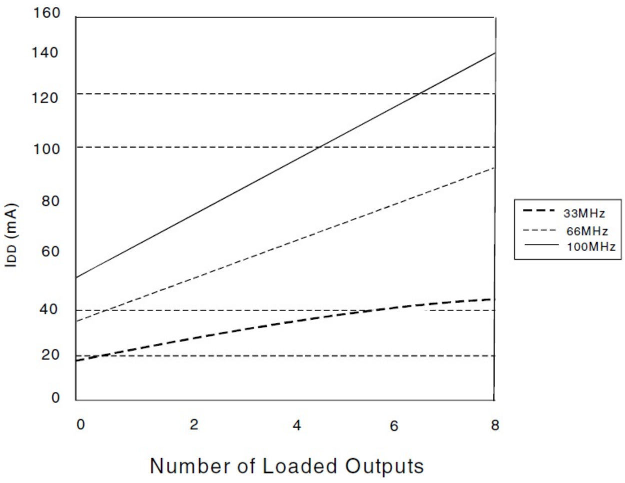


Figure 20. IDD vs Number of Loaded Outputs (for 30pF loads over frequency – 3.3V, 25°C)

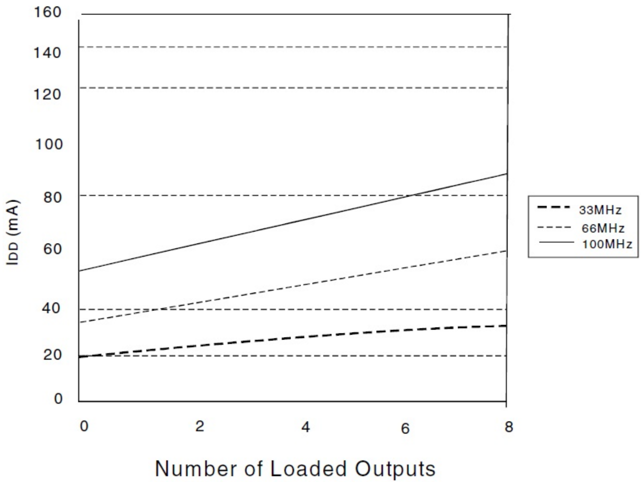


Figure 21. IDD vs Number of Loaded Outputs (for 10pF loads over frequency – 3.3V, 25°C)

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

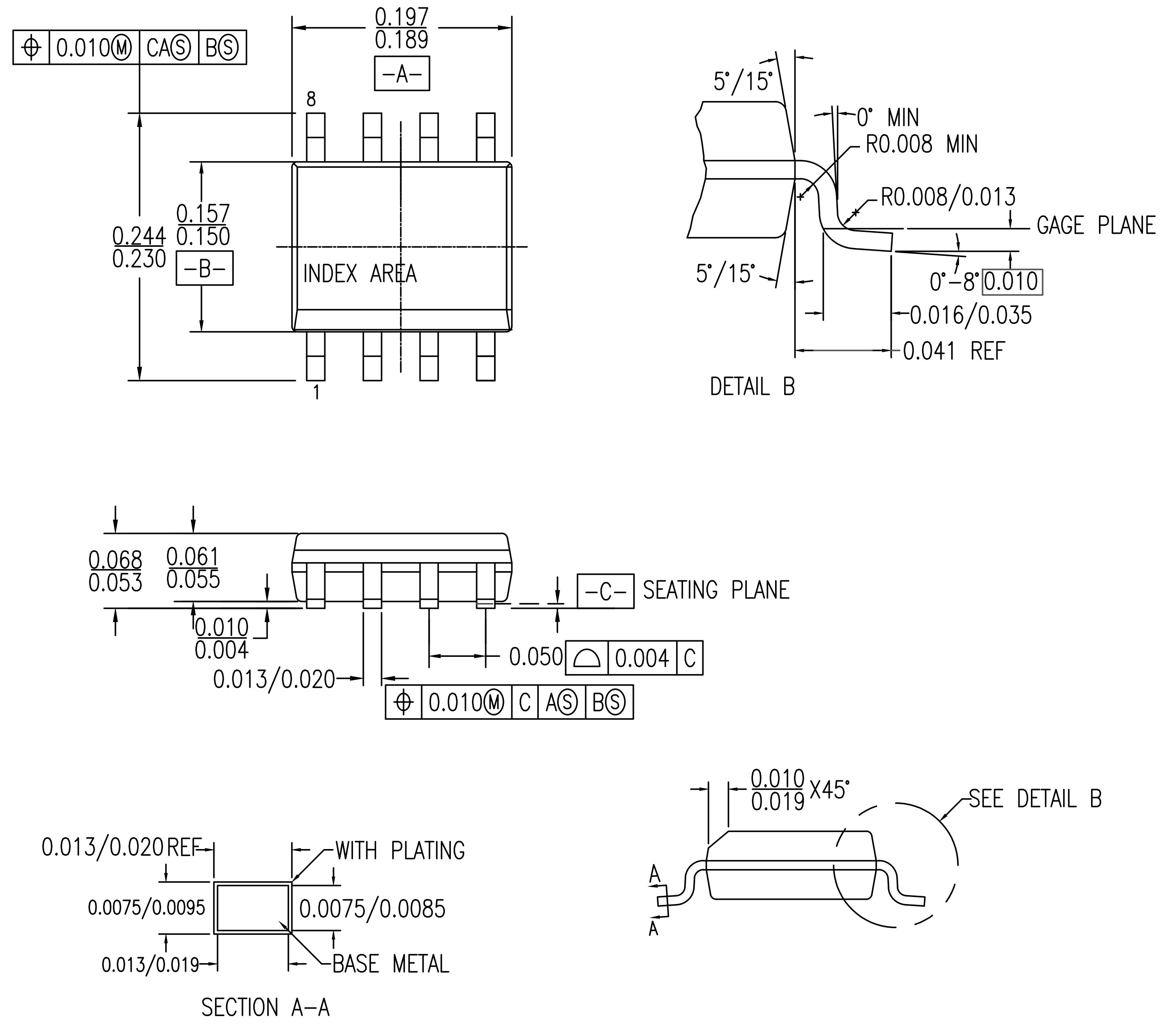
9. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
2305-1DCG8[1]	8-SOIC, 0.150" body, 0.050" pitch	Tape and Reel	0 to +70°C
2305-1DCG		Tray	
2305-1DCGI8[1]	8-SOIC, 0.150" body, 0.050" pitch	Tape and Reel	-40 to +85°C
2305-1DCGI		Tray	
2305-1HDCG8[1]	8-SOIC, 0.150" body, 0.050" pitch	Tape and Reel	0 to +70°C
2305-1HDCG		Tray	
2305-1HDCGI8[1]	8-SOIC, 0.150" body, 0.050" pitch	Tape and Reel	-40 to +85°C
2305-1HDCGI		Tray	
2305-1PGGI	8-TSSOP, 4.4 × 3.0 mm, 0.65mm pitch	Tray	-40 to +85°C
2305-1PGG		Tray	0 to +70°C

1. 3000 pieces per reel in tape and reel form.
2. G = lead-free, RoHS compliant.

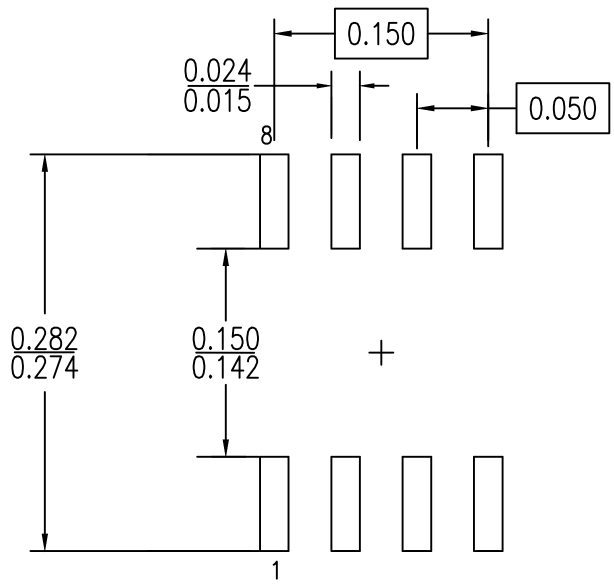
10. Revision History

Revision	Date	Description
1.00	Jan 7, 2025	▪ Reformatted to the latest Renesas template. ▪ Updated Package Outline Drawings section and added links to PODs in Ordering Information. ▪ Added note for tape and reel quantity after Ordering Information.
-	Aug 16, 2012	Previous released version of datasheet.



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES



RECOMMENDED LAND PATTERN DIMENSION

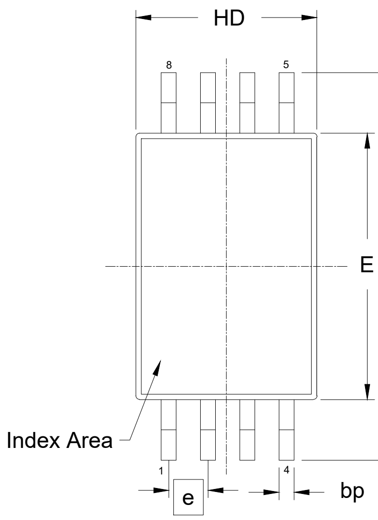
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN INCHES

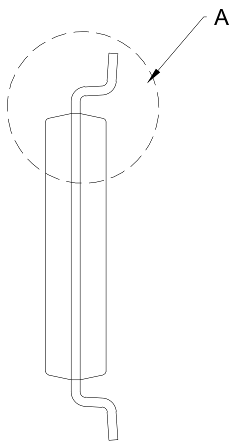
Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 01	Dedicate to Package DCG8 Only
Feb 24, 2016	Rev 00	Initial Release

Package Outline Drawing

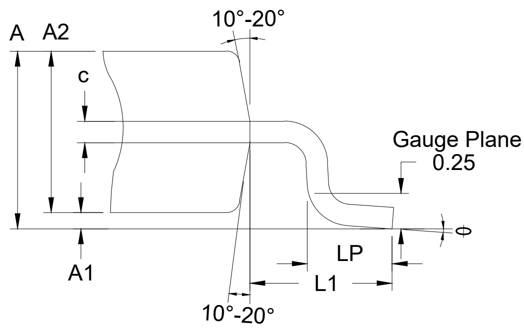
Package Code: PGG8D1
8-TSSOP 4.4 x 3.0 x 1.0 mm Body, 0.65mm Pitch
PSC-4768-01, Revision: 02, Date Created: Apr 29, 2024



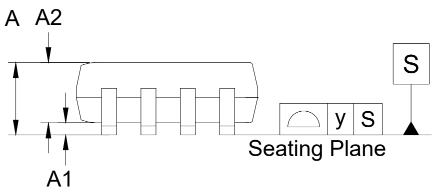
TOP VIEW



SIDE VIEW

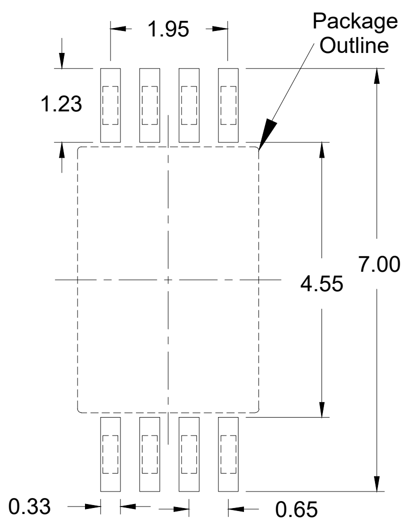


Detail A
(Rotated 90° CW)



SIDE VIEW

Reference Symbol	Dimension in mm		
	Min	Nom	Max
E	4.30	4.40	4.50
A2	0.80	-	1.05
HD	2.90	3.00	3.10
HE	6.20	6.40	6.60
A	0.85	-	1.20
A1	0.05	0.10	0.15
bp	0.19	0.25	0.30
c	0.09	-	0.20
θ	0.00	-	8.00
e	0.65 BSC		
y	-	-	0.10
LP	0.50	0.625	0.75
L1	-	1.00	-



RECOMMENDED LAND PATTERN
(PCB Top View, SMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.