IS-2100ARH, IS-2100AEH

Radiation Hardened High Frequency Half Bridge Drivers

FN9037
Rev 3.00
May 10, 2016

The radiation hardened IS-2100ARH, IS-2100AEH are high frequency, 130V half bridge N-Channel MOSFET driver ICs, which are functionally similar to industry standard 2110 types. The low-side and high-side gate drivers are independently controlled. This gives the user maximum flexibility in dead time selection and driver protocol.

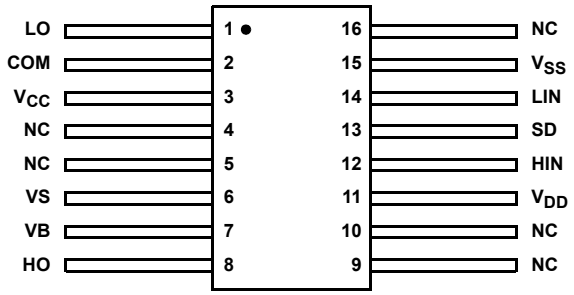
In addition, the devices have on-chip error detection and correction circuitry, which monitors the state of the high-side latch and compares it to the HIN signal. If they disagree, a set or reset pulse is generated to correct the high-side latch. This feature protects the high-side latch from single event upsets (SEUs).

Applications

- High frequency switch-mode power supplies
- Drivers for inductive loads
- DC motor drivers

Pin Configuration

IS-2100ARH, IS-2100AEH
FLATPACK (CDFP4-F16)
TOP VIEW



Features

- Electrically screened to DLA SMD # 5962-99536
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - Maximum total dose . . . . . 300krad(Si)
  - DI RSG process provides latch-up immunity
  - SEU rating . . . . . 82MeV/mg/cm^2
  - Vertical device architecture reduces sensitivity to low dose rates
- Bootstrap supply maximum voltage to 150V
- Drives 1000pF load at 1MHz with rise and fall times of 30ns (typical)
- 1.5A (typical) peak output current
- Independent inputs for non-half bridge topologies
- Low DC power consumption . . . . . 60mW (typical)
- Operates with V_{DD} = V_{CC} over 12V to 20V range
- Low-side supply undervoltage protection

Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9953602V9A	IS0-2100ARH-Q	-55 to +125	Die	
5962F9953602VXC	IS9-2100ARH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9953602QXC	IS9-2100ARH-8	-55 to +125	16 Ld Flatpack	K16.A
N/A	IS9-2100ARH/Proto	-55 to +125	16 Ld Flatpack	K16.A
5962F9953603VXC	IS9-2100AEH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9953603V9A	IS0-2100AEH-Q	-55 to +125	Die	

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table must be used when ordering.

Die Characteristics

DIE DIMENSIONS:

4820µm x 3300µm (190 mils x 130 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

Top Metallization:

Type: ALSiCu
Thickness: 16.0kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

$< 2.0 \times 10^5$ A/cm^2

Transistor Count:

542

Metallization Mask Layout

IS-2100ARH, IS-2100AEH

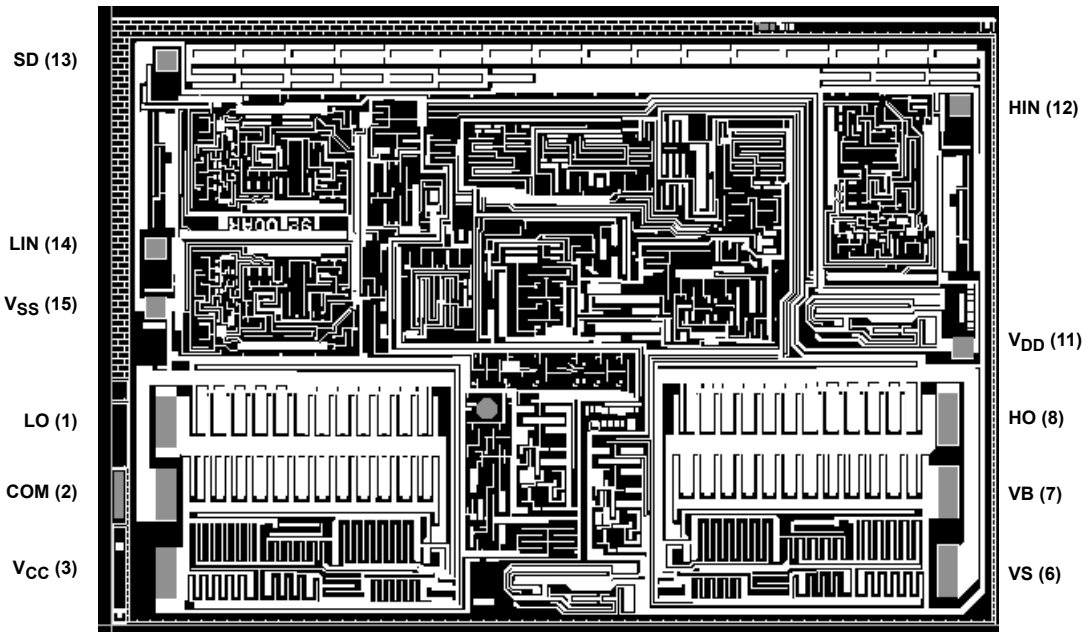


TABLE 1. IS-2100ARH, ISL-2100AEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PAD CENTER		PAD SIZE	
		X (µm)	Y (µm)	DX (µm)	DY (µm)
3	VCC	296.5	270	109	280
6	VS	4561	284.5	109	280
7	VB	4561	711	109	280
8	HO	4561	1079	109	280
11	VDD	4645.5	1500	109	109
12	HIN	4627.5	2817	109	109
13	SD	302	3064.5	109	109
14	LIN	237.5	2040	109	109
15	VSS	239	1719	109	109
1	LO	296.5	1095	109	280
2	COM	296.5	697	109	280

NOTE: Origin of coordinates is the lower left corner of the die.

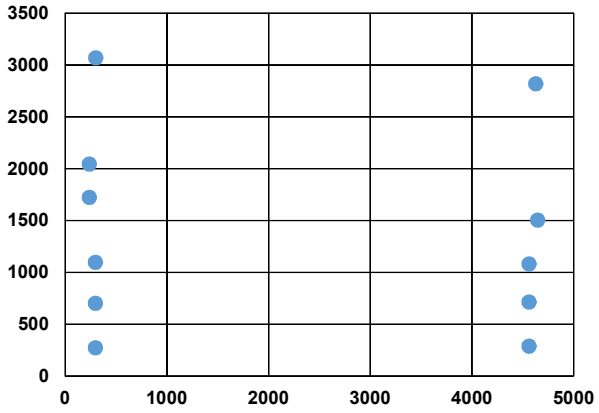


FIGURE 1. XY PAD CENTER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 10, 2016	FN9037.3	Updated Ordering information table by applying new standards and adding Notes 1 and 2. Added Table 1 on page 4. Added Package Outline Drawing K16.A.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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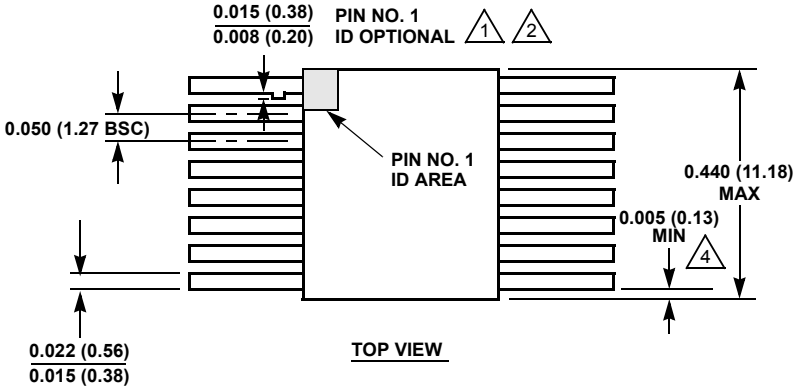
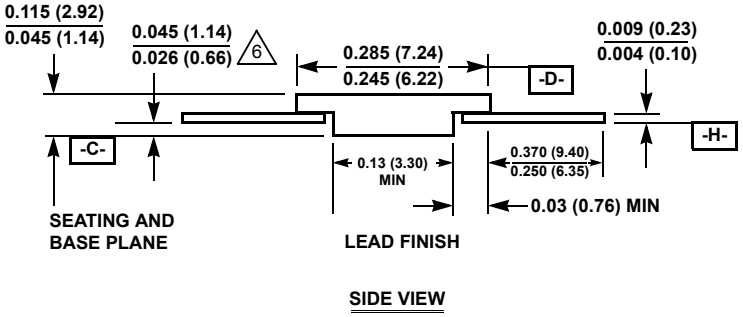
Package Outline Drawing

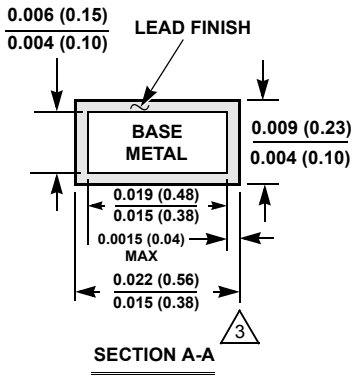
K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.