Datasheet

IS-1715ARH, IS-1715AEH

Radiation Hardened Complementary Switch FET Drivers

The radiation hardened IS-1715ARH and IS-1715AEH are high speed, high current, complementary power FET drivers designed for use in synchronous rectification circuits. Soft switching transitions for the two output waveforms can be managed by setting the independently programmable delays. Alternatively, the delay pins can be configured for zero-voltage sensing to allow for precise switching control.

The IS-1715ARH and IS-1715AEH have a single input, which is PWM and TTL compatible, and can run at frequencies up to 1MHz. The AUX output switches immediately at the rising edge of the INPUT, but waits for the T2 delay before responding to the falling edge. A logic low on the enable pin (ENBL) places both outputs into an active-low mode, and an Undervoltage Lockout (UVLO) function is set at 9V (maximum).

These devices are constructed with the dielectrically isolated Rad Hard Silicon Gate (RSG) process and are immune to Single Event Latch-Up (SEL). They have been specifically designed to provide highly reliable performance in harsh radiation environments.

Applications

- Synchronous rectification in power supplies

Features

- Electrically screened to SMD #5962-00521
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - ○ Gamma dose 3x10^5rad(Si)
  - ○ Latch-up immune
- PWR output current (source and sink): 3A (peak)
- AUX output current (source and sink): 3A (peak)
- Low operating supply current: 6mA (max)
- Wide programmable delay range: 100ns to 600ns
- Configurable for zero-voltage switching
- Switching frequency to 1MHz
- Both outputs active-low in Sleep mode
- 9V (maximum) UVLO

Related Literature

For a full list of related documents, visit our website:

- IS-1715ARH, IS-1715AEH device pages

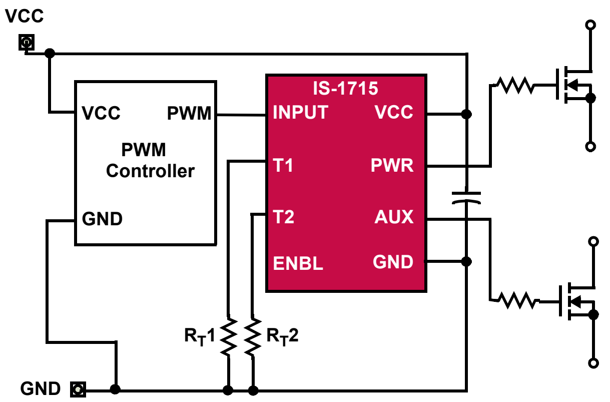


Figure 1. IS-1715 Typical Application Diagram

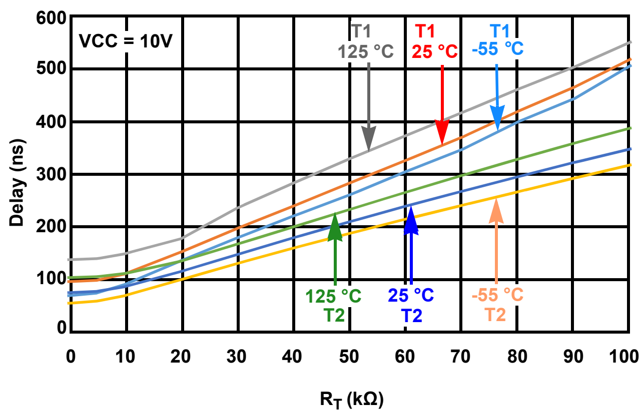
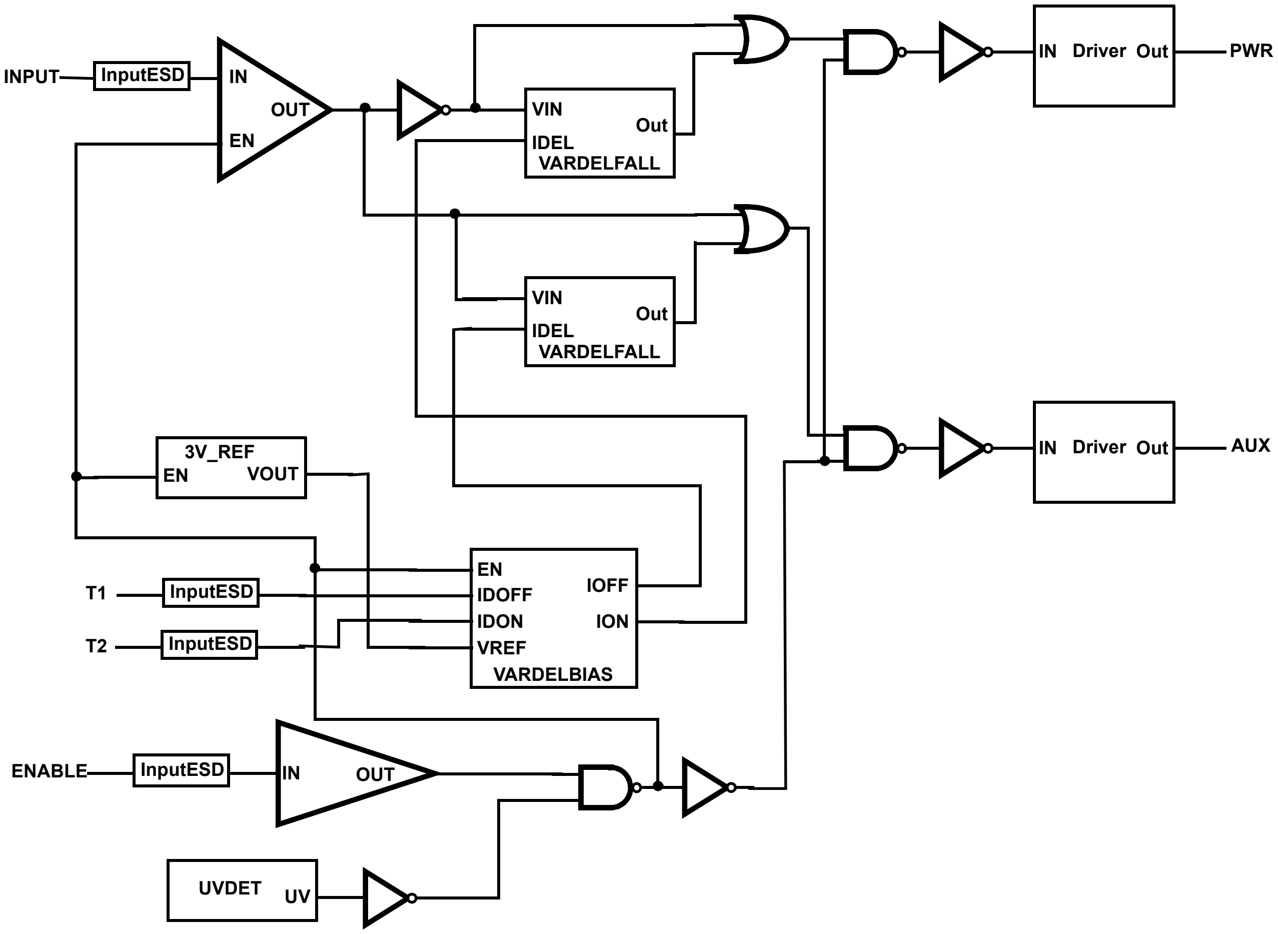


Figure 2. T1 Delay, T2 Delay vs R_T vs Temperature

1. Overview

1.1 Functional Block Diagram



Note: VCC and VSS (GND) connections not shown.

Figure 3. Functional Block Diagram

1.2 Ordering Information

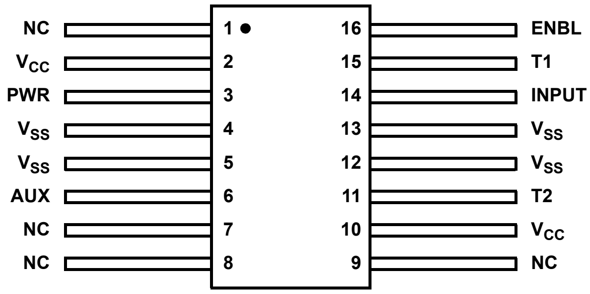
Ordering SMD Number (Note 1)	Part Number (Note 2)	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
5962F0052101VXC	IS9-1715ARH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F0052101QXC	IS9-1715ARH-8	-55 to +125	16 Ld Flatpack	K16.A
5962R0052101TXC	IS9-1715ARH-T	-55 to +125	16 Ld Flatpack	K16.A
5962F0052101V9A	IS0-1715ARH-Q (Note 3)	-55 to +125	Die	N/A
N/A	IS0-1715ARH/SAMPLE (Notes 3, 4)	-55 to +125	Die	N/A
N/A	IS9-1715ARH/PROTO (Note 4)	-55 to +125	16 Ld Flatpack	K16.A
5962F0052103VXC	IS9-1715AEH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F0052103V9A	IS0-1715AEH-Q (Note 3)	-55 to +125	Die	N/A

Notes:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 5.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

1.3 Pin Configuration

Flatpack (CDFP4-F16)
Top View



1.4 Pin Description

Pin Number	Pin Name	Description
1, 7, 8, 9	NC	No connection.
2, 10	V_{CC}	Chip positive supply (10V to 18V).
3	PWR	Output. PWR switches immediately (neglecting propagation delay) at INPUT's falling edge but is delayed after the rising edge by the value of the resistance on T1. PWR is capable of sinking and sourcing 3.0A of peak gate drive current. During sleep mode, PWR is active low.
4, 5, 12,13	V_{SS}	Chip negative supply (ground connection).
6	AUX	Output. AUX switches immediately (neglecting propagation delay) at INPUT's rising edge but is delayed after the falling edge before switching by the value of the resistance on T2. AUX is capable of sinking and sourcing 3.0A of peak gate drive current. During sleep mode, AUX is active low.
11	T2	Input. A resistor to ground programs the time delay between PWR switch turn-off and AUX turn-on.
14	INPUT	Input. INPUT switches at TTL logic levels but the allowable range is from 0V to VCC, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.
15	T1	Input. A resistor to ground programs the time delay between AXU switch turn-off and PWR turn-on.
16	ENBL	Input. The ENABLE input switches at TTL logic levels, but the allowable range is from 0 to VCC. The ENABLE input places the device into sleep mode when it is a logic low. The current into VCC during sleep mode is typically 500µA.
N/A	LID	No connection (floating).

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage Range (VCC)	10	20	VDC
DC Input Voltage Range (INPUT, ENBL)	0	VCC	VDC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld FP Package (Notes 5, 6)	90	18

Notes:
5. θ_{JA} is measured with the component mounted to a high effective thermal conductivity test board in free air. See TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.

Parameter	Minimum	Maximum	Unit
Lead Temperature (soldering, 10 seconds)		+265	°C
Maximum Junction Temperature (T_{JMAX})		+175	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage Range (VCC)	10	18	VDC
Temperature Range	-55	+125	°C

2.4 Electrical Specifications

V_{CC} = 10V to 18V, ENBL ≥ 3V, Limits apply over the operating temperature range, -55°C to +125°C unless otherwise specified.

Description	Parameter	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Overall						
Operating Voltage Range	V_{CC}		10	-	18	V
Input Current, Nominal	I_{CC}	ENBL = 3.0V	1.0	-	6.0	mA
Input Current, Sleep Mode	I_{CCS}	ENBL = 0.8V	300	-	900	µA
Under Voltage, Rising Threshold	UV+		8.5	-	9.5	V
Under Voltage, Falling Threshold	UV-		7.7	-	8.8	V
Under Voltage Delta	UVD		0	-	2.0	V
Power Driver (PWR)						
Pre Turn-On PWR Output, Low	V_{PPWR}	V_{CC} = 0V, ENBL ≤ 0.8V, I_{OUT} = 10mA	-	-	2.0	V
PWR Pin Output Low, Saturation	V_{PWR}	INPUT = 0.8V, I_{OUT} = 40mA	-	-	1.0	V
		INPUT = 0.8V, I_{OUT} = 100mA	-	-	1.5	V
PWR Pin Output High, Saturation	V_{CC} - V_{PWR}	INPUT = 3.0V, I_{OUT} = -40mA	-	-	1.0	V
		INPUT = 3.0V, I_{OUT} = -100mA	-	-	1.5	V
Rise Time	t_{RP}	C_L = 2200pF	15	-	50	ns

V_{CC} = 10V to 18V, ENBL ≥ 3V, Limits apply over the operating temperature range, -55°C to +125°C unless otherwise specified. **(Continued)**

Description	Parameter	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Fall Time	t_{FP}	C_L = 2200pF	15	-	50	ns
T1 Input Pin Delay, AUX to PWR	t_{T1}	INPUT Rising Edge, R_{T1} = 10kΩ, (Figure 4)(Note 8)	45	-	200	ns
		INPUT Rising Edge, R_{T1} = 100kΩ, (Figure 4)(Note 8)	250	-	1300	ns
PWR Propagation Delay	t_{DP}	INPUT Falling Edge, 50% Points, (Figure 4)(Note 9)	50	-	300	ns
Auxiliary (AUX)						
AUX Pre Turn-On AUX Output, Low	V_{PAUX}	V_{CC} = 0V, ENBL ≤ 0.8V, I_{OUT} = 10mA	-	-	2.0	V
AUX Pin Output Low, Saturation	V_{AUX}	INPUT = 3.0V, I_{OUT} = 40mA	-	-	1.0	V
		INPUT = 3.0V, I_{OUT} = 100mA	-	-	1.5	V
AUX Pin Output High, Saturation	V_{CC} - V_{AUX}	INPUT = 0.8V, I_{OUT} = -40mA	-	-	1.0	V
		INPUT = 0.8V, I_{OUT} = -100mA	-	-	1.5	V
Rise Time	t_{RP}	C_L = 2200pF	15	-	50	ns
Fall Time	t_{FP}	C_L = 2200pF	15	-	50	ns
T2 Input Pin Delay, PWR to AUX	t_{T2}	INPUT Falling Edge, R_{T2} = 10kΩ, (Figure 4)(Note 8)	50	-	130	ns
		INPUT Rising Edge, R_{T2} = 100kΩ, (Figure 4)(Note 8)	200	-	700	ns
AUX Propagation Delay	t_{DA}	INPUT Rising Edge at 50% Points, (Figure 4)(Note 9)	50	-	185	ns
Enable (ENBL)						
Input Threshold Voltage	V_{IT}		-	-	2.8	V
Input Current High	I_{IH}	ENABLE = 15V	-10	-	10	µA
Input Current Low	I_{IL}	ENABLE = 0V	-15	-	15	µA
T1 Input						
Current Limit	T_{1CL}	T1 Input = 0V	-5.5	-	-1.6	mA
Nominal Voltage at T1 Pin	T_{1NV}		2.7	-	3.3	V
Minimum T1 Pin Delay	T_{1DM}	T1 Pin = 2.5V	25	-	120	ns
T2 Input						
Current Limit	T_{2CL}	T2 Input = 0V	-5.5	-	-2.1	mA
Nominal Voltage at T2 Pin	T_{2NV}		2.7	-	3.3	V
Minimum T2 Pin Delay	T_{2DM}	T1 Pin = 2.5V	20	-	80	ns
Input						
Input Threshold Voltage	V_{IT}		-	-	2.8	V
Input Current High	I_{IH}	ENABLE = 15V	-10	-	10	µA
Input Current Low	I_{IL}	ENABLE = 0V	-20	-	20	µA

Notes:

7. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
8. T1 delay and T2 delay are defined as the time between the 50% transition point of AUX (PWR) and the 50% transition point of PWR (AUX) with no capacitive load on either output (Figure 4).
9. Propagation delays (t_{DP} and t_{DA}) are measured from the 50% point of the input signal to the 50% point of the output signal's transition with no load on the outputs (Figure 4).

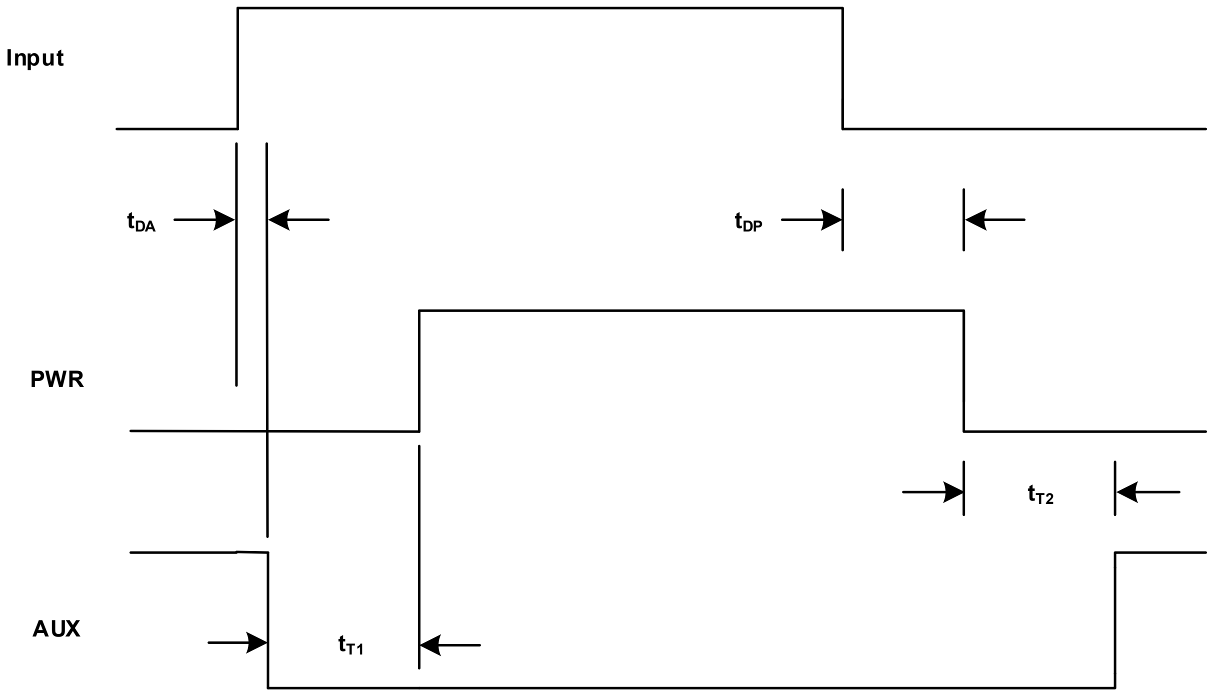


Figure 4. Timing Diagram

3. Typical Performance Curves

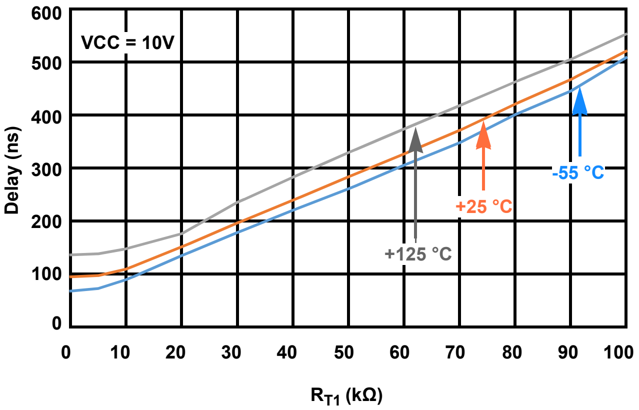


Figure 5. T1 Delay vs R_{T1} vs Temperature

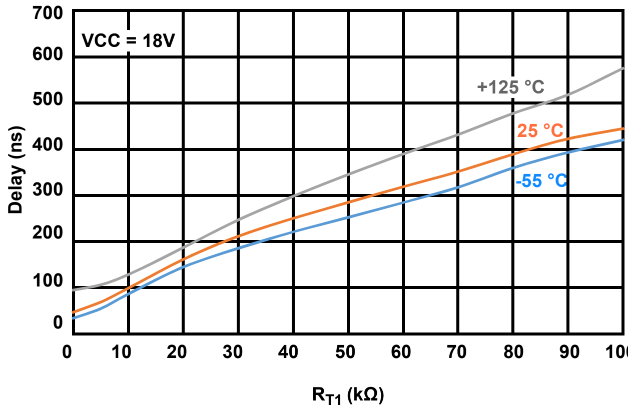


Figure 6. T1 Delay vs R_{T1} vs Temperature

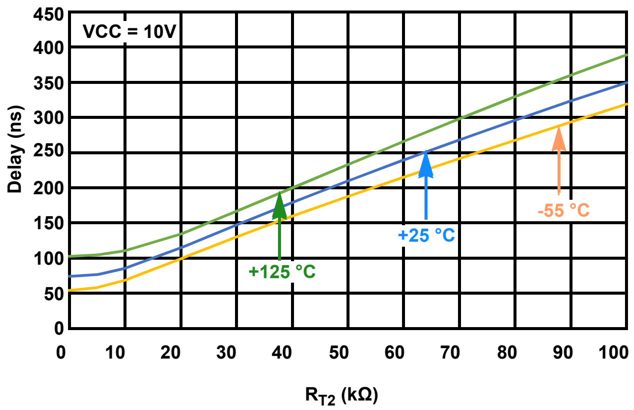


Figure 7. T2 Delay vs R_{T2} vs Temperature

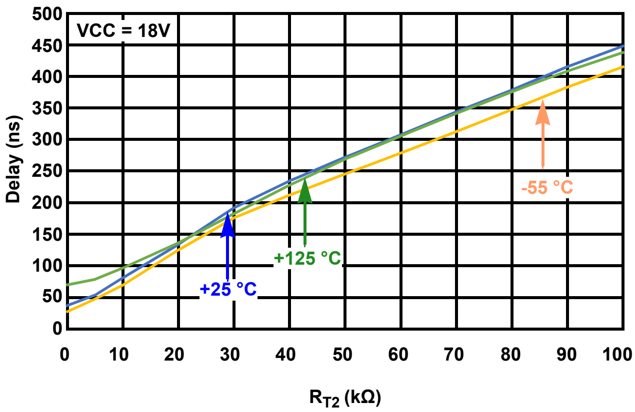


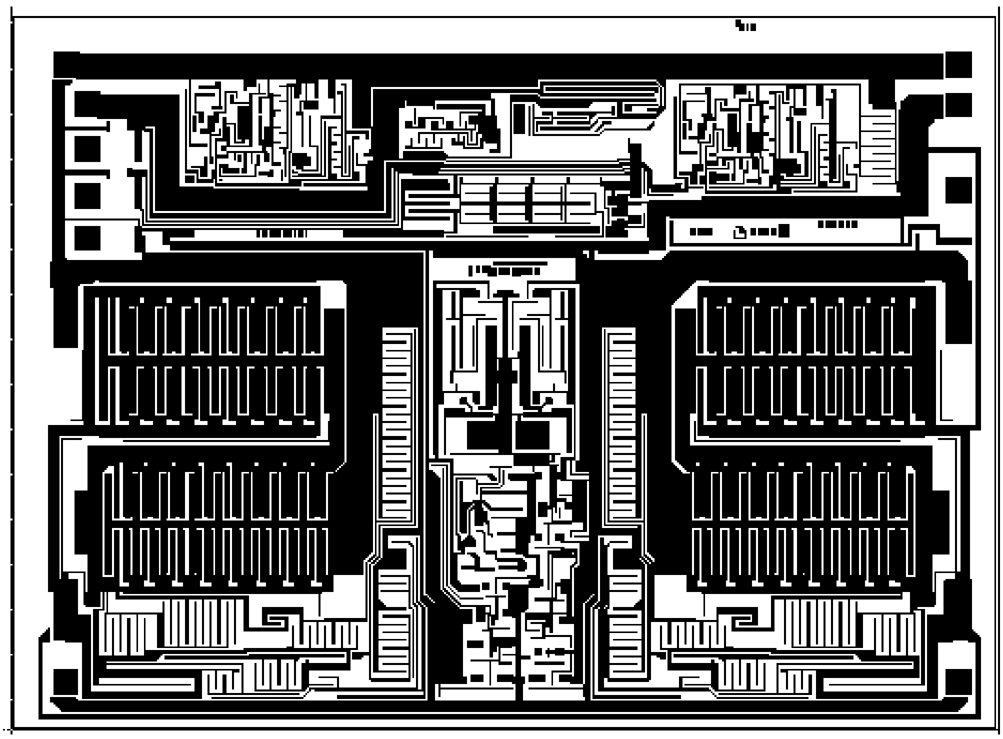
Figure 8. T2 Delay vs R_{T2} vs Temperature

4. Die Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Die Dimensions	3559µm x 4420µm (129 mils x 174 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: Phosphorus Silicon Glass (PSG) Thickness: 8.0kÅ ± 1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ± 2kÅ
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Backside Finish	Silicon
Assembly Related Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	<2.0 x 10^5 A/cm^2
Transistor Count	222

4.1 Metallization Mask Layout



Notes:

10. All double-sized pads should be double bonded.
11. All Pin 2 and Pin 10 VCC pads are bonded to VCC for power and noise considerations (these are lead-frame connected in packaged devices).

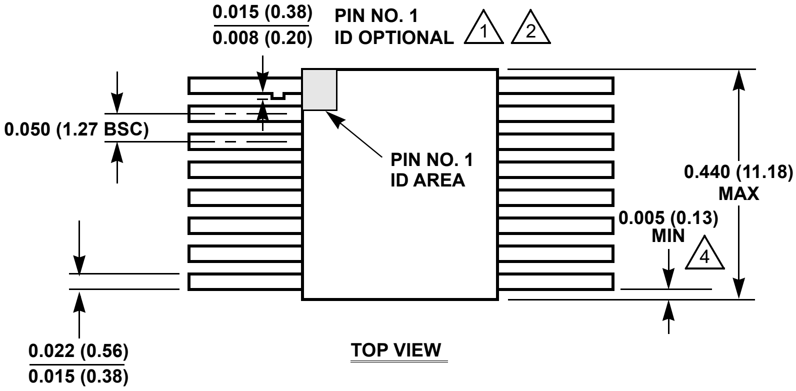
5. Revision History

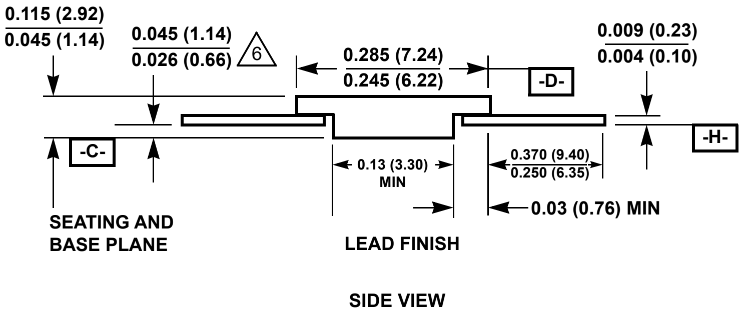
Rev.	Date	Description
5.0	Feb.4.21	Updated Figure 4.
4.0	Jul.22.20	On page 3, Section 1.4 Pin Description Table added new row for the “LID”. On page 7, corrected Figure 4, Timing Diagram.
3.0	Aug.16.19	Updated to new format. Updated links throughout document Updated Ordering information table by correcting package information for IS0-1715ARH/SAMPLE. Updated Disclaimer.
2.0	Dec.21.17	On page 1, added Figure 1 and Figure 2. On page 2, added Functional Block Diagram. On page 4, added table of Pin Descriptions On page 5, added Absolute Maximum Ratings, Thermal Information, and Recommended Operating Conditions. On page 6 and 7, added Electrical Specifications. On page 7, added Timing Diagram. On page 8, added Typical Performance Curves.
1.0	Aug.23.17	Updated to new format. On page 1, added Related Literature. Ordering Information table: Added IS9-1715ARH-T, IS0-1715ARH-Q, IS0-1715ARH/SAMPLE, IS9-1715AEH-Q and IS0-1715AEH-Q Added Package and Pkg Dwg columns Added Notes 1, 2, 3 Added Revision History table, POD K16.A, and About Intersil.

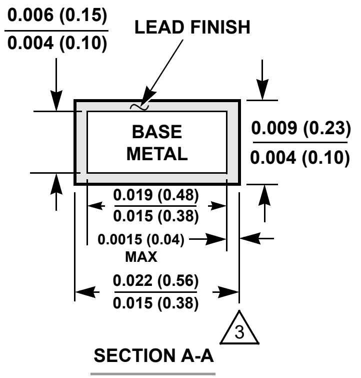
6. Package Outline Drawing

For the most recent package outline drawing, see K16.A.

K16.A
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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Contact Information

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