RENESAS

User Programmable Laser Engine Pixel Clock Generator

Description

The **ICS1574B** is a very high performance monolithic phase-locked loop (PLL) frequency synthesizer designed for laser engine applications. Utilizing ICS's advanced CMOS mixed-mode technology, the **ICS1574B** provides a low cost solution for high-end pixel clock generation for a variety of laser engine product applications.

The pixel clock output (PCLK) frequency is derived from the main clock by a programmable resettable divider.

Operating frequencies are fully programmable with direct control provided for reference divider, feedback divider and post-scaler.

Features

- Supports high resolution laser graphics. PLL/VCO frequency re-programmable through serial interface port to 400 MHz; allows less than ±1.5ns pixel clock resolution.
- Laser pixel clock output is synchronized with conditioned beam detect input
- Ideal for laser printer, copier and FAX pixel clock applications
- On-chip PLL with internal loop filter
- On-chip XTAL oscillator frequency reference
- Resettable, programmable counter gives glitch-free clock alignment
- Single 5 volt power supply
- Low power CMOS technology
- 16-pin 0.150" SOIC package (Pb free available)
- User re-programmable clock frequency supports zoom and gray scale functions

Block Diagram

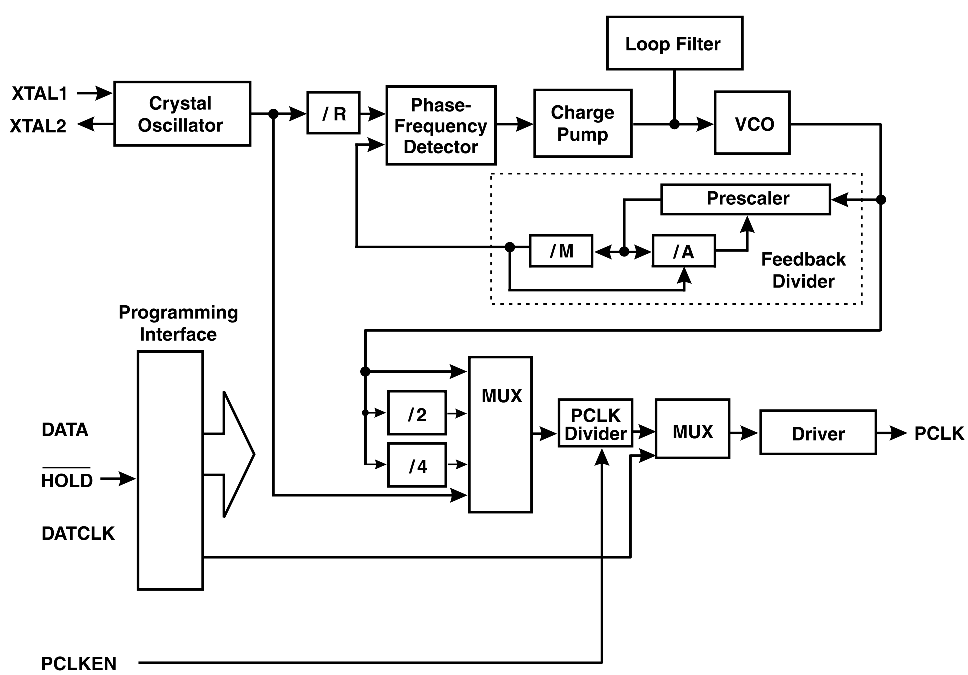
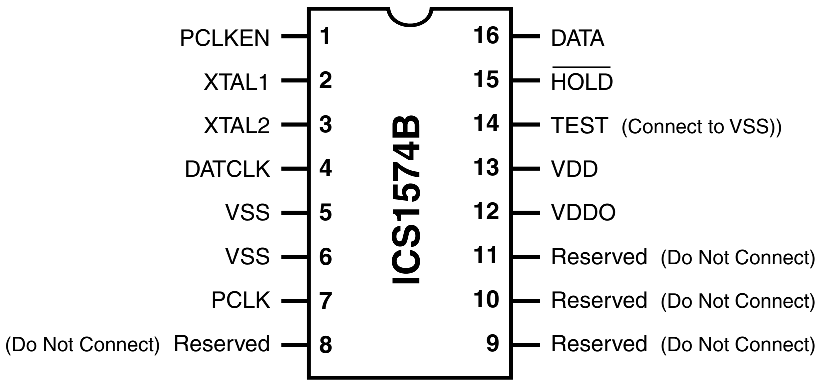


Figure 1

Pin Configuration



16-Pin Skinny SOIC

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
7	PCLK	Pixel clock output.
1	PCLKEN	PCLK Enable (Input).
2	XTAL1	Quartz crystal connection 1 / external reference frequency input.
3	XTAL2	Quartz crystal connection 2.
4	DATCLK	Data Clock (Input).
16	DATA	Serial Register Data (Input).
15	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$ (Input).
14	Test	Test. (Must be connected to VSS.)
8, 9, 10, 11	Reserved	Reserved. (Do Not Connect.)
13	VDD	PLL system power (+5V. See application diagram).
12	VDDO	Output stage power (+5V).
5, 6	VSS	Device ground. (Both pins must be connected.)

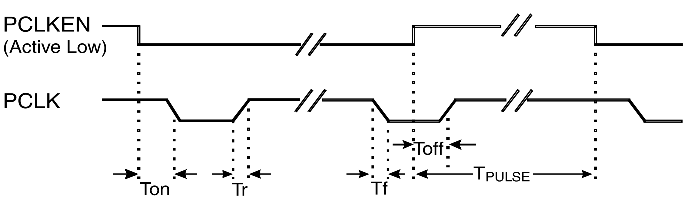
PCLK Programmable Divider

The **ICS1574B** has a programmable divider (referred to in Figure 1 as the PCLK divider) that is used to generate the PCLK clock frequency for the pixel clock output. The modulus of this divider may be set to 3, 4, 5, 6, 8, 10, 12, 16 or 20 under register control. The design of this divider permits the output duty factor to be 50/50, even when an odd modulus is selected. The input frequency to this divider is the output of the PLL post-scaler described below:

The phase of the PCLK output is aligned with the internal high frequency PLL clock (F_{VCO}) immediately after the assertion of the PCLKEN input pulse (active low if PCLKEN_POL bit is 0 or active high if PCLKEN_POL bit is 1).

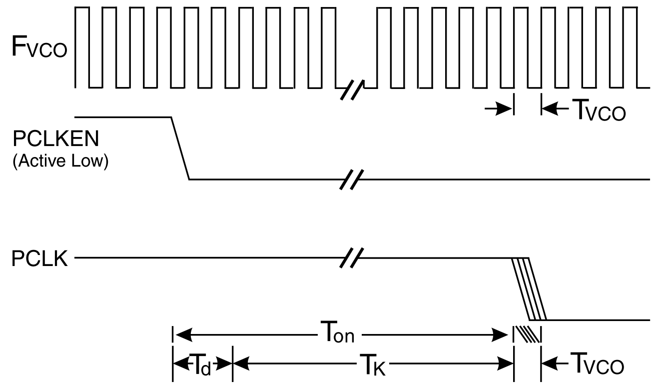
When PCLKEN is deasserted, the PCLK output will complete its current cycle and remain at VDD until the next PCLKEN pulse. The minimum time PCLKEN must be disabled (T_{PULSE}) is $1/F_{PCLK}$.

See Figure 2a for an example of PCLKEN enable (negative polarity) vs. PCLK timing sequences.



$T_{off} < T_{PCLK}$, $T_{PCLK} = 1/F_{PCLK}$
$T_{PULSE} > T_{PCLK}$

Figure 2a



$T_K = K \cdot T_{VCO}$

T_d = LOGIC PROP.DELAY TIME
(typically 9ns with a 10pF load on PCLK)

$T_{VCO} = 1/F_{VCO}$

Figure 2b

The resolution of Ton is one VCO cycle.

The time required for a PCLK cycle start following a PCLKEN enable is described by Figure 2b and the following table:

K Values	
PCLK Divider	**K**
3	2
4a	3.5
4b	3
5	4.5
6	3.5
8a	5.5
8b	5
10	7
12	6.5
16a	9.5
16b	9
20	12

Typical values for Tr and Tf with a 10pF load on PCLK are 1ns.

PLL Post-Scaler

A programmable post-scaler may be inserted between the VCO and the PCLK divider of the **ICS1574B**. This is useful in generating lower frequencies, as the VCO has been optimized for high-frequency operation. The post-scaler is not affected by the PCLKEN input.

The post-scaler allows the selection of:

- VCO frequency
- VCO frequency divided by 2
- VCO frequency divided by 4
- AUX-EN Test Mode

PLL Synthesizer Description — Ratiometric Mode

The **ICS1574B** generates its output frequencies using phase-locked loop techniques. The phase-locked loop (or PLL) is a closed-loop feedback system that drives the output frequency to be ratiometrically related to the reference frequency provided to the PLL (see Figure 1). The reference frequency is generated by an on-chip crystal oscillator or the reference frequency may be applied to the **ICS1574B** from an external frequency source.

The phase-frequency detector shown in the block diagram drives the voltage-controlled oscillator, or VCO, to a frequency that will cause the two inputs to the phase-frequency detector to be matched in frequency and phase. This occurs when:

$$F_{(VCO)}: = \frac{F(XTAL1) \bullet \text{Feedback Divider}}{\text{Reference Divider}}$$

This expression is exact; that is, the accuracy of the output frequency depends solely on the reference frequency provided to the part (assuming correctly programmed dividers).

The VCO gain is programmable, permitting the **ICS1574B** to be optimized for best performance at all operating frequencies.

The reference divider may be programmed for any modulus from 1 to 128 in steps of one.

The feedback divider may be programmed for any modulus from 37 through 392 in steps of one. Any even modulus from 392 through 784 can also be achieved by setting the "double" bit which doubles the feedback divider modulus. The feedback divider makes use of a dual-modulus prescaler technique that allows the programmable counters to operate at low speed without sacrificing resolution. This is an improvement over conventional fixed prescaler architectures that typically impose a factor-of-four (or larger) penalty in this respect.

Table 1 permits the derivation of "A" & "M" converter programming directly from desired modulus.

Digital Inputs

The programming of the **ICS1574B** is performed serially by using the DATCLK, DATA, and $\overline{\text{HOLD}}$ pins to load an internal shift register.

DATA is shifted into the register on the rising edge of DATCLK. The logic value on the $\overline{\text{HOLD}}$ pin is latched at the same time. When $\overline{\text{HOLD}}$ is low, the shift register may be loaded without disturbing the operation of the **ICS1574B**. When high, the shift register outputs are transferred to the control registers, and the new programming information becomes active. Ordinarily, a high level should be placed on the $\overline{\text{HOLD}}$ pin when the last data bit is presented. See Figure 3 for the programming sequence.

The PCLKEN input polarity may be programmed under register control via Bit 39.

ICS1574 Register Loading

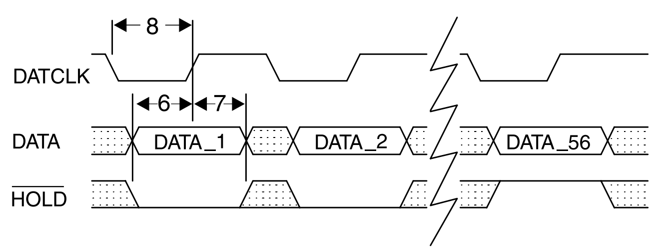


Figure 3

Output Description

The PCLK output is a high-current CMOS type drive whose frequency is controlled by a programmable divider that may be selected for a modulus of 3, 4, 5, 6, 8, 10, 12, 16 or 20. It may also be suppressed under register control via Bit 46.

Reference Oscillator and Crystal Selection

The **ICS1574B** has circuitry on-board to implement a Pierce oscillator with the addition of only one external component, a quartz crystal. Pierce oscillators operate the crystal in anti- (also called parallel-) resonant mode. See the AC Characteristics for the effective capacitive loading to specify when ordering crystals.

Series-resonant crystals may also be used with the **ICS1574B**. Be aware that the oscillation frequency will be slightly higher than the frequency that is stamped on the can (typically 0.025 – 0.05%).

As the entire operation of the phase-locked loop depends on having a stable reference frequency, we recommend that the crystal be mounted as closely as possible to the package. Avoid routing digital signals or the **ICS1574B** outputs underneath or near these traces. It is also desirable to ground the crystal can to the ground plane, if possible.

If an external reference frequency source is to be used with the **ICS1574B**, it is important that it be jitter-free. The rising and falling edges of that signal should be fast and free of noise for best results.

The loop phase can be locked to either the rising or falling edges of the XTAL1 input signals, and is controlled by Bit 56.

Power-On Initialization

The **ICS1574B** has an internal power-on reset circuit that performs the following functions:

1) Selects the modulus of the PCLK divider to be four (4).

2) Sets the multiplexer to pass the reference frequency to PCLK divider input.

These functions should allow initialization for most applications that cannot immediately provide for register programming upon system power-up.

Because the power-on reset circuit is on the VDD supply, and because that supply is filtered, care must be taken to allow the reset to de-assert before programming. A safe guideline is to allow 20 microseconds after the VDD supply reaches 4 volts.

Programming Notes

- VCO Frequency Range: Use the post-divider to keep the VCO frequency as high as possible within its operating range.

- Divider Range: For best results in normal situations keep the reference divider modulus as short as possible (for a frequency at the output of the reference divider in the few hundred kHz to several MHz range). If you need to go to a lower phase comparator reference frequency (usually required for increased frequency accuracy), that is acceptable, but jitter performance will suffer somewhat.

- VCO Gain Programming: Use the minimum gain which can reliably achieve the VCO frequency desired, as shown here:

VCO GAIN	MAX FREQUENCY
4	100 MHz
5	200 MHz
6	300 MHz
7	400 MHz

- Phase Detector Gain: For most applications and divider ranges, set P[1,0] = 10 and set P[2] = 1. Under some circumstances, setting the P[2] bit "on" can reduce jitter. During operation at exact multiples of the crystal frequency, P[2] bit = 0 may provide the best jitter performance.

Board Test Support

It is often desirable to statically control the levels of the output pins for circuit board test. The **ICS1574B** supports this through a register programmable mode, AUX-EN. When this mode is set, a register bit directly controls the logic level of the PCLK pin. This mode is activated when the S[0] and S[1] bits are both set to logic 1. See Register Mapping for details.

Power Supplies and Decoupling

The **ICS1574B** has two VSS pins to reduce the effects of package inductance. Both pins are connected to the same potential on the die (the ground bus). BOTH of these pins should connect to the ground plane of the PCB as close to the package as is possible.

The **ICS1574B** has a VDDO pin which is the supply of +5 volt power to the output driver. This pin should be connected to the power plane (or bus) using standard high-frequency decoupling practice. That is, capacitors should have low series inductance and be mounted close to the **ICS1574B**.

The VDD pin is the power supply pin for the PLL synthesizer circuitry and other lower current digital functions. We recommend that RC decoupling or zener regulation be provided for this pin (as shown in the recommended application circuitry). This will allow the PLL to "track" through power supply fluctuations without visible effects. See Figure 4 for typical external circuitry.

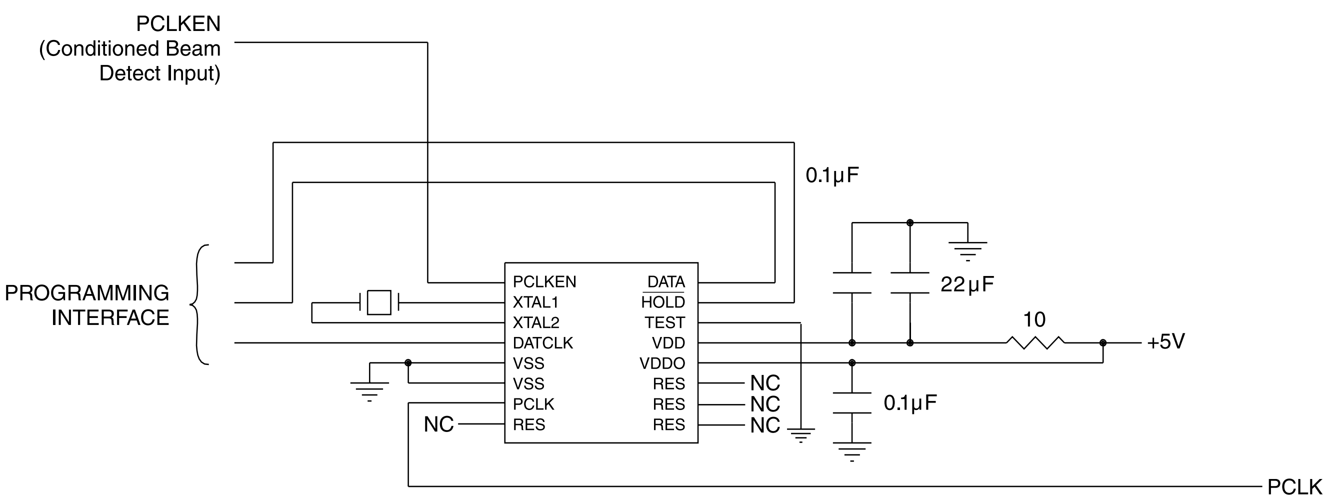


Figure 4

Register Mapping — ICS1574B

NOTE: It is not necessary to understand the function of these bits to use the ICS1574B. PC Software is available from ICS to automatically generate all register values based on requirements. Contact factory for details.

BIT(S)	BIT REF.	DESCRIPTION
1 – 4	PCLK[0]..PCLK[3]	Sets PCLK divider modulus according to this table. These bits are set to implement a divide-by-four on power-up.

PCLK[3]	PCLK[2]	PCLK[1]	PCLK[0]	MODULUS
0	0	0	0	3
0	0	0	1	4(a)
0	0	1	0	4(b)
0	0	1	1	5
0	1	0	0	6
0	1	0	1	8(a)
0	1	1	0	8(b)
0	1	1	1	10
1	X	0	0	12
1	X	0	1	16(a)
1	X	1	0	16(b)
1	X	1	1	20

(X = Don't Care)

BIT(S)	BIT REF.	DESCRIPTION
5, 6	Reserved	Must be set to 0.
7	Reserved	Must be set to 1.
8	SELXTAL	Normally set to 0. When set to logic 1, passes the reference frequency to the post-scaler instead of the PLL output (defaults to 1 on power-up).
9	Reserved	Must be set to 0.
10	Reserved	Must be set to 1.
11, 12	Reserved	Must be set to 0.
13 – 14	S[0]..S[1]	PLL post-scaler / test mode select bits.

S[1]	S[0]	DESCRIPTION
0	0	Post-scaler = 1. F(CLK) = F(PLL). The output of the PCLK divider drives the PCLK output.
0	1	Post-scaler = 2. F(CLK) = F(PLL)/2. The output of the PCLK divider drives the PCLK output.
1	0	Post-scaler = 4. F(CLK) = F(PLL)/4. The output of the PCLK divider drives the PCLK output.
1	1	AUX-EN TEST MODE. The AUX_PCLK bit drives the PCLK output.

BIT(S)	BIT REF.	DESCRIPTION
15	Reserved	Must be set to 0.
16	AUX_PCLK	Must be set to 0 except when in the AUX-EN test mode. When in the AUX-EN test mode, this bit controls the PCLK output.
17 – 24	Reserved	Must be set to 0.
25 – 27	V[0]..V[2]	Sets the gain of VCO

V[2]	V[1]	V[0]	VCO GAIN (MHz/Volt)
1	0	0	30
1	0	1	45
1	1	0	60
1	1	1	80

BIT(S)	BIT REF.	DESCRIPTION
28	Reserved	Must be set to 1.
29 – 30	P[0]..P[1]	Sets the gain of the phase detector according to this table:

P[1]	P[0]	GAIN (μA/radian)
0	0	0.05
0	1	0.15
1	0	0.5
1	1	1.5

BIT(S)	BIT REF.	DESCRIPTION
31	Reserved	Must be set to 0.
32	P[2] See text.	Phase detector tuning bit. Should normally be set to one.
33 – 38	M[0]..M[5]	M counter control bits. Modulus = value + 1.
39	PCLKEN_POL	When = 0, PCLK output enabled when PCLKEN input is low. When = 1, PCLK output enabled when PCLKEN input is high.
40	DBLFREQ	Doubles modulus of dual-modulus prescaler (from 6/7 to 12/14).
41 – 44	A[0]..A[3]	Controls A counter. When set to zero, modulus = 7. Otherwise, modulus = 7 for "value" underflows of the prescaler, and modulus = 6 thereafter until M counter underflows.

BIT(S)	BIT REF.	DESCRIPTION
45	Reserved	Must be set to 1.
46	PCLK_EN	Must be set to 0. Disables the PCLK divider when set to 1 regardless of PCLKEN input state.
47, 48	Reserved	Must be set to 0.
49 – 55	R[0]..R[6]	Reference divider modulus control bits. Modulus = value +1.
56	REF_POL	PLL locks to rising edge of XTAL1 input when REFPOL = 1, falling edge of XTAL1 when REFPOL = 0.

Table 1 — "A" & "M" Divider Programming
Feedback Divider Modulus Table

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
000000								7
000001	13							14
000010	19	20						21
000011	25	26	27					28
000100	31	32	33	34				35
000101	37	38	39	40	41			42
000110	43	44	45	46	47	48		49
000111	49	50	51	52	53	54	55	56
001000	55	56	57	58	59	60	61	63
001001	61	62	63	64	65	66	67	70
001010	67	68	69	70	71	72	73	77
001011	73	74	75	76	77	78	79	84
001100	79	80	81	82	83	84	85	91
001101	85	86	87	88	89	90	91	98
001110	91	92	93	94	95	96	97	105
001111	97	98	99	100	101	102	103	112
010000	103	104	105	106	107	108	109	119
010001	109	110	111	112	113	114	115	126
010010	115	116	117	118	119	120	121	133
010011	121	122	123	124	125	126	127	140
010100	127	128	129	130	131	132	133	147
010101	133	134	135	136	137	138	139	154
010110	139	140	141	142	143	144	145	161
010111	145	146	147	148	149	150	151	168
011000	151	152	153	154	155	156	157	175
011001	157	158	159	160	161	162	163	182
011010	163	164	165	166	167	168	169	189
011011	169	170	171	172	173	174	175	196
011100	175	176	177	178	179	180	181	203
011101	181	182	183	184	185	186	187	210
011110	187	188	189	190	191	192	193	217
011111	193	194	195	196	197	198	199	224

A[2]..A[0]-	001	010	011	100	101	110	111	000
M[5]..M[0]								
100000	199	200	201	202	203	204	205	231
100001	205	206	207	208	209	210	211	238
100010	211	212	213	214	215	216	217	245
100011	217	218	219	220	221	222	223	252
100100	223	224	225	226	227	228	229	259
100101	229	230	231	232	233	234	235	266
100110	235	236	237	238	239	240	241	273
100111	241	242	243	244	245	246	247	280
101000	247	248	249	250	251	252	253	287
101001	253	254	255	256	257	258	259	294
101010	259	260	261	262	263	264	265	301
101011	265	266	267	268	269	270	271	308
101100	271	272	273	274	275	276	277	315
101101	277	278	279	280	281	282	283	322
101110	283	284	285	286	287	288	289	329
101111	289	290	291	292	293	294	295	336
110000	295	296	297	298	299	300	301	343
110001	301	302	303	304	305	306	307	350
110010	307	308	309	310	311	312	313	357
110011	313	314	315	316	317	318	319	364
110100	319	320	321	322	323	324	325	371
110101	325	326	327	328	329	330	331	378
110110	331	332	333	334	335	336	337	385
110111	337	338	339	340	341	342	343	392
111000	343	344	345	346	347	348	349	399
111001	349	350	351	352	353	354	355	406
111010	355	356	357	358	359	360	361	413
111011	361	362	363	364	365	366	367	420
111100	367	368	369	370	371	372	373	427
111101	373	374	375	376	377	378	379	434
111110	379	380	381	382	383	384	385	441
111111	385	386	387	388	389	390	391	448

Notes: To use this table, find the desired modulus in the table. Follow the column up to find the A divider programming values. Follow the row to the left to find the M divider programming. Some feedback divisors can be achieved with two or three combinations of divider settings. Any are acceptable for use.

The formula for the effective feedback modulus is: $N = [(M+1) \bullet 6] + A$
except when A=0, then: $N = (M+1) \bullet 7$
Under all circumstances: $A \leq M$

Absolute Maximum Ratings

VDD, VDDO (measured to Vss) 7.0V
Digital Inputs . . . . V_{SS} −0.5V to V_{DD} +0.5V
Digital Outputs . . . . V_{SS} −0.5V to V_{DDO} +0.5V
Ambient Operating Temperature . . . . −55°C to +125°C
Storage Temperature . . . . −65°C to +150°C
Junction Temperature . . . . 175°C
Soldering Temperature . . . . 260°C

Recommended Operating Conditions

VDD, VDDO (measured to Vss) . . . . 4.75 to 5.25 V
Operating Temperature (Ambient) . . . . . . 0 to +70°C

DC Electrical Characteristics

TTL-Compatible Inputs (DATCLK, DATA, $\overline{\text{HOLD}}$, PCLKEN)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{IH}		2.0	V_{DD} +0.5	V
Input Low Voltage	V_{IL}		V_{SS} –0.5	0.8	V
Input High Current	I_{IH}	V_{IH} = VDD	—	10	µA
Input Low Current	I_{IL}	V_{IL} = 0.0	—	200	µA
Input Capacitance	C_{IN}		—	8	pF
Hysterisis (DATCLK input)	V_{HYS}	VDD = 5V	.20	.60	V

XTAL1 Input (External Reference Frequency)

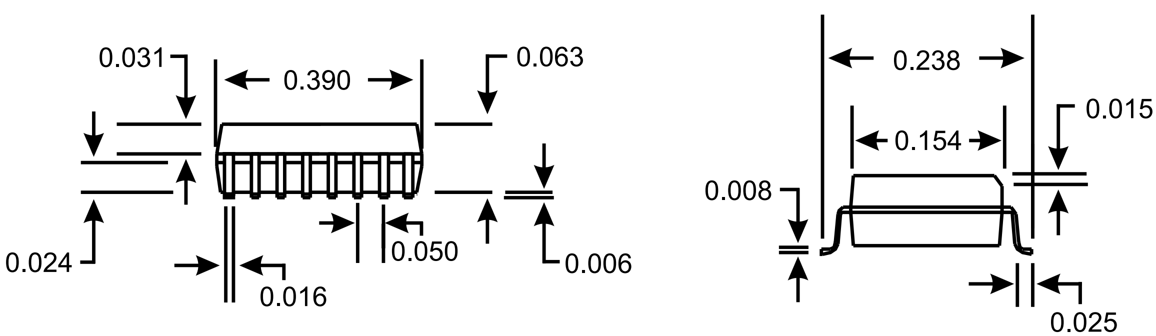
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input High Voltage	V_{XH}		3.75	V_{DD} +0.5	V
Input Low Voltage	V_{XL}		V_{SS} –0.5	1.25	V

PCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output High Voltage (I_{OH} = 4.0mA)			2.4	—	V
Output Low Voltage (I_{OL} = 8.0mA)			—	0.4	V

AC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VCO Frequency	FVCO	40		400	MHz
Crystal Frequency	FXTAL	5		20	MHz
Crystal Oscillator Loading Capacitance	CPAR		20		pF
XTAL1 High Time (when driven externally)	TXHI	8			ns
XTAL1 Low Time (when driven externally)	TXLO	8			ns
PLL Acquire Time (to within 1%)	TLOCK		500		µs
VDD Supply Current	IDD		15	t.b.d.	mA
VDDO Supply Current	IDDO		20	t.b.d.	mA
Digital Inputs					
DATA/HOLD ~Setup Time		10			ns
DATA/HOLD ~Hold Time		10			ns
DATCLK Pulse Width (Thi or Tlo)		20			ns
Digital Output					
PCLK output rate	FPCLOCK			130	MHz



16-Pin Skinny SOIC Package

Ordering Information

ICS1574BM / ICS1574BEB

Example:

ICS 1574B M LF

LF — Pb (lead) free package

M — **Package Type**
M = SOIC • EB = Evaluation Board

1574B — **Device Type**

ICS — **Prefix**
ICS, AV = Standard Device • GSP = Genlock Device

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