KDC5612EVAL Schematics

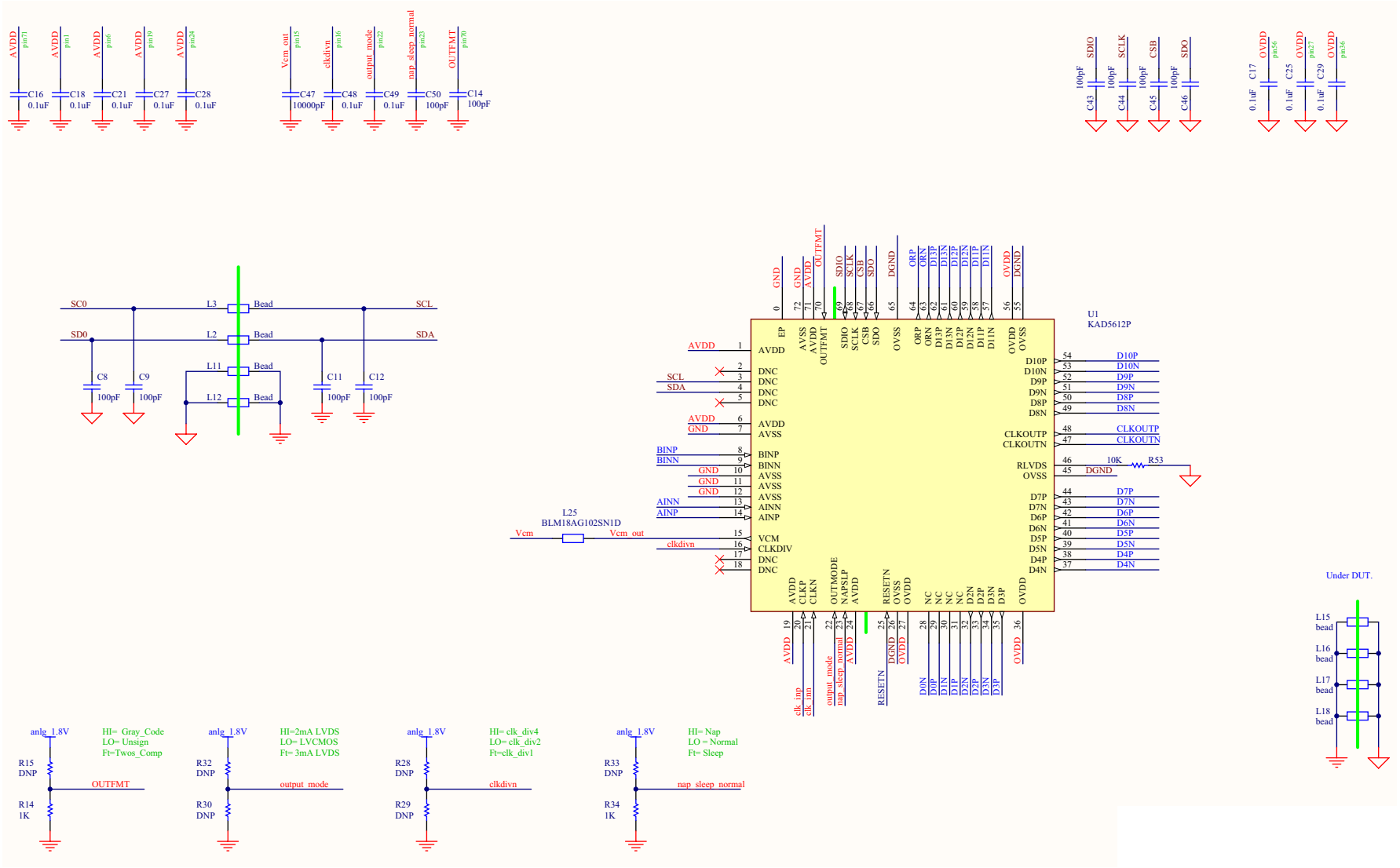

FIGURE 1. ADC, MODE PINS AND POWER SUPPLY BYPASS

KDC5612EVAL Schematics (Continued)

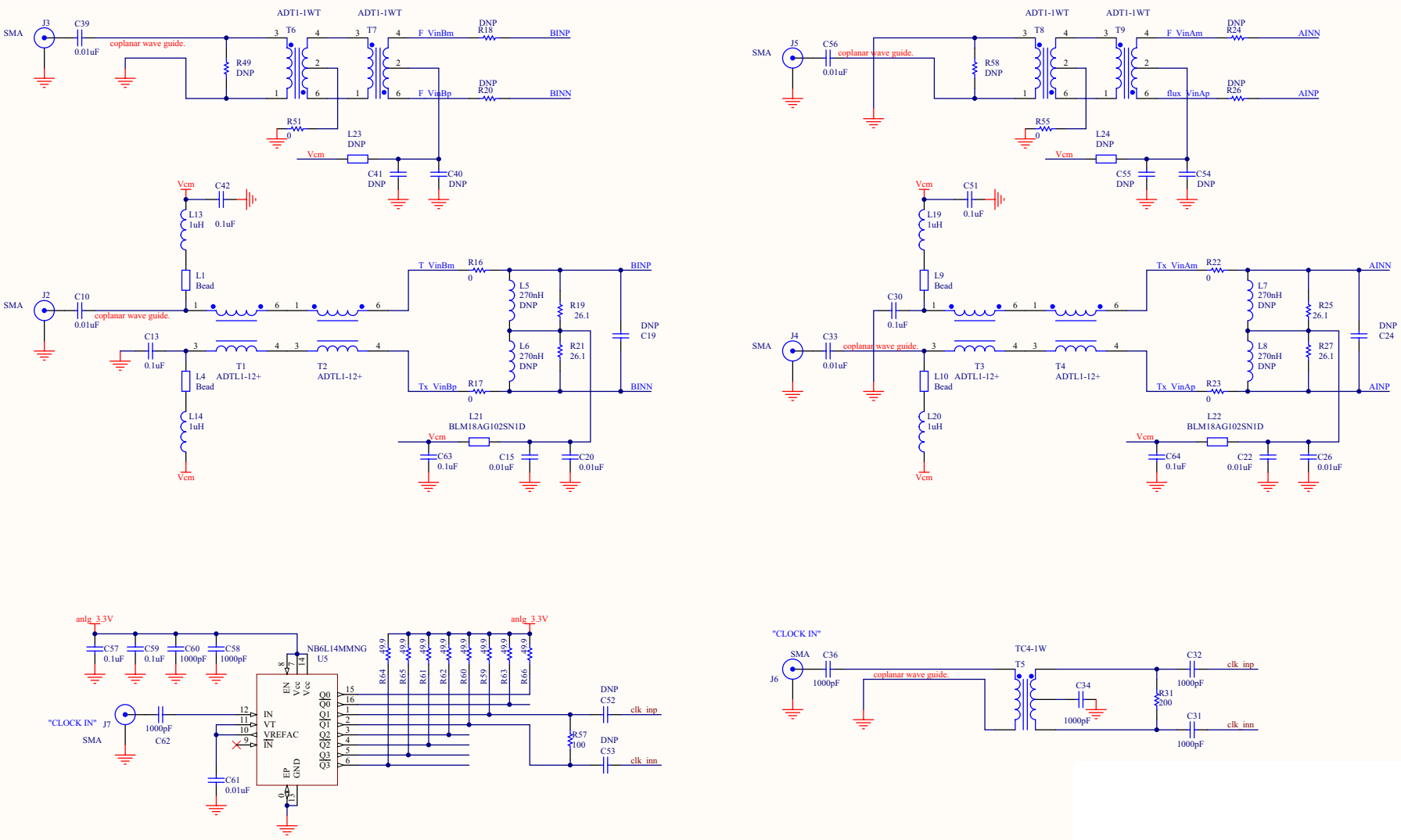

FIGURE 2. CLOCK AND ANALOG INPUTS

KDC5612EVAL Schematics (Continued)

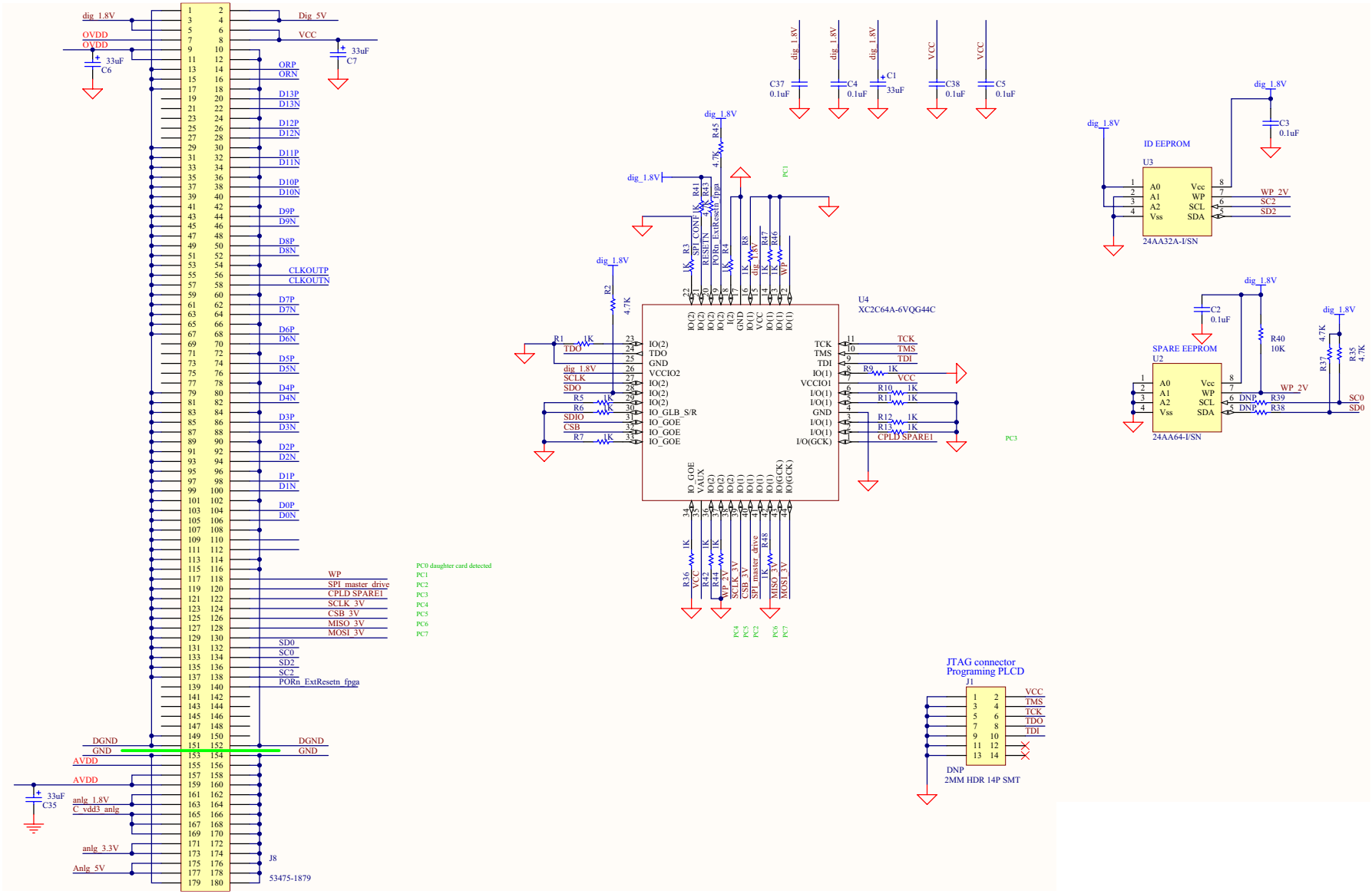

FIGURE 3. INPUT/OUTPUT MEZZANINE CONNECTOR

KDC5612EVAL Layers

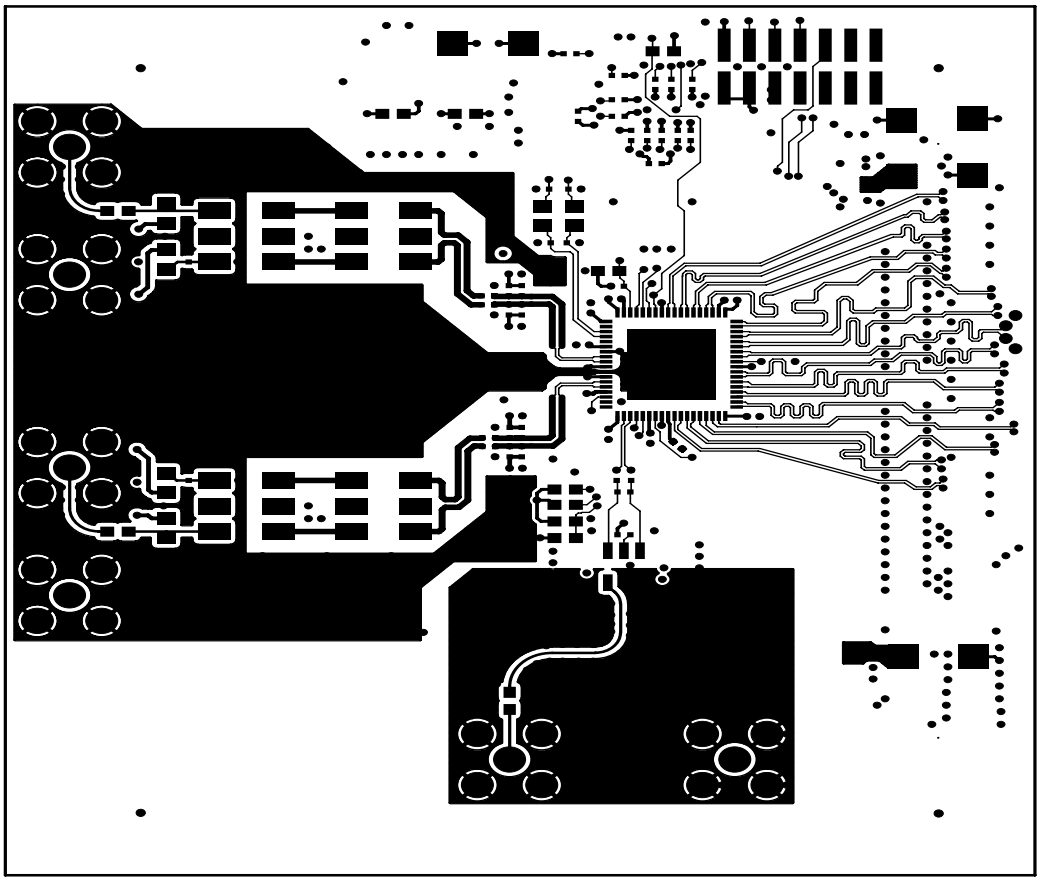

FIGURE 4. PRIMARY SIDE

KDC5612EVAL Layers (Continued)

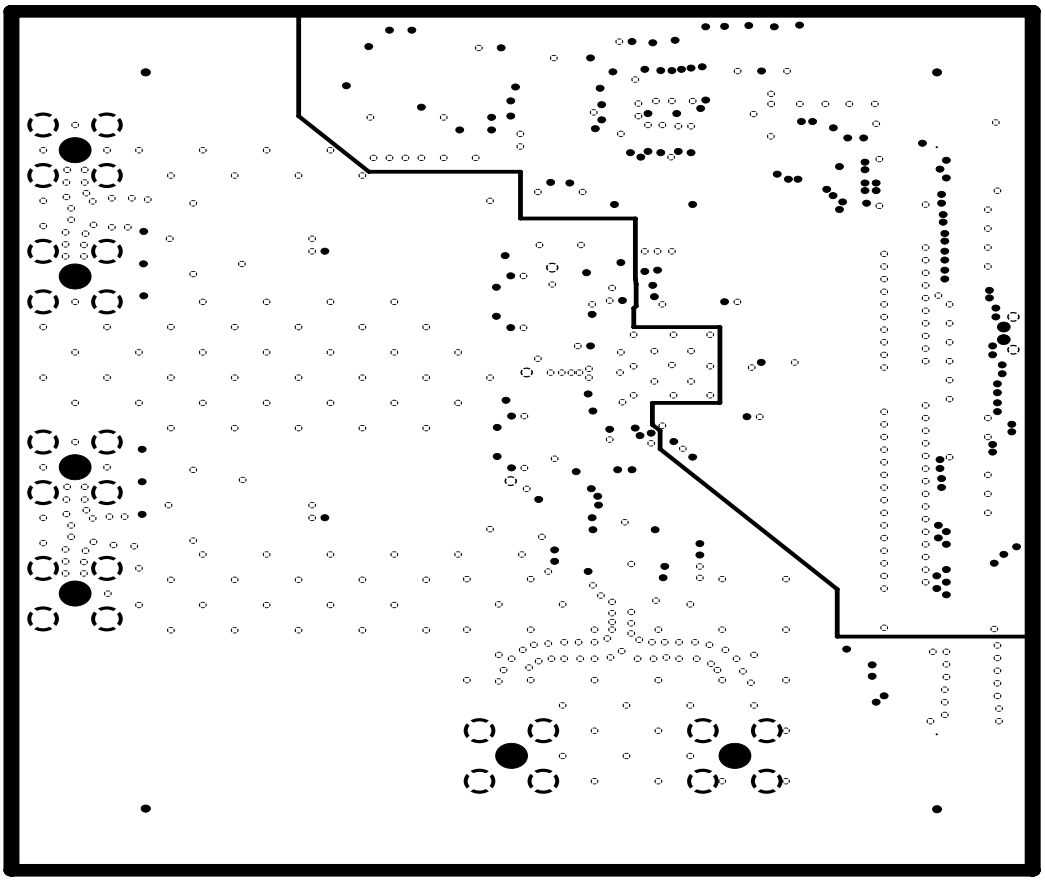

FIGURE 5. GND PLANE 1

KDC5612EVAL Layers (Continued)

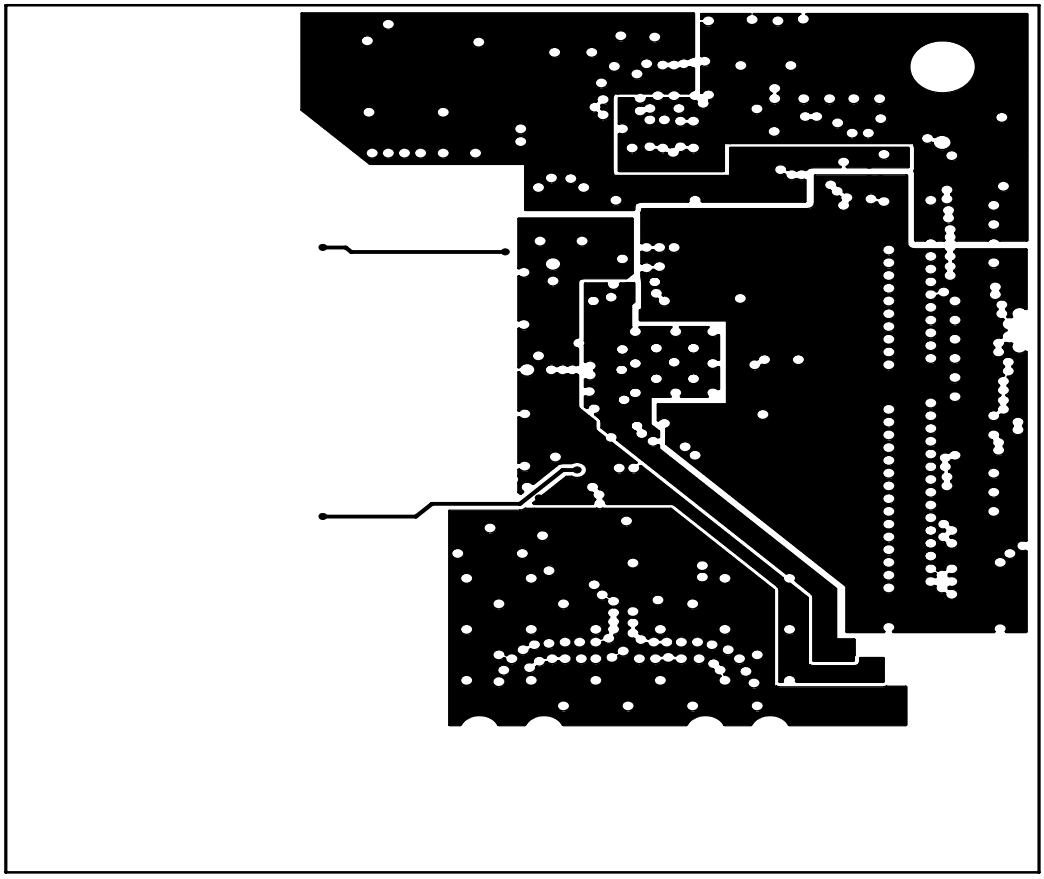

FIGURE 6. PWR PLANE

KDC5612EVAL Layers (Continued)

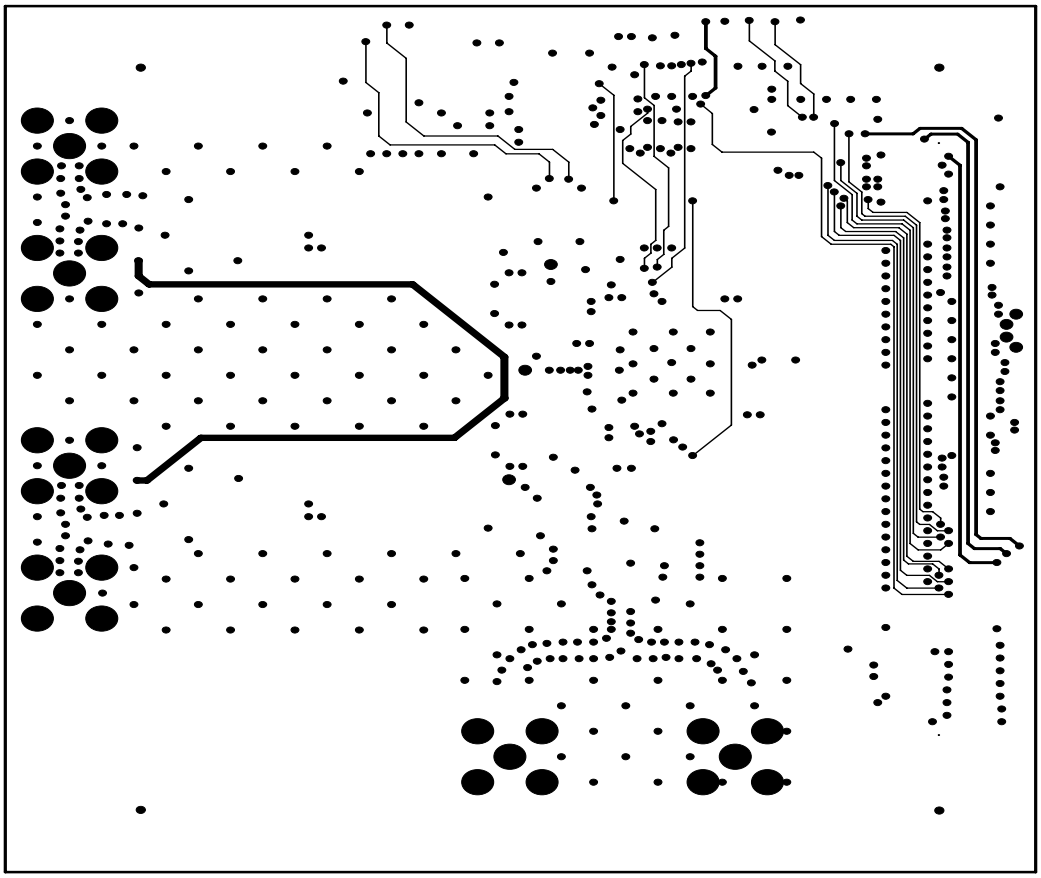

FIGURE 7. INTERNAL SIGNAL

KDC5612EVAL Layers (Continued)

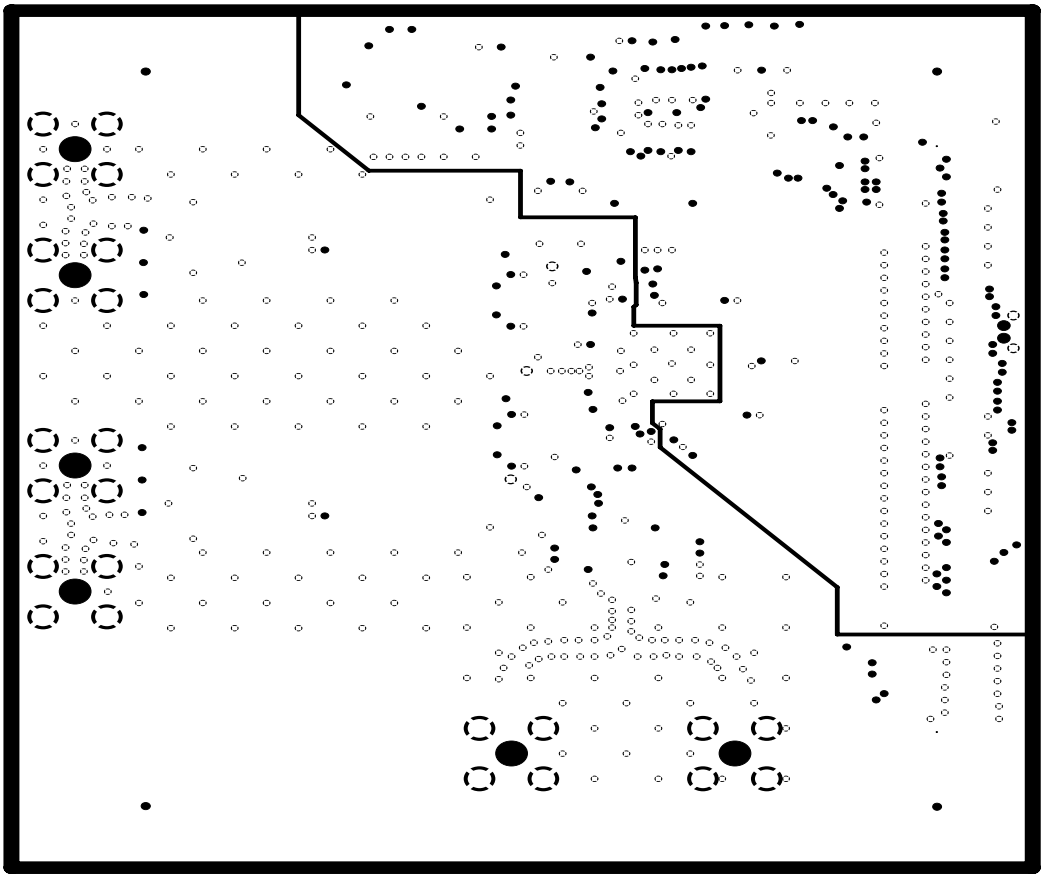

FIGURE 8. GND PLANE 2

KDC5612EVAL Layers (Continued)

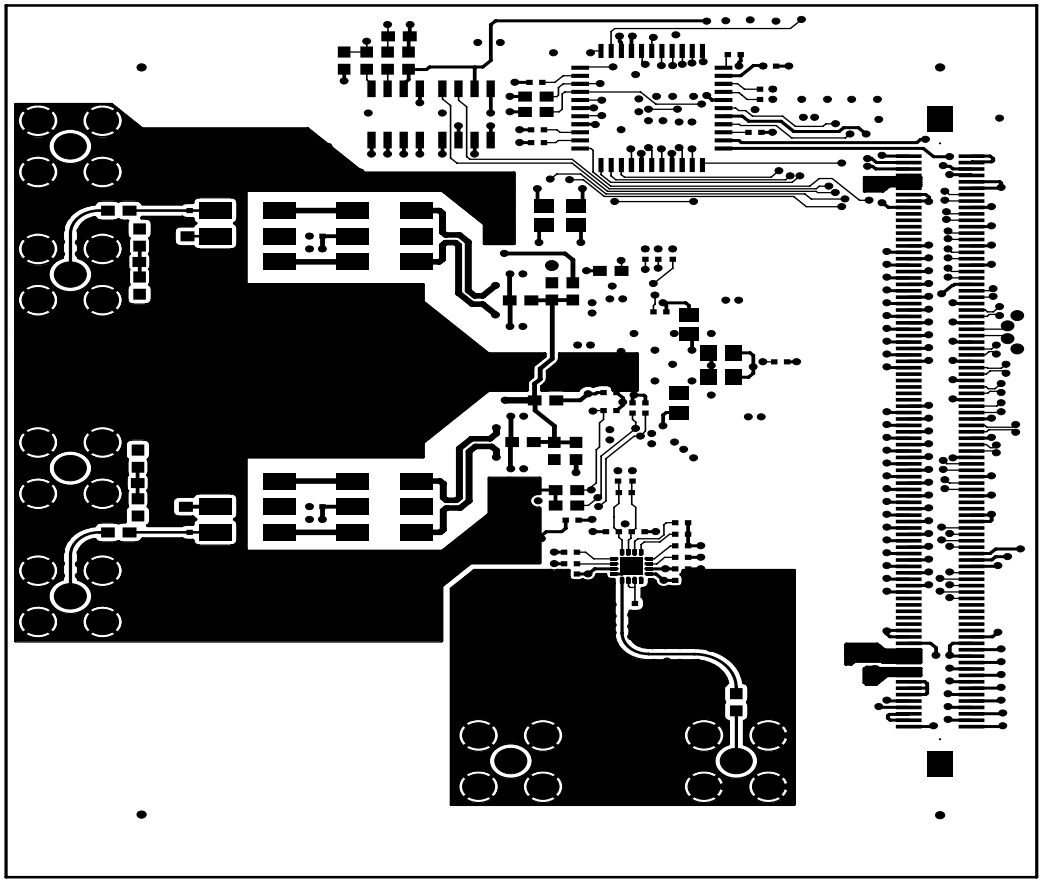

FIGURE 9. SECONDARY SIDE

KDC5612EVAL Layers (Continued)

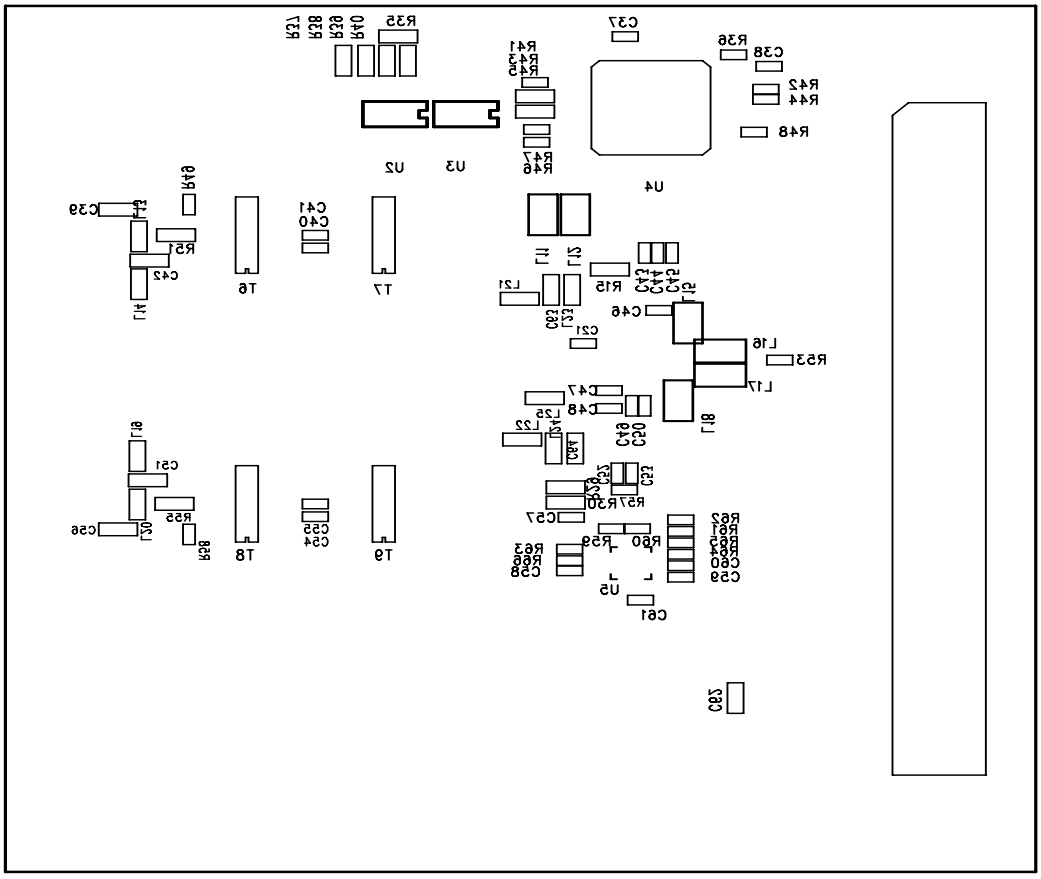

FIGURE 10. SECONDARY SIDE SILKSCREEN

KDC5612EVAL Layers (Continued)

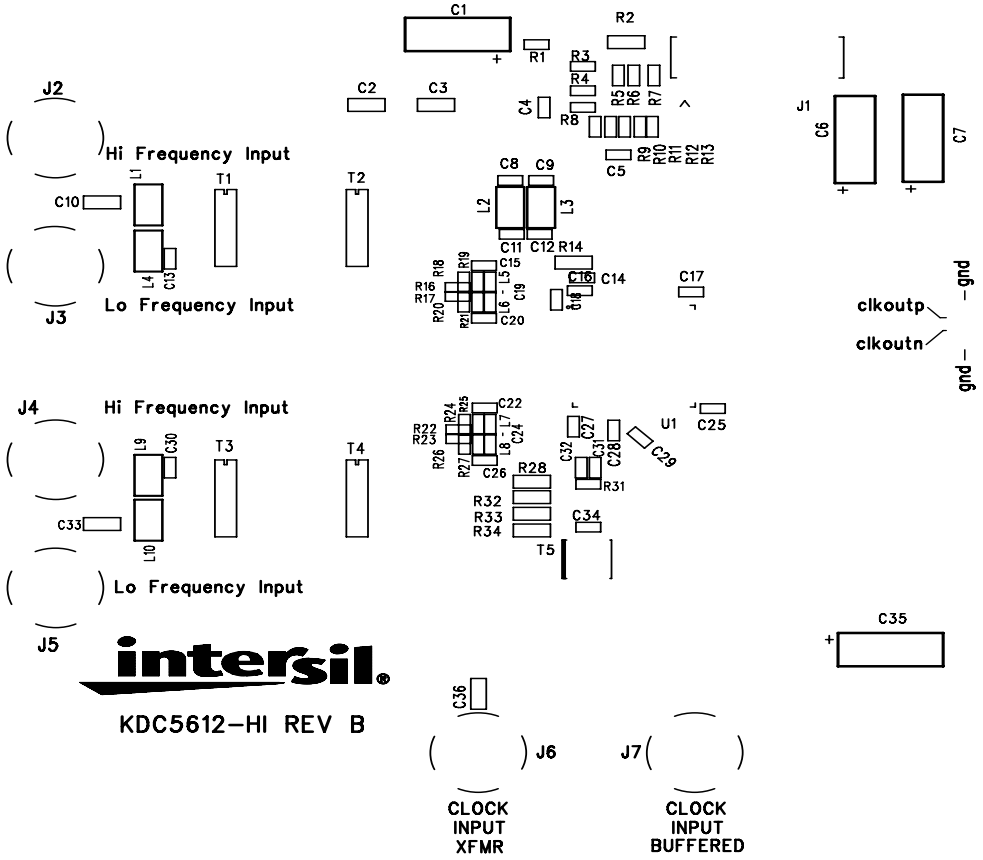

FIGURE 11. LAYER - PRIMARY SIDE SILKSCREEEN