

Supplemental Information

This notice describes the differences between the updated version and its previous version of the IDT82V3012 Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Changed Items
November 18, 2004	-	Item 6 - 5
February 02, 2004	-	Item 4
October 22, 2003	F0312-03	Item 3-1

Changed Items

November 18, 2004

Item 6: Added green package option (page 1, 31)

Item 5: Corrected an error description on the State Control Circuit (page 10, 3rd paragraph of the left column)

Old: “When changing the operating mode, the TIE control block is enabled/disabled automatically by the state control circuit as shown in [Figure - 3](#), except for the changes from Normal (S1) to Auto-Holdover (S2), and from Auto-Holdover (S2), Holdover (S3) and Short Time Holdover (S4) to Normal (S1). During these four changes, the TIE control block can be enabled or disabled, depending on the logic level on the TIE_en pin.”

New: “When the operating mode is changed from one to another, the TIE control block is automatically disabled as shown in [Figure - 3](#), except the changes from Short Time Holdover (S4), Holdover (S3) or Auto-Holdover (S2) to Normal (S1). In the case of changing from S4, S3 or S2 to S1, the TIE control block is enabled or disabled by the TIE_en pin.”

February 02, 2004

Item 4: In section 2.10, add the content about lock and TIE application. (page 14, 15)

October 22, 2003

Item 3: The accuracy of holdover frequency has been updated from 0.00625 ppm to 0.025 ppm. (page 1, 10, 11, 19)

Item 2: C19o (19.44 MHz) Intrinsic Jitter Filtered Table has been updated as follows: (page 20)

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see “Notes” on page 24)
Intrinsic jitter (500 Hz to 1.3 MHz filter)		0.4	0.5	nspp	1-15, 22-25, 37
Intrinsic jitter (65 kHz to 1.3 MHz filter)		0.2	0.3	nspp	1-15, 22-25, 37

Item 1: Input/Output Timing Table has been updated as follows: (Page 25)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	51			ns	8 kHz, 1.544 MHz or 2.048 MHz reference input
		5			ns	19.44 MHz reference input
t_{R8D}	8 kHz reference input to F8o delay		8		ns	
t_{R15D}	1.544 MHz reference input to F8o delay		332		ns	
t_{R2D}	2.048 MHz reference input to F8o delay		253		ns	
t_{R19D}	19.44 MHz reference input to F8o delay		8		ns	
t_{F0D}	F8o to $\overline{F0o}$ delay	118	121	124	ns	
t_{F19S}	F19o setup to C19o falling	20		35	ns	
t_{F19H}	F19o hold to C19o falling	20		35	ns	
t_{C15D}	F8o to C1.5o delay	-3	0	+3	ns	
t_{C3D}	F8o to $\overline{C3o}$ delay	-3	1.6	+3	ns	
t_{C6D}	F8o to C6o delay	-3	1.6	+3	ns	
t_{C2D}	F8o to C2o	-2	0	+2	ns	
t_{C4D}	F8o to $\overline{C4o}$	-2	0	+2	ns	
t_{C8D}	F8o to C8o delay	-2	0	+2	ns	
t_{C16D}	F8o to $\overline{C16o}$ delay	-2	0	+2	ns	
t_{C19D}	F8o to C19o delay	-8	0	+8	ns	
t_{C32D}	F8o to $\overline{C32o}$ delay	-2	2	+2	ns	
t_{TSPD}	F8o to TSP delay	-3	0	+3	ns	
t_{RSPD}	F8o to RSP delay	-3	0	+3	ns	
t_{C15W}	C1.5o pulse width high or low		323		ns	
t_{C3W}	$\overline{C3o}$ pulse width high or low		161		ns	
t_{C6W}	C6o pulse width high or low		82		ns	
t_{C2W}	C2o pulse width high or low		244		ns	
t_{C4W}	$\overline{C4o}$ pulse width high or low		122		ns	
t_{C8W}	C8o pulse width high or low		61		ns	
t_{C16W}	$\overline{C16o}$ pulse width high or low		30.5		ns	
t_{C32WH}	$\overline{C32o}$ pulse width high		14.4		ns	
t_{TSPW}	TSP pulse width high		486		ns	
t_{RSPW}	RSP pulse width high		490		ns	
t_{F0WL}	$\overline{F0o}$ pulse width low		243		ns	
t_{F8WH}	F8o pulse width high		123.6		ns	
t_{F16WL}	$\overline{F16o}$ pulse width low		60.9		ns	
t_{ORF}	Output clock and frame pulse rise or fall time		3		ns	

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{F16D}	F8o to $\overline{F16o}$ delay	27.1	30.1	33.1	ns	
t_{F19D}	F8o to F19o delay	17	25	33	ns	
t_{F32D}	F8o to $\overline{F32o}$ delay	12	15.8	19	ns	
t_{F32WL}	$\overline{F32o}$ pulse width low		30.6		ns	

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