

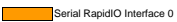

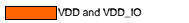
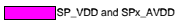

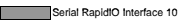


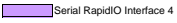
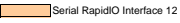
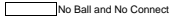
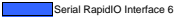
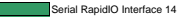


Note: This is the ballmap when looking through the top of the package. This ballmap represents the PCB footprint for the Tsi568A.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
A	NO_BALL	VSS	VSS	VSS	VSS	VSS	SP14_TD_P	VSS	SP14_TC_N	VSS	SP14_TB_P	VSS	SP14_TA_N	VSS	SP6_TD_P	VSS	SP6_TC_N	VSS	SP6_TB_P	VSS	SP6_TA_N	VSS	VSS	VSS	VSS	VSS	A	
B	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP14_TD_N	VSS	SP14_TC_P	SP_VDD	SP14_TB_N	VSS	SP14_TA_P	SP_VDD	SP6_TD_N	VSS	SP6_TC_P	SP_VDD	SP6_TB_N	VSS	SP6_TA_P	SP_VDD	VSS	S_CLK1_P	S_CLK1_N	VSS	B	
C	SP0_TA_N	SP0_TA_P	SP_VDD	SP0_RA_P	SP0_RA_N	SP_VDD	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	SP_VDD	VSS	SP_VDD	C	
D	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP14_RD_N	VSS	SP14_RC_P	SP14_RREF	SP14_RB_N	VSS	SP14_RA_P	VSS	SP6_RD_N	VSS	SP6_RC_P	SP6_RREF	SP6_RB_N	VSS	SP6_RA_P	VSS	VSS	S_CLK2_P	S_CLK2_N	VSS	D	
E	SP0_TB_P	SP0_TB_N	SP_VDD	SP0_RB_P	SP0_RB_N	SP_VDD	SP14_RD_P	SP14_VTT	SP14_RC_N	SP14_AVDD	SP14_RB_P	SP_VDD	SP14_RA_N	VSS	SP6_RD_P	SP6_VTT	SP6_RC_N	SP6_AVDD	SP6_RB_P	SP_VDD	SP6_RA_N	VSS	VSS	VSS	VSS	VSS	E	
F	VSS	SP_VDD	VSS	SP0_RREF	SP0_AVDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	F	
G	SP0_TC_N	SP0_TC_P	SP_VDD	SP0_RC_P	SP0_RC_N	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP12_RD_P	SP12_RD_N	SP_VDD	SP12_TD_N	SP12_TD_P	G
H	VSS	VSS	VSS	VSS	SP0_VTT	VSS	SP_VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP12_VTT	VSS	VSS	VSS	H	
J	SP0_TD_P	SP0_TD_N	SP_VDD	SP0_RD_N	SP0_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	SP12_RC_N	SP12_RC_P	SP_VDD	SP12_TC_P	SP12_TC_N	J
K	VSS	SP_VDD	VSS	VSS	VSS	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	VSS	SP12_AVDD	SP12_RREF	VSS	SP_VDD	VSS	K
L	SP8_TA_N	SP8_TA_P	SP_VDD	SP8_RA_P	SP8_RA_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	SP12_RB_P	SP12_RB_N	SP_VDD	SP12_TB_N	SP12_TB_P	L
M	VSS	VSS	VSS	VSS	SP_VDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	VSS	VSS	VSS	M
N	SP8_TB_P	SP8_TB_N	SP_VDD	SP8_RB_P	SP8_RB_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	SP12_RA_N	SP12_RA_P	SP_VDD	SP12_TA_P	SP12_TA_N	N
P	VSS	SP_VDD	VSS	SP8_RREF	SP8_AVDD	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	VSS	VSS	VSS	SP_VDD	VSS	P	
R	SP8_TC_N	SP8_TC_P	SP_VDD	SP8_RC_P	SP8_RC_N	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	SP4_RD_P	SP4_RD_N	SP_VDD	SP4_TD_N	SP4_TD_P	R
T	VSS	VSS	VSS	VSS	SP8_VTT	VSS	SP_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	VSS	SP4_VTT	VSS	VSS	VSS	VSS	T
U	SP8_TD_P	SP8_TD_N	SP_VDD	SP8_RD_N	SP8_RD_P	SP_VDD	VSS	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	SP4_RC_N	SP4_RC_P	SP_VDD	SP4_TC_P	SP4_TC_N	U
V	VSS	VDD_IO	VSS_IO	VSS	VSS_IO	VDD_IO	VSS	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS	SP_VDD	VSS	SP4_AVDD	SP4_RREF	VSS	SP_VDD	VSS	V
W	VSS_IO	SP4_PWRD_N	SP4_PWRD_P	VDD_IO	SP6_PWRD_N	SP7_PWRD_N	SP14_PWRD_N	VSS_IO	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	SP_VDD	SP4_RB_P	SP4_RB_N	SP_VDD	SP4_TB_N	SP4_TB_P	W
Y	SP8_PWRD_N	VDD_IO	SP9_PWRD_N	SP10_PWRD_N	VSS_IO	SP11_PWRD_N	VDD_IO	SP15_PWRD_N	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	NC	NC	VSS	SP_VDD	VSS	VSS	VSS	VSS	Y	
AA	VSS_IO	SP12_PWRD_N	SP13_PWRD_N	VDD_IO	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP4_RA_N	SP4_RA_P	SP_VDD	SP4_TA_P	SP4_TA_N	AA
AB	SP4_MODESEL	VDD_IO	SP4_MODESEL	SP8_MODESEL	VSS_IO	SP2_RA_N	SP_VDD	SP2_RB_P	SP2_AVDD	SP2_RC_N	SP2_VTT	SP2_RD_P	VSS	SP10_RA_N	SP_VDD	SP10_RB_P	SP10_AVDD	SP10_RC_N	SP10_VTT	SP10_RD_P	VSS	VSS	VSS	VSS	SP_VDD	VSS	AB	
AC	VSS_IO	INT_B	SP10_MODESEL	VDD_IO	VSS	SP2_RA_P	VSS	SP2_RB_N	SP2_RREF	SP2_RC_P	VSS	SP2_RD_N	VSS	SP10_RA_P	VSS	SP10_RB_N	SP10_RREF	SP10_RC_P	VSS	SP10_RD_N	VSS	SP_IO_SP_EED[0]	SP_IO_SP_EED[1]	DC_DISABLE	VDD_IO	TMS	AC	
AD	NC	VDD_IO	SW_RST_B	NC	VSS_IO	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	VSS	SP_VDD	SP0_MOD_ESEL	SP2_MODESEL	VSS_IO	TDO	TDI	AD
AE	VSS_IO	NC	NC	VDD_IO	SP_VDD	SP2_TA_P	VSS	SP2_TB_N	SP_VDD	SP2_TC_P	VSS	SP2_TD_N	SP_VDD	SP10_TA_P	VSS	SP10_TB_N	SP_VDD	SP10_TC_P	VSS	SP10_TD_N	VSS	SP0_PWRD_N	SP2_PWRD_N	INT_SP	VDD_IO	TRST_B	AE	
AF	P_CLK	HARD_RST_B	SP12_MODESEL	SP14_MODESEL	VSS	SP2_TA_N	VSS	SP2_TB_P	VSS	SP2_TC_N	VSS	SP2_TD_P	VSS	SP10_TA_N	VSS	SP10_TB_P	VSS	SP10_TC_N	VSS	SP10_TD_P	VSS	SP10_PWRD_N	SP3_PWRD_N	VSS_IO	INT_SCLK	TCK	AF	

**Legend**

 VSS and VSS_IO	 JTAG	 Serial RapidIO Interface 0	 Serial RapidIO Interface 8
 VDD and VDD_IO	 SP_VDD and SPX_AVDD	 Serial RapidIO Interface 2	 Serial RapidIO Interface 10
 Miscellaneous	 S_CLK_x	 Serial RapidIO Interface 4	 Serial RapidIO Interface 12
 No Ball and No Connect		 Serial RapidIO Interface 6	 Serial RapidIO Interface 14

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**Revision History**

August 2009, 80B801A\_PN002\_02 -- No technical changes. Formatting was changed to reflect IDT.