RZ FAMILY MICROPROCESSORS

64-Bit & 32-Bit Arm-based high-end MPUs
THE NEXT-GENERATION PROCESSOR TO MEET THE NEEDS OF THE SMART SOCIETY HAS ARRIVED.

CONTENTS

RZ/V SERIES .......................... 04
RZ/G SERIES .......................... 08
RZ/A SERIES .......................... 16
RZ/T SERIES .......................... 22
RZ/N SERIES .......................... 30
PACKAGE LINEUP ......................... 35
The utilization of intelligent technology is advancing in all aspects of our lives, including electric household appliances, industrial equipment, building management, power grids, and transportation. The cloud-connected “smart society” is coming ever closer to realization. Microcontrollers are now expected to provide powerful capabilities not available previously, such as high-performance and energy-efficient control combined with interoperation with IT networks, support for human-machine interfaces, and more. To meet the demands of this new age, Renesas has drawn on its unmatched expertise in microcontrollers to create the RZ family of embedded processors. The lineup of these “next-generation processors that are as easy to use as conventional microcontrollers” to meet different customer requirements.

The Zenith of the Renesas micro

As embedded processors to help build the next generation of advanced products, the RZ family offers features not available elsewhere and brings new value to customer applications.

**RZ/V Series**
- 64-bit Cortex®-A CPU, up to 1GHz
- Low-power Embedded AI for Vision-Al Application

**RZ/G Series**
- 32/64-bit Cortex®-A CPU, up to 1.5Hz
- 3D Graphics for HMI Application

**RZ/A Series**
- 32-bit Cortex®-A CPU, up to 528MHz
- 10MB Embedded RAM for HMI Application

**RZ/T Series**
- 32-bit Cortex®-R CPU, up to 600MHz
- Real-time Control
- Multi-protocol Encoder I/F for AC Servo, Actuator, Inverter

**RZ/N Series**
- 32-bit Cortex®-A/M CPU, up to 500MHz
- Multi-protocol Industrial Network for PLC, Remote IO, Gateway
RZ/V Series

RZ/V Series Roadmap

- RZ/V2M
  - Cortex®-A53 x2 (1GHz)
  - DRP-AI, ISP
- RZ/V-next (TBD)

RZ/V Series Features

- Dedicated AI hardware "DRP-AI" achieves high-speed AI inference and low power consumption
- 4K (2160p30) video codec and high-performance image signal processor (ISP)
- Adopts Civil Infrastructure Platform (CIP) Linux kernel that can be supported for more than 10 years

* DRP: Dynamically Reconfigurable Processor

RZ/V Series Application

- IP Camera
- Surveillance camera
- Retail
- Logistics
- Image inspection

Founded in CY2016
AI Development Flow

- Open frameworks can be used for learning
- Converts from industry standard ONNX Format to executable with DRP-AI Translator

Training On PC with Deep Learning Frameworks

Dataset for Training ➔ Training

Dataset for Testing ➔ Evaluation

Trained Model ➔ ONNX

Convert to ONNX format ➔ DRP-AI Translator

Object code for DRP-AI ➔ Deploy

Camera ➔ Target Board ➔ “Cat”

Use Case

Standalone system

Add-on the AI inference on your system

Main System

Serial interface

Capturing image

Result of AI or videos

RZ/V2M

Output AI result

HDMI

Capturing image

Result of AI or videos

RZ/V2M

Output AI result

HDMI

Capturing image

Result of AI or videos

RZ/V2M

Output AI result

HDMI
RZ/V2M Group

CPU
- 2× Cortex-A53 (up to 1.0GHz)
- Vision and AI
- AI Accelerator; DRP-AI at 1.0 TOPS/W class
- Camera Interface; 2× MIPI CSI-2
- Face and Human Detection Engine

Video and Graphics
- H.265/H.264 Multi Codec
- JPEG Codec Engine
- 2D Graphics Engine
- Display Interface
- MIPI-DSI (4-lane)
- HDMI 1.4a
- Audio Interface
- Serial Sound Interface × 1ch
- Communication Interface
- SD Host × 2ch
- PCI-Express 2.0 (1-lane) × 1ch
- Gigabit Ethernet × 1ch
- USB3.1 Gen1 Host/Function × 1ch
- I²C Bus × 4ch
- SCI × 6ch
- UART × 2ch
- Memory Interface
- NAND Flash Interface ONFI1.0 × 1ch
- eMMC 4.5.1 × 1ch
- 32-bit LPDDR4-3200 × 1ch
- Security
- Hardware Security Engine

CPU
- 2× Cortex-A53 (up to 1.0GHz)
- NEON
- FPU
- DRP-AI at 1.0 TOPS/W class
- H.264/265 Multi Codec
- JPEG Codec
- 2D Graphics engine
- Security

Communication I/F
- 2× SD
- 1× PCIe2.0 (1Lane)
- 1× Gbit Ethernet MAC
- 4× IIC
- 6× CSI
- 2× UART
- 1× Motor Control (for Lens)
- 1× Environment Sensor I/F

Memory I/F
- 1× LPDDR4-3200 32-bit
- 1× eMMC
- 1× NAND

Analog
- 20× ADC (12-bit)
**Super Long Term Software Support**

Renesas RZ/G2 and RZ/V2 microprocessors are the only embedded MPUs that meet the long-term support demands for industrial and infrastructure equipment manufacturers through the 10+ year support offered by the Super Long Term Support (SLTS) kernel maintained by the Civil Infrastructure Platform (CIP). The CIP SLTS Linux kernel supports countermeasures against vulnerability to security attacks with a long-term maintenance period of 10 years or more. This reduces Linux maintenance costs and simplifies adoption of reliable industrial-grade Linux.

**Verified Linux Package (VLP) Reduces Cost and Simplifies Design**

The "Verified Linux Package (VLP)" for the RZ/G and RZ/V series is a combination of the Civil Infrastructure Platform (CIP) Core Package and the basic software (Linux BSP, multimedia, graphics, security, etc.) for IoT devices. This packaged software is verified by Renesas and is available. With VLPs, you can start developing applications quickly while minimizing Linux maintenance resources.

*1: RZ/G Reference Board is used for Kernel development as a software development platform for CIP projects.

**Development Environment for AI**

- DRP-AI Translator
  - Converts ONNX* format into object code for DRP-AI.

* ONNX: Open Neural Network Exchange
**RZ/G Series**

**RZ/G Series Roadmap**

**RZ/G2 Platform Highlights**

- **High Performance**
  - 64-bit Arm Cortex-A cores, plus powerful 3D graphics engine and video engine capable of supporting up to 4K UHD, to offer the highest performance

- **Wide Coverage**
  - Entry-level RZ/G2L Group 3 products equipped with Cortex-A55 with improved processing performance have been newly added to the RZ/G2 lineup

- **High Reliability**
  - Built-in Error Correction Code (ECC) for internal and external memory, which is essential for high-reliability mission critical systems

- **Super Long Term Support (SLTS)**
  - Applying Civil Infrastructure Platform (CIP) Linux, the Linux kernel will be provided with over 10 years of support

- **Verified Linux Package**
  - Renesas verifies and provides a Linux package that combines CIP and Linux basic software. Minimize your Linux maintenance resources

**RZ/G2 Group Specification 1**

<table>
<thead>
<tr>
<th>Items</th>
<th>RZ/G2H</th>
<th>RZ/G2M</th>
<th>RZ/G2N</th>
<th>RZ/G2E</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>4x Cortex®<a href="mailto:-A57@1.5GHz">-A57@1.5GHz</a></td>
<td>2x Cortex®<a href="mailto:-A57@1.5GHz">-A57@1.5GHz</a></td>
<td>2x Cortex®<a href="mailto:-A57@1.5GHz">-A57@1.5GHz</a></td>
<td>2x Cortex®<a href="mailto:-A53@1.2GHz">-A53@1.2GHz</a></td>
</tr>
<tr>
<td></td>
<td>4x Cortex®<a href="mailto:-A53@1.2GHz">-A53@1.2GHz</a></td>
<td>4x Cortex®<a href="mailto:-A53@1.2GHz">-A53@1.2GHz</a></td>
<td>4x Cortex®<a href="mailto:-A53@1.2GHz">-A53@1.2GHz</a></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU (Arm® Cortex®-R)</td>
<td>1x Cortex®-R7@800MHz L1,TCM w/ECC</td>
<td>1x Cortex®-R7@800MHz L1,TCM w/ECC</td>
<td>1x Cortex®-R7@800MHz L1,TCM w/ECC</td>
<td>1x Cortex®-R7@800MHz L1,TCM w/ECC</td>
</tr>
<tr>
<td>DRAM I/F</td>
<td>32-bit x2ch LPDDR4(3200) w/ECC</td>
<td>32-bit x2ch LPDDR4(3200) w/ECC</td>
<td>32-bit x1ch LPDDR4(3200) w/ECC</td>
<td>32-bit x1ch DDR3L(1856) w/ECC</td>
</tr>
<tr>
<td>Video in</td>
<td>2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8 input image can be captured</td>
<td>2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8 input image can be captured</td>
<td>2xMIPI-CSI2, 2xDigital (RGB/YCbCr) up to 8 input image can be captured</td>
<td>1xMIPI-CSI2, 1xDigital (RGB/YCbCr) up to 2 input image can be captured</td>
</tr>
<tr>
<td>Video Codec</td>
<td>Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264</td>
<td>Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264</td>
<td>Support up to 4k resolutions Decoding: H.265, Encoding and Decoding: H.264</td>
<td>Support up to FHD resolutions Decoding: H.265, Encoding and Decoding: H.264</td>
</tr>
<tr>
<td>3D GFX</td>
<td>PowerVR GX6650@600MHz</td>
<td>PowerVR GX6250@600MHz</td>
<td>PowerVR GE8300@600MHz</td>
<td>PowerVR GE8300@600MHz</td>
</tr>
<tr>
<td>Display out</td>
<td>1xHDMI, 1xLVDS, 1xDigital RGB</td>
<td>1xHDMI, 1xLVDS, 1xDigital RGB</td>
<td>1xHDMI, 1xLVDS, 1xDigital RGB</td>
<td>2xLVDS or 1xLVDS, 1xDigital RGB</td>
</tr>
<tr>
<td>USB</td>
<td>USB2.0 x2ch (1H, 1H/F/OTG)</td>
<td>USB2.0 x2ch (1H, 1H/F/OTG)</td>
<td>USB2.0 x2ch (1H, 1H/F/OTG)</td>
<td>USB2.0 x1ch (H/F) USB3.0/0.2 x1ch (DRD)</td>
</tr>
<tr>
<td></td>
<td>USB3.0/0.2 x1ch (DRD)</td>
<td>USB3.0/0.2 x1ch (DRD)</td>
<td>USB3.0/0.2 x1ch (DRD)</td>
<td>USB3.0/0.2 x1ch (DRD)</td>
</tr>
<tr>
<td>Gbit Ether</td>
<td>1ch</td>
<td>1ch</td>
<td>1ch</td>
<td>1ch</td>
</tr>
<tr>
<td>CAN</td>
<td>2ch (support CAN-FD)</td>
<td>2ch (support CAN-FD)</td>
<td>2ch (support CAN-FD)</td>
<td>2ch (support CAN-FD)</td>
</tr>
<tr>
<td>PCIe</td>
<td>2ch (Rev2.0 1Lane)</td>
<td>2ch (Rev2.0 1Lane)</td>
<td>2ch (Rev2.0 1Lane)</td>
<td>1ch (Rev2.0 1Lane)</td>
</tr>
<tr>
<td>SATA</td>
<td>1ch (Pin Shared) No</td>
<td>1ch (Pin Shared) No</td>
<td>1ch (Pin Shared) No</td>
<td>No</td>
</tr>
<tr>
<td>Package</td>
<td>1022pin FCB6A, 29mm×29mm 0.8mm ball pitch</td>
<td>1022pin FCB6A, 29mm×29mm 0.8mm ball pitch</td>
<td>1022pin FCB6A, 29mm×29mm 0.8mm ball pitch</td>
<td>552pin FCB6A, 21mm×21mm 0.8mm ball pitch</td>
</tr>
</tbody>
</table>

**Pin Compatible**
**RZ/G2 Group Specification 2**

### Items

<table>
<thead>
<tr>
<th></th>
<th>RZ/G2L</th>
<th>RZ/G2LC</th>
<th>RZ/G2UL (Type2)</th>
<th>RZ/G2UL (Type1)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong>&lt;br&gt;(Arm® Cortex®-A)</td>
<td>1× or 2× Cortex®<a href="mailto:-A55@1.2GHz">-A55@1.2GHz</a> L1,L3 Parity/ECC</td>
<td>1× or 2× Cortex®<a href="mailto:-A55@1.2GHz">-A55@1.2GHz</a> L1,L3 Parity/ECC</td>
<td>1× Cortex®<a href="mailto:-A55@1.0GHz">-A55@1.0GHz</a> L1,L3 Parity/ECC</td>
<td>1× Cortex®<a href="mailto:-A55@1.0GHz">-A55@1.0GHz</a> L1,L3 Parity/ECC</td>
</tr>
<tr>
<td><strong>CPU</strong>&lt;br&gt;(Arm® Cortex®-M)</td>
<td>1× Cortex®-M33@200MHz</td>
<td>1× Cortex®-M33@200MHz</td>
<td>1× Cortex®-M33@200MHz</td>
<td>1× Cortex®-M33@200MHz</td>
</tr>
<tr>
<td><strong>DRAM I/F</strong>&lt;br&gt;</td>
<td>16-bit x1ch DDR4-1600/DDR3L-1333 w/ECC</td>
<td>16-bit x1ch DDR4-1600/DDR3L-1333 w/ECC</td>
<td>16-bit x1ch DDR4-1600/DDR3L-1333 w/ECC</td>
<td>16-bit x1ch DDR4-1600/DDR3L-1333 w/ECC</td>
</tr>
<tr>
<td><strong>Video in</strong>&lt;br&gt;1×MIPI CSI-2 or 1×Digital Parallel input</td>
<td>1×MIPI CSI-2</td>
<td>1×MIPI CSI-2</td>
<td>1×MIPI CSI-2</td>
<td>1×MIPI CSI-2</td>
</tr>
<tr>
<td><strong>Video Codec</strong>&lt;br&gt;Support up to Full HD @30fps resolutions Encoding and Decoding</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>3D FX</strong>&lt;br&gt;Arm Mali-G31 GPU @500MHz</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>Display out</strong>&lt;br&gt;1×MIPI DSI or 1×Digital Parallel output</td>
<td>1×MIPI DSI</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>USB</strong>&lt;br&gt;USB2.0×2ch (1Host, 1Host/Function/OTG)</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>CAN</strong>&lt;br&gt;2ch (support CAN-FD)</td>
<td>2ch</td>
<td>2ch</td>
<td>2ch</td>
<td>2ch</td>
</tr>
<tr>
<td><strong>T2-bit ADC</strong>&lt;br&gt;8ch</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td><strong>Package</strong>&lt;br&gt;551pin LFBGA, 21mm×21mm 0.8mm ball pitch 456pin LFBGA, 15mm×15mm 0.5mm ball pitch</td>
<td>361pin LFBGA, 13mm×13mm 0.5mm ball pitch</td>
<td>361pin LFBGA, 13mm×13mm 0.5mm ball pitch</td>
<td>361pin LFBGA, 13mm×13mm 0.5mm ball pitch</td>
<td></td>
</tr>
</tbody>
</table>

**Super Long Term Software Support**

Renesas RZ/G2 and RZ/V2 microprocessors are the only embedded MPUs that meet the long-term support demands for industrial and infrastructure equipment manufacturers through the 10+ year support offered by the Super Long Term Support (SLTS) kernel maintained by the Civil Infrastructure Platform (CIP). The CIP SLTS Linux kernel supports countermeasures against vulnerability to security attacks with a long-term maintenance period of 10 years or more. This reduces Linux maintenance costs and simplifies adoption of reliable industrial-grade Linux.

**Verified Linux Package (VLP) Reduces Cost and Simplifies Design**

The “Verified Linux Package (VLP)” for the RZ/G and RZ/V series is a combination of the Civil Infrastructure Platform (CIP) Core Package and the basic software (Linux BSP, multimedia, graphics, security, etc.) for IoT devices. This packaged software is verified by Renesas and is available from the Renesas RZ Linux platform site. With VLPs, you can start developing applications quickly while minimizing Linux maintenance resources.
Flexible Development Kits

RZ/G2 development kits support the industry standard 96Boards specification and SMARC specification to enable evaluation and speed development with a wide variety of mezzanine boards and existing carrier boards. Renesas provides circuit schematics, component BOMs, and board layout data to make it easy to spin your own custom hardware.

- **RZ/G2H,G2M,G2N Development Kit (96Boards format compatible)**
  - Main Memory: 4 GB DDR4
  - QSPI NOR FLASH 64 MByte
  - I²C EEPROM 512 Byte
  - External Storage: micro SD × 1
  - Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
  - HDMI out / LVDS out or MIPI DSI out
  - Wi-Fi + BT

- **RZ/G2L SMARC v2.1 Module board + Carrier Board**
  - Module board (Dimension: 82mm × 50mm)
    - Processor: RZ/G2L / RZ/G2LC / RZ/G2UL
    - Main Memory: 2GB DDR4 (1GB ×2)
    - QSPI NOR FLASH: 64MB
    - eMMC Memory: 64GB
    - External Storage: micro SD ×1
    - A/D Converter Interface ×6
    - JTAG connector
  - Carrier board (Dimension: 160mm × 100mm)
    - Gigabit Ethernet ×2
    - USB2.0 × 2ch (OTG ×1ch, Host ×1ch)
    - MIPI CSI-2 Camera connector (can connect to Google Coral Camera)
    - Micro HDMI (output) connector
    - CAN-FD ×2
    - External Storage: micro SD ×1
    - Audio Line in ×1
    - Audio Line out ×1
    - PMOD ×2
    - USB-Type C for Power Input

- **RZ/G2E Development Kit (96Boards format compatible)**
  - Main Memory: 2 GB DDR3L
  - QSPI NOR FLASH 64 MByte
  - I²C EEPROM 512 Byte
  - External Storage: micro SD × 1
  - Connectivity: USB 2.0 × 2ch, USB 3.0 × 1ch, GbE × 1
  - HDMI out / LVDS out or MIPI DSI out
  - Wi-Fi + BT
**HMI Solutions**

**Max Display resolution**
- 4K (3840 × 2160)
- Full HD (1920 × 1080)
- WXGA and below (1280 × 768)

**RZ/G2H (R8A774Ex)**

**CPU core**
- Arm® Cortex®-A57, quad-core
- Arm® Cortex®-A53, quad-core
- Arm® Cortex®-R7, single-core

**Max. operating frequency**
- 1.5GHz
- 1.2GHz
- 800MHz

**Cache memory**
- Cortex®-A57: 512KB with ECC
- Cortex®-A53: 2MB
- Cortex®-R7: 32KB

**System RAM**
- 384KB

**Video codec module**
- VCP4 × 1

**IP converter module**

**Video image processing functions**
- Color conversion, image enlargement/reduction, filtering

**Audio functions**
- Sampling rate converter × 10 channels
- Serial sound interface × 10 channels
- Storage interfaces
- USB 3.0 DDR × 1 channel
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1 channel)
- SD host interface × 4 channels
- Multimedia card interface × 2 channels
- Serial ATA interface × 1 channel
- Other peripheral functions
  - 32-bit timer × 15 channels
  - PWM timer × 7 channels
  - I²C bus interface × 7 channels
  - Serial communication interface (SCI) × 6 channels
  - Quad serial peripheral interface (QSPI) × 2 channels (boot support)
  - Clock-synchronous serial interface (MSIOP) × 4 channels (SPI/IIS support)
  - Ethernet controller with AVB support (support for IEEE 802.1BA, IEEE 802.1AS, IEEE 802.1Qav, and IEEE 1722)
  - Controller area network (CAN) interface × 2 channels
  - Interrupt controller (INTC)
  - Clock generator (CPG): on-chip PLL
  - On-chip debug function
  - 3-way Video in
  - MIPI-CSI2 (1 × 4L, 1 × 2L)
  - 2 × Digital

**Video Signal Processor**
- 32-bit × 2ch LPDDR4-3200 (ECC)
- 4 × SPI
- 2 × CAN2.0B
- 7 × I²C
- 1 × DVFS ctrl
- Serial data bus: 32 bits × 2 channels
- External expansion
- Ability to connect flash ROM or SRAM directly
- Data bus width: 32 bits × 2 channels
- Data bus width: 8/16 bits
- PCI Express 2.0: 1 Lane × 2 channels (one of PHY is shared with Serial ATA)
- 3D graphics
- PowerVR™ GX6650
- Video functions
  - Video display interface × 3 channels (1 channel: HDMI(option), 1 channel: LVDS, 1 channel: RGB888)
  - Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video display interface × 3 channels
  - PowerVR™ GX6650, 2K functions: 3D Graphics, Video Codec
  - OS: Linux (RichOS)

**Operating System**
- RTOS
- 32-bit Linux
- 64-bit Linux

**Memory I/F**
- 2 × PCIe2.0 (1Lane)
- SATA (Rev.3.2) (shared)
- 4 × USB2.0 (2H, 2H/F/OTG)
- Ethernet AVB (16bps)
- 2 × CAN2.0B
- 6 × UART, 5 × H-UART
- 7 × I²C
- 1 × DVFS ctrl
- 4 × USB2.0 (2H, 2H/F/OTG)
- 2 × PCIe2.0 (1Lane)
- SATA (Rev.3.2) (shared)
- 4 × USB2.0 (2H, 2H/F/OTG)
- Ethernet AVB (16bps)
- 2 × CAN2.0B
- 6 × UART, 5 × H-UART
- 7 × I²C
- 1 × DVFS ctrl

**Connectivity**
- 16-bit ExtBus/SGRAM
- 1 Gbps
- 1 × Hyperflash
- 8 × Video in
- MIPI-CSI2 (1 × 4L, 1 × 2L)
- 2 × Digital
- 3 × Display out
- 1 × Digital out, 1 × LVDS
- 1 × HDMI
- 8 × Video in
- MIPI-CSI2 (1 × 4L, 1 × 2L)
- 2 × Digital
- Video display interface × 3 channels
- PowerVR™ GX6650, 2K functions: 3D Graphics, Video Codec
- OS: Linux (RichOS)
## RZ/G2M (R8A774Ax)

**CPU**
- Arm® Cortex®-A57, quad-core
- Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core
- Max. operating frequency: 800MHz

**Cache memory (Cortex®-A57)**
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 2MB
- External memory
  - L1 instruction cache: 32KB
  - L1 data cache: 32KB
  - I-TCM: 32KB
  - D-TCM: 32KB

**Cache memory (Cortex®-R7)**
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- External memory
  - Ability to connect LPDDR4-SRAM via DDR dedicated bus
  - Data bus width: 32 bits × 2 channels
  - External expansion
  - Ability to connect flash ROM or SRAM directly
  - Data bus width: 8/16 bits

**Audio IPs**
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- PowerVR™ GE7800
- Video codec module: VCP4 × 1 channel

**Video functions**
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video output interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video display interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

**PowerVR™ GE7800**
- Video functions
- Video codec module: VCP4 × 1 channel
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video display interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

## RZ/G2N (R8A774Bx)

**CPU**
- Arm® Cortex®-A57, quad-core
- Max. operating frequency: 1.5GHz
- Arm® Cortex®-R7, single-core
- Max. operating frequency: 800MHz

**Cache memory (Cortex®-A57)**
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- L2 cache: 2MB
- External memory
  - L1 instruction cache: 32KB
  - L1 data cache: 32KB
  - I-TCM: 32KB
  - D-TCM: 32KB

**Cache memory (Cortex®-R7)**
- L1 instruction cache: 32KB
- L1 data cache: 32KB
- External memory
  - Ability to connect LPDDR4-SRAM via DDR dedicated bus
  - Data bus width: 32 bits × 1 channel
  - External expansion
  - Ability to connect flash ROM or SRAM directly
  - Data bus width: 8/16 bits

**Audio IPs**
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video input interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))
- PowerVR™ GE7800
- Video functions
- Video codec module: VCP4 × 1 channel
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video display interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

**PowerVR™ GE7800**
- Video functions
- Video codec module: VCP4 × 1 channel
- Video display interface × 3 channels (1 channel: HDMI/1option, 1 channel: LVDS, 1 channel: RGB888)
- Video display interface × 4 channels (2 channels: MIPI-CSI2, 2 channels: Digital(RGB/YCbCr))

---

**Diagram (RZ/G2M)**

**Diagram (RZ/G2N)**
### RZ/G2LC(R9A07G044Cxx) block diagram

**CPU**
- Arm® Cortex®-A55, dual-core
- Arm® Cortex®-M33, single-core
- Max. operating frequency: 1.2GHz
- Max. operating frequency: 200MHz
- Cache memory (Cortex®-A55)
- Device Unique ID
- JTAG Disable
- D-L1$: 32KB w/ECC
- External memory
- Cache memory (Cortex®-A55)
- Video functions
- Video display interface: MIPI DSI × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions (Reziser and Color Space / Color Format Conversion)
- CPU core
- Internal and External memory
- Video functions
- Video display interface: MIPI DSI × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions
- Analog interface
- Digital parallel output × 1 channel

**Audio functions**
- Sampling rate converter x 1 channel
- Serial sound interface x 2 channels
- Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)
- Other peripheral functions
- 32-bit timer x 1 channel
- 16-bit timer x 5 channels
- PWM timer x 4 channels
- I²C bus interface x 4 channels
- Serial communication interface (SCI) x 2 channels
- SPI Multi I/O Bus Controller x 1 channel (Hot Double data rate)
- Serial Peripheral Interface (RSPI) x 3 channels
- Gigabit Ethernet controller x 1 channel
- Controller area network (CAN) interface x 2 channels (support CAN FD)
- Interrupt controller
- Clock generator (CPU): on-chip PLL
- On-chip debug function

### RZ/G2UL(R9A07G043Uxx) block diagram

**CPU**
- Arm® Cortex®-A55, single-core
- Arm® Cortex®-M33, single-core
- Max. operating frequency: 1.0GHz
- Max. operating frequency: 200MHz
- Cache memory (Cortex®-A55)
- Device Unique ID
- JTAG Disable
- D-L1$: 32KB w/Parity
- External memory
- Cache memory (Cortex®-A55)
- Video functions
- Video display interface: MIPI DSI × 1 channel
- Video input interface: MIPI CSI-2 × 1 channel
- Video image processing functions
- Analog interface
- Digital parallel output × 1 channel

**Audio functions**
- Sampling rate converter x 1 channel
- Serial sound interface x 4 channels
- Storage interfaces
- USB 2.0 × 2 channels (Host only 1 channel/Host-Function 1channel)
- SD host interface × 2 channels
- Multimedia card interface x 1 channel (Shared with SDHI)
- Other peripheral functions
- 16-bit timer x 8 channels
- I²C bus interface x 4 channels
- Serial communication interface with FIFO (SCIF) x 5 channels
- Serial communication interface (SCI) x 2 channels
- SPI Multi I/O Bus Controller x 1 channel (Hot Double data rate)
- Serial Peripheral Interface (RSPI) x 3 channels
- Gigabit Ethernet controller x 2 channels
- Controller area network (CAN) interface x 2 channels (support CAN FD)
- 12-bit A/D converter x 2 channels
- Interrupt controller
- Clock generator (CPU): on-chip PLL
- On-chip debug function
RZ/G Series Application

The HMI can be made more expressive by making full use of the 3D graphics and video capabilities.

RZ/G Linux Platform Solutions from Partner Companies

Visit the webpage below for the latest information on RZ/G Linux Platform development tools, including solutions from partner companies.
https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rzg
RZ/A Series

RZ/A Series Roadmap

RZ/A1H
Cortex®-A9 (400MHz)
10MB, WXGA, 2D

RZ/A1M
Cortex®-A9 (400MHz)
5MB, WXGA, 2D

RZ/A1L
Cortex®-A9 (400MHz)
3MB XGA

RZ/A1LU
Cortex®-A9 (400MHz)
3MB, XGA, JPEG

RZ/A2M
Cortex®-A9 (528MHz)
4MB, XGA, 2D

RZ/A-next


RZ/A Series Application

Intercoms White goods White goods Vending machines Digital signage Diagnostic panels
Barcode scanners Office equipment Image sensor Data communication modules (telematics, emergency communications)
Robot Biometrics Handwriting recognition input devices

RZ/A Series Features

- Large-capacity on-chip RAM: 10MB
- Graphics display and camera input capabilities on a single chip
- Rich peripheral functions and software
- Large-capacity on-chip RAM: 10MB

DRAM-less solution

Advantages
• No need to design a high-speed interface
• Reduced mounting area
• Reduced PCB cost
• No DRAM procurement issues
• Reduced EMI noise

6 PCB layers for 1.2V, 3.3V, 1.5V/0.75V (DDR3)

4 PCB layers for 1.2V, 3.3V
### Rich peripheral functions and software

**Graphics**
- On-chip 2D graphics accelerator for fast image rendering
- "Smooth" and "beautiful" graphics display by utilizing large-capacity on-chip RAM to the full

**Network**
- Wired LAN/wireless LAN
- Narrowing down by RZ/A1 of only valuable information for transmission over the network
- Reduction of network communication volume/ability to increase number of cameras flexibly

**Example system solution**
- RZ/A
- CPU
- HMI functions
- Large-capacity on-chip RAM

**Camera**
- Real-time correction of distorted images
- Ability to connect analog CMOS cameras
- Ability to process imported images and extract a variety of information

**DRP (Dynamically Reconfigurable Processor)**
- Ability to accelerate image processing for applications such as barcode readers and biometric authentication

With ample peripheral functions and software, a single chip can cover a wide range of fields, including display, camera input, communication, and audio functions.

The bus configuration with independent buses for images and hardware-based superimposition processing make it easy to create graphical applications.
### DRP Library
- The RZ/A2M’s DRP* can process applications such as image processing several to dozens of times faster than software processing that relies on the CPU, resulting in a faster system.
- A wide variety of DRP libraries are available, and users do not need to code the DRP itself by calling it from user programs using the DRP driver.
- The functions processed by the DRP can be dynamically changed from the user program, allowing multiple different processes to be used in combination.

### Image Signal Processing (Simple ISP group)
- Simple ISP with Color Calibration and 3DNR
- Simple ISP with Object Detection by Color (HSV)
- Simple ISP with Distortion Correction, etc.

### Image Transformation and Filter
- Bayer to Grayscale / RGB
- Gamma Correction
- Median Blur, etc.

### Feature Detection
- Canny Edge Detection
- Harris’ Corner Detection
- Find Contours, etc.

### RZ/A2M Group
**CPU (Arm® Cortex®-A9)**
- Operating frequency: 528MHz
- Single-precision/double-precision FPU
- Arm® NEON™

**On-chip memory**
- SRAM: 4MB
- I CACHE: 32KB D Cache: 32KB
- L2 Cache: 128KB

**Graphics**
- VDC6 (LCDC)
- Timing Controller
- Digital Input
- CMOS Camera I/F
- 2D Graphics Engine
- Sprite Engine
- JPEG Codec Engine

**Security (Option)**
- Secure Boot
- Crypto Engine
- TRNG
- Device Unique ID
- JTAG Disable

**Main memory interface functions**
- NOR flash, SDRAM, NAND flash
- Serial flash: 1-bit/4-bit/8-bit: 1 channel, 8-bit: 1 channel (ability to run stored programs directly)
- SD/MMC host interface: 2 channels

**Main communication functions**
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 2 channels
- SCIF: 5 channels
- I²C: 4 channels
- SCI: 4 channels
- RSPI: 3 channels
- CAN-FD: 2 channels

**Optional functions**
- DRP (Dynamically Reconfigurable Processor)

**Package**
- 176-LFBGA (13mm×13mm, 0.8mm pitch)
- 256-LFBGA (11mm×11mm, 0.5mm pitch)
- 272-FBGA (17mm×17mm, 0.8mm pitch)
- 324-FBGA (19mm×19mm, 0.8mm pitch)
**RZ/A1H Group and RZ/A1M Group (Pin Compatible)**

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- RZ/A1H: 10MB
- RZ/A1M: 5MB

Main graphics and camera input functions
- Video display controller (VDC5): 2 channels
- LCD output: Max. WXGA
- Screen superimposition: 4 layers
- Video input: Max. XGA (CVBS analog input supported)
- CMOS camera input (CEU): 1 channel
- PAL/NTSC decoder (DVDEC): 2 channels
- Distortion compensation unit (IMR): 1 channel
- Open VG accelerator: 1 channel
- JPEG encoding engine: 1 channel

Main memory interface functions
- NOR flash, SDRAM, NAND flash
- SPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 8 channels
- I²C: 4 channels
- SSI: 6 channels
- RSPI: 5 channels
- Ethernet AVB: 1 channel
- CAN: 5 channels

Package
- 256-LFQFP (11mm × 11mm, 0.5mm pitch)
- 256-LFQFP (28mm × 28mm, 0.4mm pitch)
- 324-FBGA (19mm × 19mm, 0.8mm pitch)

---

**RZ/A1LU Group**

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- 3MB

Main graphics and camera input functions
- LCD controller (VDC5): 1 channel
- LCD output: Max. WXGA
- Screen superimposition: 3 layers
- Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel

Main memory interface functions
- NOR flash, SDRAM
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I²C: 4 channels
- RSPI: 3 channels
- Ethernet AVB: 1 channel
- CAN: 2 channels

Package
- 176-LFQFP (8mm × 8mm, 0.5mm pitch)
- 176-LFQFP (24mm × 24mm, 0.5mm pitch)
- 208-LFQFP (28mm × 28mm, 0.5mm pitch)

---

**RZ/A1H, and RZ/A1M block diagram**

**CPU**
- Cortex®-A9 400MHz
- NEON™
- FPU

**Timers**
- MTU2: 16-bit × 8ch
- WDT: 8-bit × 1ch
- OS Timer: 32-bit × 2ch
- PWM Timer: 16ch
- Real-Time CLK

**System**
- DMAC 16ch
- Interrupt Controller
- Clock Generation with SSCG
- JPEG Debug
- Customer Unique ID*

**Audio**
- SCUX 4ch ASRC
- CDRUM DEC
- Sound Generator

**Analog**
- ADC: 12-bit × 8ch

**Memory**
- SDRAM: 512MB
- SDRAM L2 Cache: 128 KB
- Cache: 32 KB × 32 KB

---

**RZ/A1LU block diagram**

**CPU**
- Cortex®-A9 400MHz
- NEON™
- FPU

**Timers**
- MTU2: 16-bit × 8ch
- WDT: 8-bit × 1ch
- OS Timer: 32-bit × 2ch
- PWM Timer: 16ch
- Real-Time CLK

**System**
- DMAC 16ch
- Interrupt Controller
- Clock Generation with SSCG
- JPEG Debug
- Customer Unique ID*

**Audio**
- SCUX 4ch ASRC

**Analog**
- ADC: 12-bit × 8ch

---

**Memory**
- SDRAM: 512MB
- SDRAM L2 Cache: 128 KB
- Cache: 32 KB × 32 KB

---

**Interfaces**
- 10/100 Ether MAC
- CAN
- CAN
- USB2.0
- HS 2ch Host/Func
- NAND Flash
- Nand Flash
- External Bus 32-bit RDM, 320AM
- SDRAM, PCMCIA
- SPI Multi
- SCIF
- RSPI
- CAN
- CAN
- Smart Card I/F
- InDA
- LIN Master
- Ethernet AVB
RZ/A1L, RZ/A1LC Group

CPU (Arm® Cortex®-A9)
- Operating frequency: 400MHz
- Single-precision/double-precision FPU
- Arm® NEON™

On-chip memory
- RZ/A1L: 3MB
- RZ/A1LC: 2MB

Main graphics and camera input functions
- LCD controller (VDC5): 1 channel
- Screen superimposition: 3 layers
- Video input: Max. XGA
- CMOS camera input (CEU): 1 channel

Main memory interface functions
- NOR flash, SDRAM, NAND flash
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

Main communication functions
- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1 channel
- SCIF: 5 channels
- I²C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels

Package
- 176-LFBGA (8mm × 8mm, 0.5mm pitch)
- 176-LFQFP (24mm × 24mm, 0.5mm pitch)
- 208-LFQFP (28mm × 28mm, 0.5mm pitch)
- 233-FBGA (15mm × 15mm, 0.8mm pitch)

* RZ/A1L Group specification only.
### RZ/A Series: Development Environments (Integrated Development Environments)

<table>
<thead>
<tr>
<th>Development environments</th>
<th>arm</th>
<th>IAR Systems</th>
<th>eSOL</th>
<th>Renesas</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS-5</td>
<td></td>
<td>IAR Embedded Workbench® for Arm®</td>
<td>eBinder</td>
<td>e’studio*3</td>
</tr>
<tr>
<td>Embedded Workbench® for Arm®</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>eBinder</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>e’studio*3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Development environments**

**Compilers**
- Arm CC*1
- IAR C/C++ compiler*2
- Arm CC*1
- GNU tool*3

**ICEs**
- DSTREAM™
- ULINKpro™
- ULINKproD™
- ULINK2™
- PARTNER-Jet2 from Kyoto Microcomputer Co., Ltd.
- adviceLUNA II from DTS INSIGHT Corporation
- PARTNER-Jet2
- microVIEW-PLUS
- adviceLUNA II
- PALMICE4

**Supported compilers**
- exeGCC from Kyoto Microcomputer
- GNU tool*1
- Arm CC*2
- IAR C/C++ compiler*2
- GNU tool*3 etc.
- Arm CC*2
- IAR C/C++ compiler*3
- GNU tool*3 etc.

---

### RZ/A Series: Development Tools (Debuggers, ICEs)

<table>
<thead>
<tr>
<th>Debuggers</th>
<th>ICEs</th>
<th>Computex</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARTNER-Jet2</td>
<td>microVIEW-PLUS</td>
<td>CSIDE version 7</td>
</tr>
<tr>
<td></td>
<td>adviceLUNA II</td>
<td>PALMICE4</td>
</tr>
</tbody>
</table>

**Debuggers**
- PARTNER-Jet2
- microVIEW-PLUS
- CSIDE version 7

**ICEs**
- adviceLUNA II
- PALMICE4

**Supported compilers**
- exeGCC from Kyoto Microcomputer
- GNU tool*1
- Arm CC*2
- IAR C/C++ compiler*2
- GNU tool*3 etc.
- Arm CC*2
- IAR C/C++ compiler*3
- GNU tool*3 etc.

---

### RZ/A Series: Solutions from Partner Companies

Visit the webpage below for the latest information on RZ/A Series development tools, including solutions from partner companies.
https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rza
**RZ/T Series**

**RZ/T Series Roadmap**

- **RZ/T1**
  - Cortex®-R4 (600/450/300MHz)
  - 544K TCM + 1MB, EtherCAT

- **RZ/T1**
  - Cortex®-R4 (600/450MHz)
  - 544K TCM + 1MB, R-IN Engine

- **RZ/T1**
  - Cortex®-R4 (450MHz)
  - 544K TCM

- **RZ/T-next**
  - Higher Performance
  - Safety

**RZ/T Series Features**

- High-performance, high-speed real-time control
- R-IN engine
- Integrated peripheral functions

- **High-performance, high-speed real-time control**

  - Cortex®-R4 Processor with FPU

  - Tightly Coupled Memory (ATCM) 512KB (w/ ECC)
  - Tightly Coupled Memory (BTCM) 32KB (w/ ECC)
  - Single-precision/ double-precision FPU
  - 300MHz/450MHz/600MHz

- **High-speed RAM directly connected to the CPU for high-speed processing and dependable real-time responsiveness without caching**
- **ECC for enhanced reliability**
- **Vectored Interrupt Controller (VIC) to assure interrupt responsiveness suitable for embedded control**
- **R-IN engine**

  - R-IN engine industrial Ethernet communication accelerator performs standard Ethernet processing in hardware.
  - Network processing is up to four times as fast.

- **Integrated peripheral functions**

  - The encoder interface was external with conventional FPGA or ASIC approaches but is now integrated on-chip.
  - This one-chip AC servo solution helps reduce the component count and save space.
RZ/T Series Application

High-speed operation at 300MHz/450MHz/600MHz provides higher performance and improved functionality for industrial equipment such as industrial motors or AC servo drivers. Products incorporating the R-IN engine accelerator for industrial Ethernet communication can also handle a variety of industrial Ethernet processing tasks without sacrificing real-time performance.

RZ/T1 Group

High performance CPU
- Arm® Cortex®-R4 Processor
- Operating frequency: 300MHz/450MHz/600MHz
- High-performance, high-speed real-time control
- Single-precision/double-precision floating-point unit

R-IN engine (option)
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- R-IN engine instruction memory: 512KB (w/ ECC) + data memory: 512KB (w/ ECC)
- On-chip memory
- Tightly Coupled Memory: 512KB (w/ ECC) + 32KB (w/ ECC)
- Extended RAM instruction memory 512KB (w/ ECC) + data memory: 512KB (w/ ECC) (option)

Features
- Industrial Ethernet communication accelerator with multi-protocol support (R-IN engine) (option)
- EtherCAT slave controller (option)
- PWM timer: MTU3a, GPT
- Encoder interface (Nikon A-format™/BiSS-C/EnDat2.2/HIPERFACE DSL®/Tamagawa) (option)

Note: 2ch encoder support depends on the combination of the selected protocol.
- High Speed USB
- Secure boot (option)
- Safety functions
  - ECC memory
  - CRC (32-bit)
  - Independent WDT: Operating on dedicated on-chip oscillator
- \( \Delta \Sigma \) interface
- 100Mbps EtherMAC (with Ethernet switch)
- Ethernet accelerator
- Power supply voltage: 1.2V, 3.3V

Package
- FBGA 320pin (17mm x 17mm, 0.8mm pitch)
- QFP 176pin (20mm x 20mm, 0.4mm pitch)

CPU

Cortex®-R4 Processor with FPU
300MHz/450MHz/600MHz
1.2V (Core), 3.3V (I/O)

FPU MPU Debug VIC

Memory

ATCM: 512KB with ECC
BTCM: 32KB with ECC

I Cache: 8KB w/ECC
D Cache: 8KB w/ECC

Extended RAM: 1MB w/ECC (option)

R-IN Engine (option)

CPU Cortex®-M3
125MHz, 1.2V (Core), 3.3V (I/O)

MPU Debug NVIC

Memory

Instruction RAM: 512KB with ECC
Data RAM: 512KB with ECC

System

2 x 16ch DMAC
JTAG Debug
Clock Generation Circuit

Timers

8 x 16-bit + 1 x 32-bit MTU3a
6 x 16-bit CMT
2 x 32-bit CMT2
4 x 16-bit GPT
1 x WDT
1 x IWD T
12 x 16-bit TPU
2 x 4gr× 4-bit PPG

Security

Secure boot (option)
JTAG w/ disable function

Interfaces

5 x SCI
2 x CAN
1 x EthernetMAC (100Mbps)
With switch + IEEE1588
USB 2.0 HS (Host/F unc)
GPIO
\( \Delta \Sigma /F \)
EtherCAT Slave Controller (option)

Memory Interfaces

4 × SPI
QSPI (Flash I/F) with Direct Access from CPU
SRAM I/F (32-bit bus)
SDRAM I/F (32-bit bus)
Burst ROM I/F (32-bit bus)

Analog

(8 x 16) × 12-bit ADC

Encoder interfaces (option)
## RZ/T1 Product Lineup

<table>
<thead>
<tr>
<th>CPU</th>
<th>Tight Coupled Memory</th>
<th>Extended RAM</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>600 MHz + R-IN Engine (150MHz)</td>
<td>512KB +32KB</td>
<td>(1MB for R-IN)</td>
<td>R7S910017</td>
<td>R7S910018</td>
</tr>
<tr>
<td>450 MHz + R-IN Engine (150MHz)</td>
<td>512KB +32KB</td>
<td>(1MB for R-IN)</td>
<td>R7S910015</td>
<td>R7S910016</td>
</tr>
<tr>
<td>600 MHz</td>
<td>512KB +32KB</td>
<td>1MB</td>
<td>R7S910007</td>
<td>R7S910013</td>
</tr>
<tr>
<td>450 MHz</td>
<td>512KB +32KB</td>
<td>1MB</td>
<td>R7S910006</td>
<td>R7S910025</td>
</tr>
<tr>
<td>300 MHz</td>
<td>512KB +32KB</td>
<td>–</td>
<td>R7S910001</td>
<td>R7S910002</td>
</tr>
<tr>
<td>Package</td>
<td>176 QFP</td>
<td>320 BGA</td>
<td>320 BGA</td>
<td>320 BGA</td>
</tr>
<tr>
<td>Encoder I/F</td>
<td>–</td>
<td>–</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Industrial Ethernet</td>
<td>(Standard Ethernet)</td>
<td>EtherCAT</td>
<td>Multi-protocol support</td>
<td></td>
</tr>
</tbody>
</table>
Utilizing the Arm® Ecosystem

Utilizing Renesas’ Experience and the Arm® Ecosystem

Customers can benefit from solutions combining Renesas’ accumulated experience in the microcontroller industry and the global ecosystem of Arm® partners. Products such as development environments, OS, and middleware are available from partner companies supporting the RZ/T series.

RZ/T Series: Development Environments (Integrated Development Environments)

<table>
<thead>
<tr>
<th>Development environments</th>
<th>Compilers</th>
<th>Other tools</th>
<th>IDEs</th>
</tr>
</thead>
<tbody>
<tr>
<td>IAR Embedded Workbench® for Arm®</td>
<td>IAR C/C++ compiler*2</td>
<td>AP4 code generation tool from Renesas is compatible.</td>
<td>i-jet™/i-jet Trace™ for Arm Cortex®-A/R/M</td>
</tr>
<tr>
<td>DS-5</td>
<td>Arm CC*3</td>
<td>AP4 code generation tool from Renesas is compatible.</td>
<td>JTAGjet-Trace</td>
</tr>
<tr>
<td>e’s studio*4</td>
<td>GNU tool*4</td>
<td>Code generation function available as a plug-in.</td>
<td>DSTREAM™</td>
</tr>
</tbody>
</table>

*1 Eclipse-based development environment from Renesas (http://renesas.com/e2studio)
*2 Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (www.iar.com/EWARM)
*3 Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*4 GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)
*5 Renesas does not handle ICEs from Segger. Contact a sales agent for details.

RZ/T Series: Development Tools (Debuggers, ICEs)

<table>
<thead>
<tr>
<th>Debuggers</th>
<th>IDEs</th>
<th>ICEs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PARTNER-Jet2</td>
<td>microVIEW-PLUS</td>
<td>i-jet™/i-jet Trace™ for Arm Cortex®-A/R/M</td>
</tr>
<tr>
<td>exeGCC from Kyoto Microcomputer</td>
<td>adviceLUNA II</td>
<td>JTAGjet-Trace</td>
</tr>
<tr>
<td>GNU tool*</td>
<td>PALMiCE4</td>
<td>DSTREAM™</td>
</tr>
<tr>
<td>Arm CC*2</td>
<td>Arm CC*2</td>
<td>ULINKpro™</td>
</tr>
<tr>
<td>GNU tool,* etc.</td>
<td>GNU tool,* etc.</td>
<td>ULINKproD™</td>
</tr>
</tbody>
</table>

*1 GNU TOOLS & SUPPORT Website (https://gcc-renesas.com)
*2 Arm CC is included in DS-5. In addition to the popularly priced DS-5 RZ/A and RZ/T editions, a fully functional evaluation version of DS-5 that expires after 30 days is available free of charge. Contact your DS-5 dealer for details.
*3 Two versions of the software are available for download free of charge. One limits the code size to 32KB and can be used with no time limitation. The other has no limit on code size and expires after 30 days. (www.iar.com/EWARM)
e2 studio: Integrated Development Environment Based on Eclipse

e2 studio is an integrated development environment based on the Eclipse open source integrated development environment and CDT plug-ins supporting development in C/C++. The version of e2 studio that is compatible with the RZ/T series provides support for a code generation plug-in.

C/C++ perspective: code generation plug-in

A code generation plug-in is available that enables the user to generate device driver programs for peripheral functions of Renesas microcontrollers (timers, UART, A/D converter, etc.) by entering settings in a graphical user interface. It is possible to specify the processing of multiplexed pins in a pin table and view a pin assignment diagram to confirm the settings.

AP4: Code Generation Support Tool

AP4 is a standalone tool that automatically generates peripheral function control programs (device driver programs) based on settings entered by the user. The build tool (compiler) is selectable. This makes it possible to generate peripheral function control program code to match a specific build tool and enables interoperability with integrated development environments. ([https://www.renesas.com/ap4](https://www.renesas.com/ap4))
The version of AP4 that is compatible with the RZ/T series can generate compatible source code for IAR Embedded Workbench® for Arm® from IAR Systems, Development Studio (DS-5™) from Arm®, and e2 studio (GNU Tools).

AP4

- Automatically generates microcontroller peripheral function control programs (device driver programs).
- Outputs integrated development environment workspace files and program files.

RZ/T Series: Solutions from Partner Companies

Visit the webpage below for the latest information on RZ/T Series development tools, including solutions from partner companies.

RZ/T1-Starter-Kit-Plus  https://www.renesas.com/RZT1-Starter-Kit-Plus

- The Renesas Starter Kit+ for RZ/T1 is the perfect starter kit for developers who are new to the RZ/T1.
- The kit includes an LCD display module, J-LINK Lite debugging emulator, and e² studio integrated development environment so you can start evaluating the RZ/T1 immediately after opening the box.
- Ordering number: RTK7910018S01000BE

- RZ/T1 (R7S910018)
- QSPI FlashROM 64Mbyte
- SDRAM 64Mbyte × 2
- NOR Flash 64Mbyte × 2
- Rich interface
- Serial, USB, CAN
- Digilent Pmod I/F (PMOD connector)
- ΔΣ I/F (DSMI connector)
- Ethernet (10/100Base, EtherCAT) I/F etc.
- Audio codec
- Includes Segger’s simple debug probe “J-LINK Lite”
- Includes LCD for debugging

RZ/T1 Motion Control Solution Kit  https://www.renesas.com/YDRIVE-IT-RZT1

- RZ/T1 Motion Control Solution Kit is a complete hardware and software solution for the Renesas RZ/T1 MPU. It delivers best-in-class processing power and real-time architecture to run tighter control loops, network connectivity to support deterministic communication, and high-speed encoder interface – effectively serving as a connected servo solution on a single chip.
- The kit includes an RZ/T1 CPU card, and a dual channel 3-phase inverter to support dual channel servo motor control with current and position feedback.
- Ordering number: YDRIVE-IT-RZT1

- Package includes all parts needed for motor control evaluation
- Supports safe design and can be used for reference
- Includes multifunction utility tool
- Servo control software is available

https://www.renesas.com/YDRIVE-IT-RZT1
https://www.renesas.com/RZT1-Starter-Kit-Plus
RZ/N Series

RZ/N Series Roadmap


Under Development

RZ/N1D
Cortex®-A7 Dual DDR, 5port Ether

RZ/N1S
Cortex®-A7 6M, 5port Ether

RZ/N1L
Cortex®-M3 6M, 3port Ether

RZ/N-next
for TSN

RZ/N Series Features

1. Provides optimized microcontrollers for a variety of industrial network applications
2. Integrated R-IN engine (accelerator) supporting main industrial Ethernet protocols
3. Redundant network configuration reduces network downtime to zero

1. Provides optimized microcontrollers for a variety of industrial network applications

The three CPU types lineup and integrated 5-port gigabit Ethernet switch make it possible to provide the optimal microcontrollers for a wide range of industrial network applications.

— Lineup of three CPU types for excellent hardware scalability: Dual-core Cortex®-A7 (500MHz × 2), single-core Cortex®-A7 (500MHz), and R-IN engine only (125MHz).

— 5-port gigabit Ethernet switch and two independent MAC units support applications such as PLC devices and Ethernet switches. Integration of peripheral components helps reduce BOM cost.

Conventional configuration

Controller

DDR2/3
App CPU
(high-performance)
Communication CPU
Ethernet switch

Ethernet switch

SRAM
App CPU
(medium-performance)
Communication CPU
Ethernet switch

Remote IO

SRAM
Communication CPU
Ethernet switch

Configuration using RZ/N1

Controller

DDR2/3
App CPU
Communication CPU
Ethernet switch

Ethernet switch

App CPU
Large-capacity RAM
R-IN engine
Ethernet switch

Remote IO

Large-capacity RAM
R-IN engine
Ethernet switch
2. Integrated R-IN engine (accelerator) supporting main industrial Ethernet protocols

The R-IN engine accelerator supports a wide range of protocols and enables high-speed processing. It reduces the load on the main CPU (Arm® Cortex®-A7) and contributes to highly efficient application control.

3. Redundant network configuration reduces network downtime to zero

Advanced redundant network configuration support helps eliminate network downtime.
- Redundant network connections: Parallel Redundancy Protocol (PRP)
- Looped network connections: HSR (High-availability Seamless Redundancy), DLR (Device Level Ring), RSTP (Rapid Spawning Trees)

RZ/N Series Application
### RZ/N1D Group

**CPU core**
- Arm® Cortex®-A7 dual-core processor
- Operating frequency: 500MHz

**Cache memory**
- L1 I-cache: 16KB x 2, D-cache: 16KB x 2
- L2: 256KB

**Internal memory**
- 2MB (ECC)

**External memory**
- DDR2/DDR3 controller
- Quad I/O SPI
- SDIO eMMC
- NAND flash controller

**R-IN engine**
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator

**Main Ethernet communication functions**
- EtherCAT slave controller
- Sercos® III slave controller
- HSR switch (400-pin)
- 5-port Ethernet switch

**Other communication functions**
- UART x 8 channels
- I²C x 2 channels
- SPI x 6 channels (master x 4 channels, slave x 2 channels)
- CAN

**Other functions**
- LCD controller
- ADC: 12-bit x 8 channels x 2 units (406-pin)
- ADC: 12-bit x 8 channels x 1 unit (324-pin)
- PWM timer, GPT

**Package**
- 400-pin LFGBA, 17 x 17mm, 0.8mm pin pitch
- 324-pin LFGBA, 15 x 15mm, 0.8mm pin pitch

**Operating temperature**
- Tj = −40°C to +110°C

---

### Application example: Programmable logic controller block diagram

![Programmable logic controller block diagram](image-url)
RZ/N1S Group

CPU core
- Arm® Cortex®-A7 single-core processor
- Operating frequency: 500MHz
- Cache memory
  - L1-cache: 16KB, D-cache: 16KB
  - L2: 128KB
- Internal memory
  - 6MB (ECC)
- External memory
  - Quad I/O SPI
  - SDIO eMMC
- NAND flash controller
- R-IN engine
- Arm® Cortex®-M3
- Operating frequency: 125MHz
- HW-RTOS accelerator
- Ethernet accelerator
- Main Ethernet communication functions
  - EtherCAT slave controller
  - Sercos® III slave controller
  - 5-port Ethernet switch
- Other communication functions
  - UART x 8 channels
  - I²C x 2 channels
  - SPI x 6 channels (master x 4 channels, slave x 2 channels)
  - CAN
- Other functions
  - LCD controller
  - ADC: 12-bit x 8 channels x 1 unit
  - PWM timer, GPT
- Package
  - 324-pin LFBGA, 15 x 15mm, 0.8mm pin pitch
  - 196-pin LFBGA, 12 x 12mm, 0.8mm pin pitch
- Operating temperature
  - Tj = -40°C to +110°C

RZ/N1S Group block diagram

CPU
- Arm® Cortex®-A7 Single Core Processor
- 500MHz

Memory Interface
- Quad SPI
- NAND Flash I/F

Memory
- L3 Cache
- DDR3 x 1024 MB (with ECC)

Interface
- 8 x UART
- 2 x CAN
- 6 x SPI
- USB2.0 HS (Host/Fast)

Display
- LCD Controller

Security (optional)
- Secure Boot, JTAG Lock, Unique ID

Timers
- 6 x 16-bit GPT
- 2 x 32-bit GPT
- 16 x PWM out
- 1 x WD1 per CPU

System
- 2x16ch DMAC
- JTAG
- Clock Generation Circuit

Package
- 324-pin LFBGA 15mm x 15mm / 0.8mm pitch
- 196-pin LFBGA 12mm x 12mm / 0.8mm pitch

Application example: Sensor Hub block diagram

Sensor Hub

40MHz Osc

USB 2.0 H/F

Serial flash

196BGA

GPIOs(LEDs,extension,...)

Eth PHY

Eth PHY

Eth PHY

IO-Link PHYs

IO-Link PHYs

Renecas Osc

RZ/N1S

32-33
RZ/N1L Group

- **R-IN engine**
  - Arm® Cortex®-M3
  - Operating frequency: 125MHz
  - HW-RTOS accelerator
  - Ethernet accelerator
- **Internal memory**
  - 6MB (ECC)
- **External memory**
  - Quad I/O SPI
  - SD10 eMMC
- **NAND flash controller**
- **Main Ethernet communication functions**
  - EtherCAT slave controller
  - Sercos® III slave controller
  - GbE Ethernet switch
- **Other communication functions**
  - UART x 8 channels
  - I²C x 2 channels
  - USB Host/Function x 1 channel, Host 1 channel
  - SPI x 6 channels (master x 4 channels, slave x 2 channels)
  - CAN x 2 channels
- **Other functions**
  - LCD controller
  - ADC: 12-bit x 8 channels x 1 unit
  - PWM timer, GPT
- **Package**
  - 196-pin: LFBGA, 12 x 12mm, 0.8mm pin pitch
  - Operating temperature: Tj = −40°C to +110°C

### RZ/N1L Group block diagram

#### System
- 2x 16ch DMAC
- JTAG
- Clock Generation Circuit

#### Timers
- 6 x 16-bit GPT
- 2 x 32-bit GPT
- 16 x PWM out
- 1 x WDT per CPU

#### Interfaces
- 8 x UART
- 2 x I²C
- 6 x SPI
- USB2.0 HS (Host/Func)

#### Memory Interface
- Quad SPI
- NAND Flash I/F
- 1 x SDIO/eMMC
- USB2.0 HS (Host/Func)

### CONNECT IT! ETHERNET RZ/N

- **CONNECT IT! ETHERNET RZ/N** is the perfect solution kit for developers new to developing with the RZ/N1.
- The kit comes with not only an evaluation board, but also a JTAG emulator and various sample software.
- **It is possible to evaluate master communication / slave communication of industrial networks.**

- **JTAG emulator**
  - IAR I-jet Lite (20-pin flat ribbon/USB cable)
- **2 USB cables**
- **Startup manuals**
- **Pin setting tool**
- **RZ/N Solution Kit DVD**
  - User's manual
  - OS (Linux, ThreadX® (Evaluation version), HW-RTOS)
  - Software PLC Codesys
  - Protocol stacks

### RZ/N Series: Solutions from Renesas Partners

Visit the webpage below for the latest information on RZ/N Series development tools, including solutions from partner companies.

https://www.renesas.com/products/microcontrollers-microprocessors/rz/softtools.html#rzn
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement of any other claims, including patents, copyrights, or other intellectual property rights of Renesas Electronics or others.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall be solely responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, distribution or other disposal of any products incorporating Renesas Electronics products, if required.

5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alterations, modifications, copying or reverse engineering.

6. Renesas Electronics products are classified accordingly in the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depend on the product quality grade, as indicated below.

<table>
<thead>
<tr>
<th>Product Quality Grade</th>
<th>Intended Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>Any applications</td>
</tr>
<tr>
<td>High Quality</td>
<td>Critical applications</td>
</tr>
</tbody>
</table>

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics’s hardware or software products, Renesas Electronics products shall not be absolutely secure against any application of the product that allows to derive key data, operating parameters, or operating conditions, including, but not limited to forward key recovery, key analysis and reverse engineering.

8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices”, “in the reliability handbook”, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for damages or losses incurred by you or third parties arising from the use of Renesas Electronics products outside of such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high-reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to reliability design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including, but not limited to redundancy, fault control and failure prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental concerns, including but not limited to the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses incurred as a result of your noncompliance with applicable laws and regulations.

11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems which manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transports the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

13. This document shall not be reproduced, republished or duplicated in any form, or in whole or in part, without prior written consent of Renesas Electronics.

14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Rev.5.0-1 October 2020)