

XO\_DPLL Monitoring for ClockMatrix FW5.2

This application note explains how to configure the XO\_DPLL input to have a pseudo input monitor.

1. Introduction

The XO\_DPLL input does not have any input monitors, specifically, a short-term or LOS monitor for loss of signal. This could be problematic if there is any signal integrity issue with the XO\_DPLL. The ClockMatrix FW5.2, however, can detect a poor XO\_DPLL signal and disqualify the input to any of the DPLLs, including the SYSDPLL.

2. GUI and Register Settings

If the XO\_DPLL monitoring feature is enabled for a DPLL, then the device will monitor the phase offset between the XO\_DPLL input and the feedback. While in LOCKED state, the XO\_DPLL input is declared valid if the phase offset is less than the phase lock threshold (lock criteria). If the lock criteria is violated, then the DPLL will go into HOLDOVER or switch to another reference if the DPLL is configured to do so.

In the example in Figure 1, the manual reference mode is selected and the TCXO/OCXO (XO\_DPLL) is selected as the input to DPLL0. The XO\_DPLL reference monitoring bit must be enabled as well.

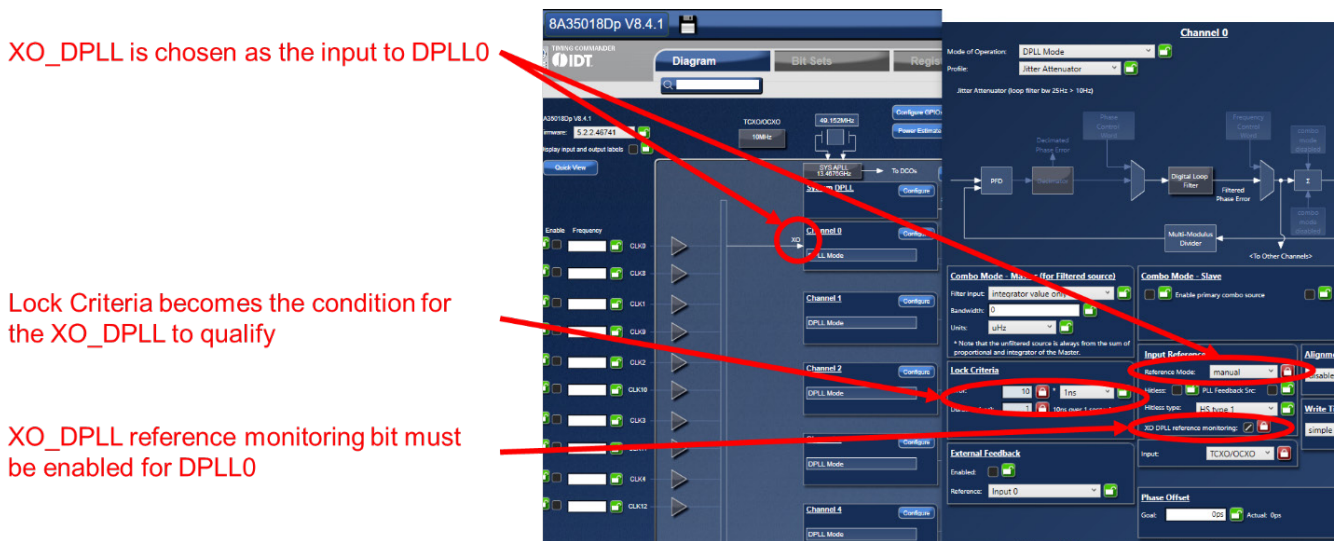


Figure 1. Configuring the GUI to Use XO\_DPLL Monitoring

Each DPLL can independently enable the XO\_DPLL reference monitoring bit as displayed in Figure 2. That allows any DPLL to use the XO\_DPLL monitoring feature, when the XO\_DPLL input is fed to a particular DPLL. The SCSR registers are named SCSR\_DPLL\_REF\_MODE\_XO\_DPLL\_MONITOR\_ENx, where x = 0, 1, 2, 3, 4, 5, 6, or 7. Also, there is SCSR\_SYS\_DPLL\_REF\_MODE\_XO\_DPLL\_MONITOR\_EN. For more information about these bits, see the 8A3xxx Family Programming Guide v5.2.

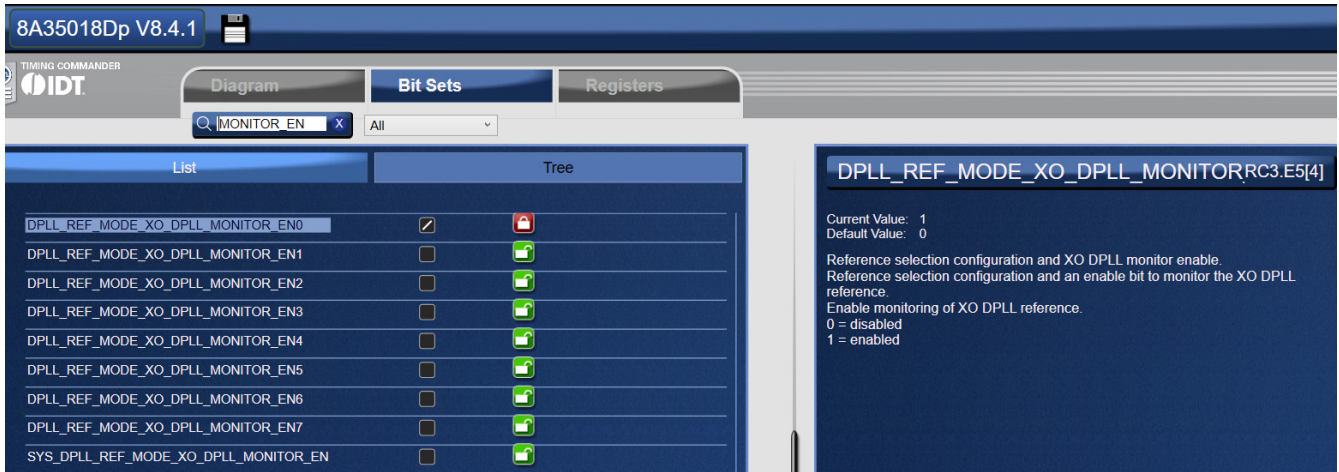


Figure 2. XO\_DPLL Monitoring Registers for Each DPLL

### 3. Revision History

Revision	Date	Description
1.00	Aug 20, 2021	Initial release.

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