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H8S/2200 Series

Watchdog Timer

Introduction

This application demonstrates watchdog timer operation of the H8S/2215. Normal operation is implemented with the setting [watchdog timer period] > [overflow period], and a power-on reset is induced by providing a low-level $\overline{\text{IRQ1}}$ signal.

Target Device

H8S/2215

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1. Specifications

1. Watchdog operations are performed using the watchdog timer function.
2. The overflow period of the timer counter (TCNT) is set to 32 μ s and TCNT is initialized at regular intervals. A low-level signal is input to the $\overline{\text{IRQ1}}$ pin using a switch to inhibit initialization of TCNT, which leads TCNT to overflow (within 32 μ s) and a power-on reset is induced.
3. Figure 1 shows an example of the switch connection to the $\overline{\text{IRQ1}}$ input pin.

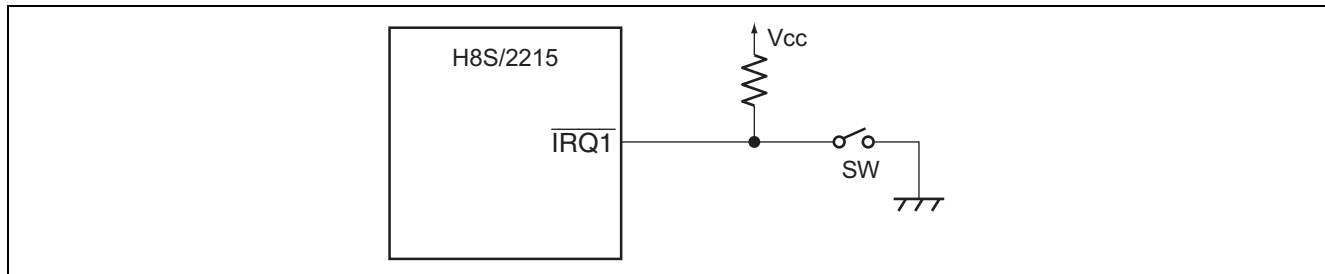


Figure 1 Example of Switch Connection to $\overline{\text{IRQ1}}$ Input Pin

2. Description of Functions

1. Figure 1 shows a block diagram of the interval timer, and the following is the description for the block diagram (this block diagram is the same as that of the watchdog timer):
 - The timer counter (TCNT) is an 8-bit up counter that can be read from or written to. TCNT is initialized to H'00 when the TME bit in the timer control/status register (TCSR) is 0.
 - The timer control/status register (TCSR) selects a clock input to TCNT, sets timer mode, etc.
 - The reset control/status register (RSTCSR) controls internal reset signal generation and selects the type of the internal reset signal. RSTCSR is initialized to H'1F by a reset signal from the RES pin. It is not initialized by an internal reset signal generated upon a WDT overflow.

To use the 8-bit timer in watchdog timer mode, set the $\overline{\text{WT/IT}}$ bit to 1 and TME bit to 1 in TCSR. This sample task is programmed so that TCNT is prevented from overflowing by rewriting the TCNT value (usually writing H'00) before it overflows. Therefore, TCNT does not overflow while the system is operating normally.

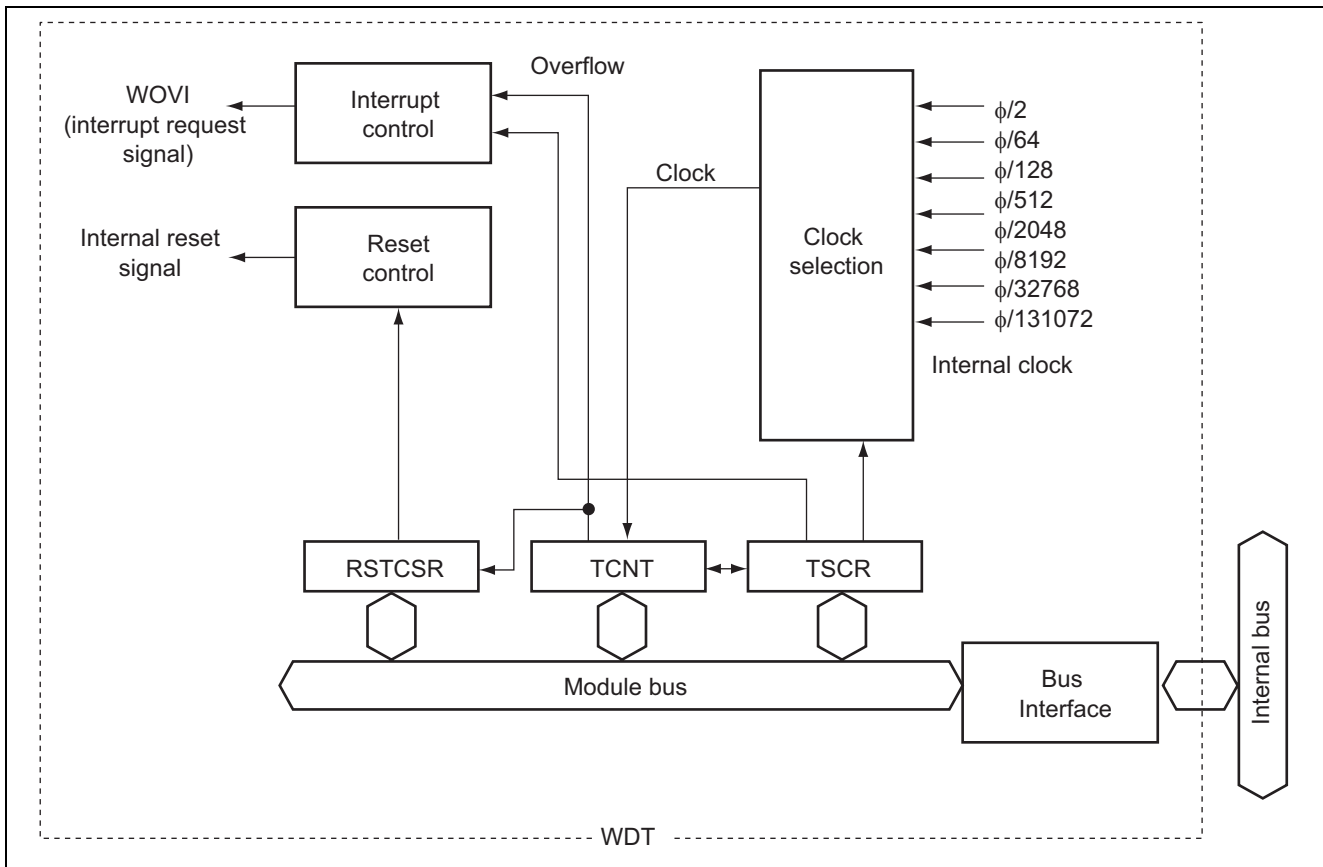


Figure 2 Block Diagram of Watchdog Timer

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCNT	8-bit up counter
TCSR	Register that selects clock input to TCNT and timer mode
RSTCSR	Register that controls the internal reset signal generated upon TCNT overflow

3. Principles of Operation

Figure 3 illustrates the operation of this sample task. Watchdog timer operation is implemented through the hardware and software processing shown in the figure.

1. System clock (ϕ)/2 is used as the input clock for TCNT ($\phi = 16$ MHz).
2. TCNT overflow period is set to $32 \mu\text{s}$ ($= (1/(16\text{MHz}/2)) \times 256$).
3. The WDT clearing cycle setting is cancelled when the $\overline{\text{IRQ1}}$ pin is driven low. An internal reset signal is then generated within $32 \mu\text{s}$ on DT overflow, and a power-on reset of the H8S/2215 is induced.

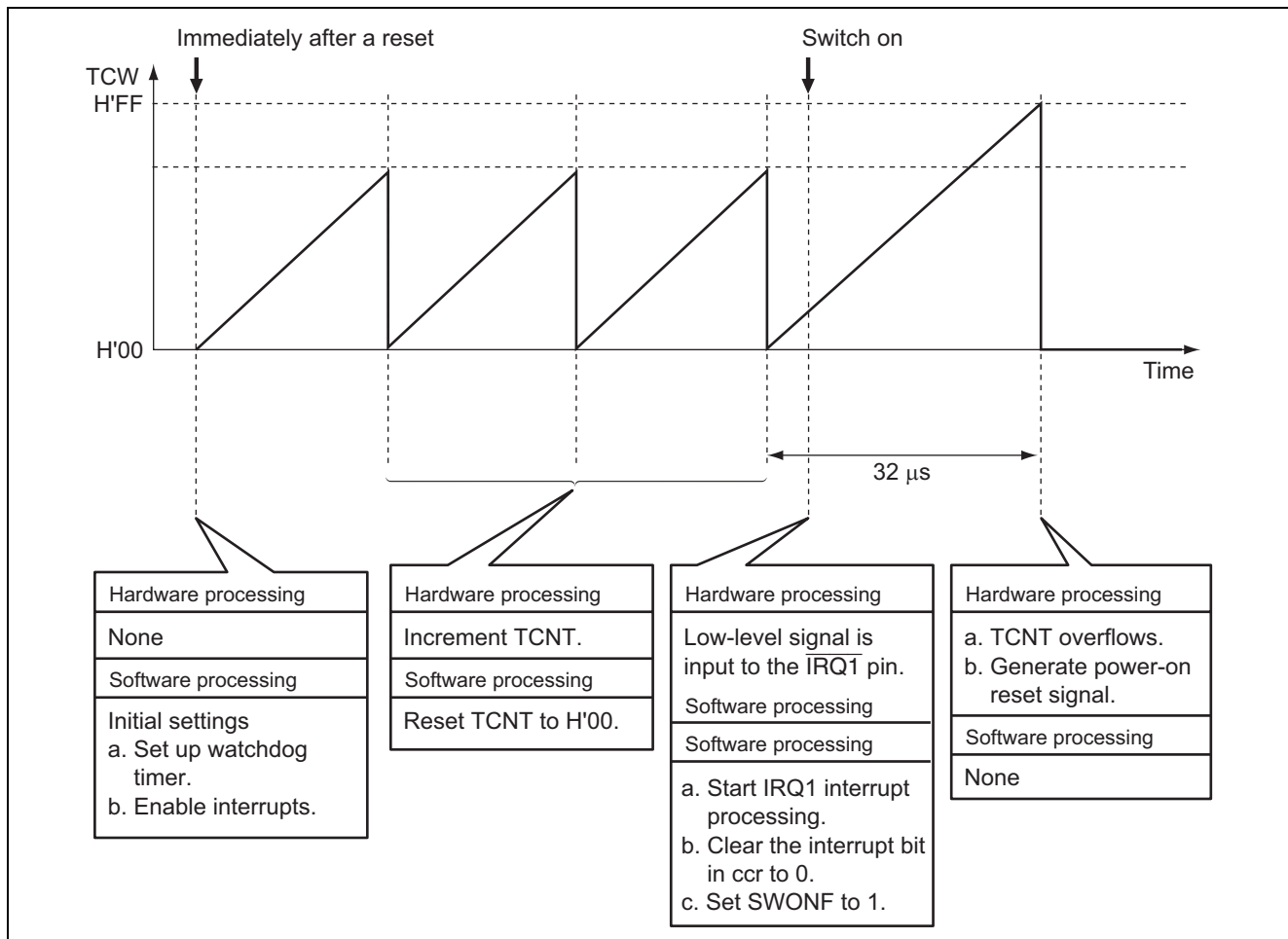


Figure 3 Operation of Watchdog Timer

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Makes settings for watchdog timer function, enables interrupts, and determines whether the switch connected to the $\overline{\text{IRQ1}}$ pin has been turned on.
Switch-on	Irq1int	IRQ1 interrupt processing routine that sets SWONF to 1.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

Table 3 Description of Internal Registers

Register	Function	Address	Setting
TCNT	Timer Counter Readable/writable 8-bit up counter	For writing: H'FFFF74 For reading: H'FFFF75	H'00 when TME in TCSR is 0
TCSR	OVF Timer Control/Status Register (Overflow Flag) Only "0" can be written for flag clearing. When OVF = 0, no overflow occurs on TCNT. When OVF = 1, an overflow occurs on TCNT.	H'FFFF74 Bit 7	0
	WT/ $\overline{\text{IT}}$ Timer Control/Status Register (Timer Mode Select) When WT/ $\overline{\text{IT}}$ = 0, interval mode is selected. When WT/ $\overline{\text{IT}}$ = 1, watchdog timer mode is selected.	H'FFFF74 Bit 6	1
	TME Timer Control/Status Register (Timer Enable) When TME = 0, counting by TCNT is stopped. When TME = 1, counting by TCNT is started.	H'FFFF74 Bit 5	0
—	Timer Control/Status Register (Reserved) These bits are always read as 1 and cannot be modified.	H'FFFF74 Bit 4 Bit 3	1, 1
CKS2 to CKS0	Timer Control/Status Register (Clock Select 2 to 0) Eight values from 000 to 111 can be set for CKS2 to CKS0. In this sample task, these bits are set to 000 to cause an overflow at the cycle of $\phi/2$ (32 μs). (ϕ = 16 MHz)	H'FFFF74 Bit 2 to bit 0	CKS2 = 0 CKS1 = 0 CKS0 = 0

Register	Function	Address	Setting
RSTCSR WOVF	Reset Control/Status Register (Watchdog Timer Overflow Flag) WOVF = 0 indicates that TCNT has not overflowed (or TCNT is cleared). WOVF = 1 indicates that TCNT has overflowed (H'FF to H'00).	For writing: H'FFFF76 For reading: H'FFFF77 Bit 7	0
RSTE	Reset Control/Status Register (Reset Enable) When RSTE = 0, internal reset is not induced but only TCNT and TCSR are reset when TCNT has overflowed. When RSTE = 1, internal reset is induced when TCNT has overflowed.	For writing: H'FFFF76 For reading: H'FFFF77 Bit 6	1
RSTS	Reset Control/Status Register (Reset Select) When RSTS = 0, a power-on reset is selected. When RSTS = 1, a manual reset is selected.	Same addresses as above. Bit 5	0
—	Reset Control/Status Register (Reserved) These bits are always read as 1 and cannot be modified.	Same addresses as above. Bit 4 to bit 0	1,1,1,1,1

4.4 RAM Usage

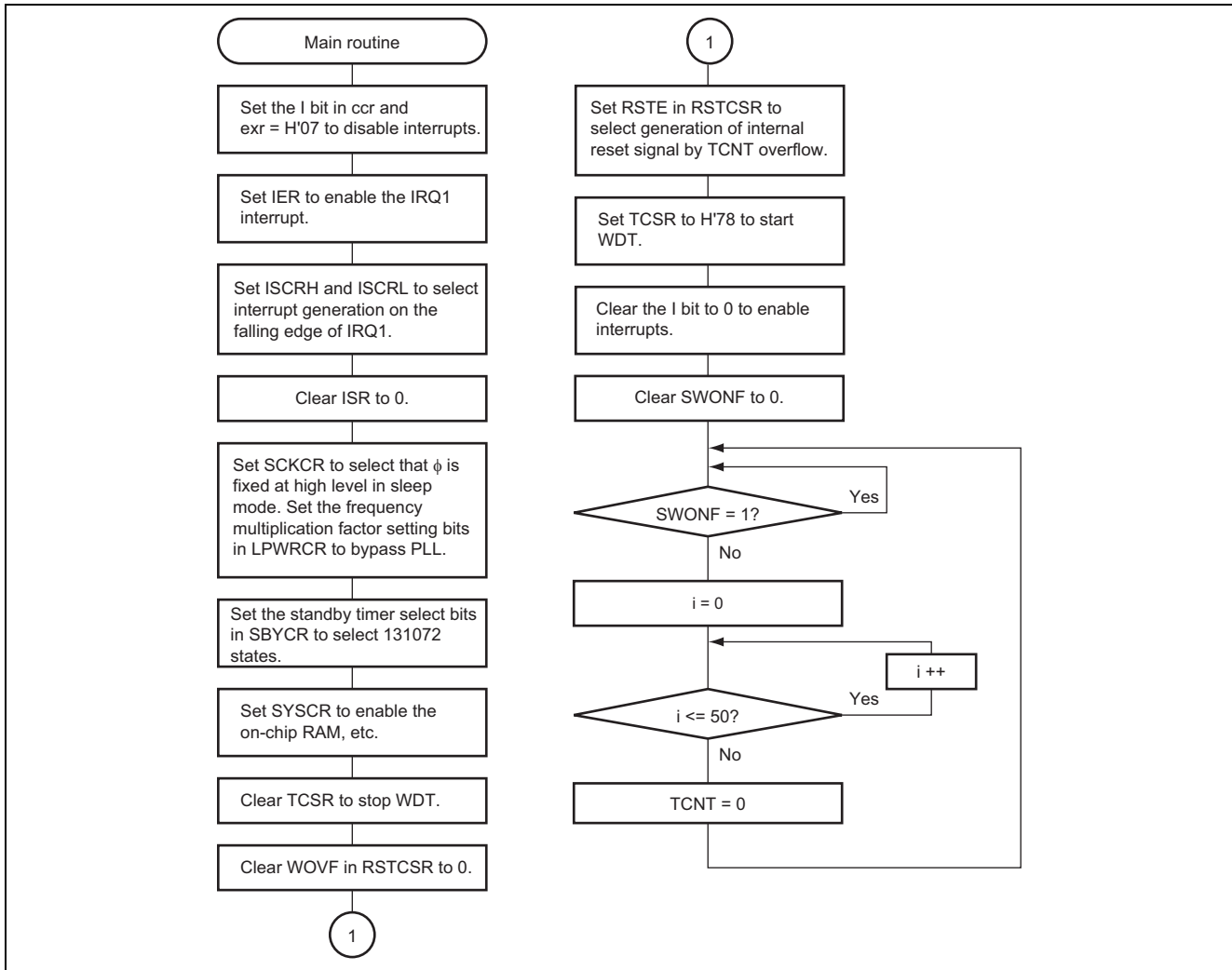
Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

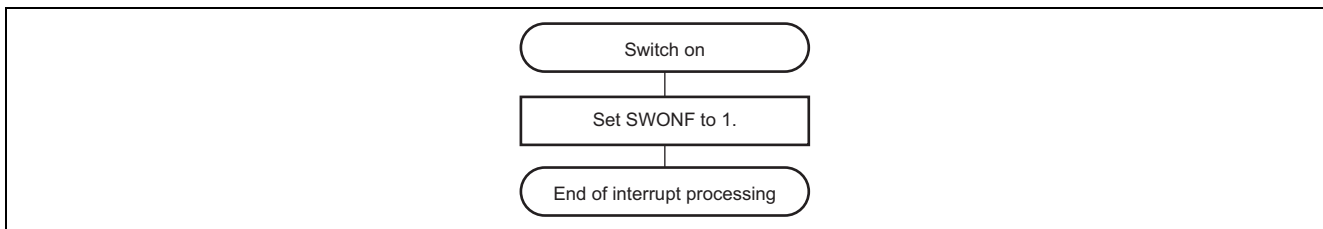
Label	Function	Address	Used in
SWONF	Flag used to determine the on/off-state of the switch input.	H'FFB000	Main routine, Switch-on

5. Flowchart

1. Main routine



2. IRQ1 interrupt processing routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued
2.00	May.23.06	All page	Error correction

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