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M32C/84, 85, 86, 87, 88 Group

Watchdog Timer

1. Abstract

The watchdog timer function allows users to detect when a program is out of control. Users can select whether to generate a watchdog timer interrupt or reset as an operation when the watchdog timer count value underflows.

For the watchdog timer count source, users can select the CPU clock or on-chip oscillator clock.

When the CPU clock is used for the count source, the watchdog timer periods are as follows:

When the main clock, PLL clock, or on-chip oscillator clock is used as the CPU clock:

$$\text{Watchdog timer period} = \frac{\text{Division ratio by prescaler (16 or 128)} \times \text{Watchdog timer count value (32768)}}{\text{CPU clock}}$$

When the sub-clock is selected as the CPU clock:

$$\text{Watchdog timer period} = \frac{\text{Division ratio by prescaler (2)} \times \text{Watchdog timer count value (32768)}}{\text{CPU clock}}$$

When the on-chip oscillator clock is selected for the watchdog timer count source, the watchdog timer period is as follows:

$$\text{Watchdog timer period} = \frac{\text{Watchdog timer count value (32768)}}{\text{On-chip oscillator clock}}$$

Table 1.1 lists a Watchdog Timer Period Example.

Table 1.1 Watchdog Timer Period Example

When XIN = 8 MHz, XCIN = 32.768 kHz, PLL clock = 32 MHz (main clock multiplied-by-4)

Setting Value							Watchdog Timer Count Source	Watchdog Timer Period
CM07	CM17	CM21	PM22	PM24	WDC7	MCD		
0	0	0	0	0	0	12h	Divided-by-16 CPU clock (main clock)	Approx. 65.5 ms
0	0	0	0	0	1	12h	Divided-by-128 CPU clock (main clock)	Approx. 524.3 ms
0	0	0	0	1	0	(NOTE)	Divided-by-16 CPU clock (main clock)	Approx. 65.5 ms
0	0	0	0	1	1	(NOTE)	Divided-by-128 CPU clock (main clock direct mode)	Approx. 524.3 ms
0	1	0	0	0	0	12h	Divided-by-16 CPU clock (PLL clock)	Approx. 16.4 ms
0	1	0	0	0	1	12h	Divided-by-128 CPU clock (PLL clock)	Approx. 131.1 ms
0	0	1	0	0	0	12h	Divided-by-16 CPU clock (on-chip oscillator)	Approx. 524.3 ms
0	0	1	0	0	1	12h	Divided-by-128 CPU clock (on-chip oscillator)	Approx. 4.2 ms
1	0	0	0	0	-	(NOTE)	Divided-by-2 CPU clock (sub clock)	2s
-	-	-	1	-	-	(NOTE)	On-chip oscillator	Approx. 32.8 ms

-: Can be set to either 0 or 1.

CM07: Bit in the CM0 register, CM17: Bit in the CM1 register, CM21: Bit in the CM2 register

PM22: Bit in the PM2 register, WDC7: Bit in the WDC register

NOTE:

1. The MCB register value does not affect the watchdog timer period.

2. Introduction

The application example described in this document is applied to the following MCUs and parameter(s):

MCUs: M32C/84 Group
M32C/85 Group
M32C/86 Group
M32C/87 Group
M32C/88 Group

This program can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above MCUs. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

This section describes how to generate the watchdog timer interrupt or reset using the CPU clock for the watchdog timer counter source.

3.1 Example Description

- (1) When the WDTS register is written, the watchdog timer is initialized to 7FFFh and starts counting.
- (2) When the WDTS register is rewritten during a count operation, the watchdog timer is initialized to 7FFFh and continues counting.
- (3) The watchdog timer holds its value and stops when in wait mode, stop mode or in hold. After exiting from wait mode or stop mode, the watchdog timer restarts counting (see NOTE below).
- (4) To use the watchdog timer interrupt:
When the watchdog timer underflows, the watchdog timer is initialized to 7FFFh and continues counting. At the same time, the watchdog timer interrupt is generated.
To use the watchdog timer reset:
When the watchdog timer underflows, the pins, CPU and SFR are initialized and the MCU starts the program beginning with the address indicated by the reset vector.

NOTE:

1. When the PM22 bit in the PM2 register is set to 1 (on-chip oscillator selected for the watchdog timer count source), the watchdog timer does not stop even when in wait mode or in a hold state.

Figure 1 shows the Watchdog Timer Operation.

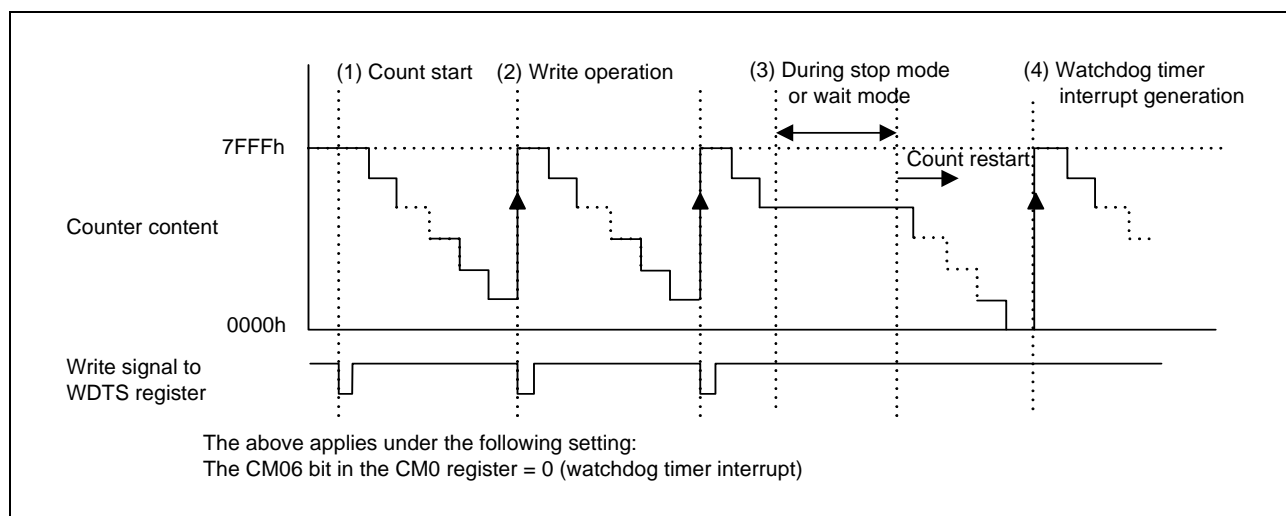


Figure 1 Watchdog Timer Operation

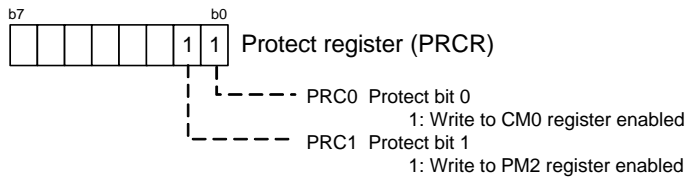
3.2 Setup

This section shows the setup sequence and values to perform the application example described in

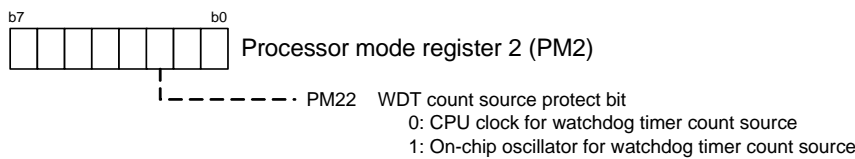
3.1 Example Description.

Refer to the each MCUs Hardware Manual for details of individual registers.

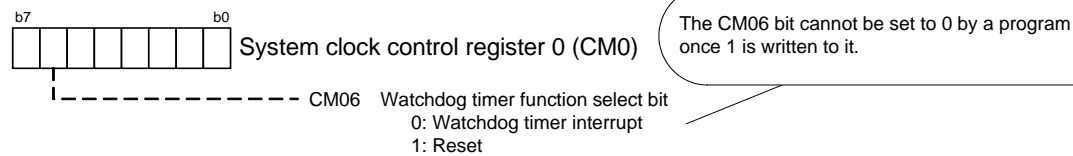
(1) Set the protect register



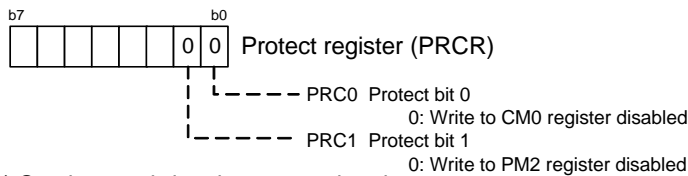
(2) Set processor mode register 2



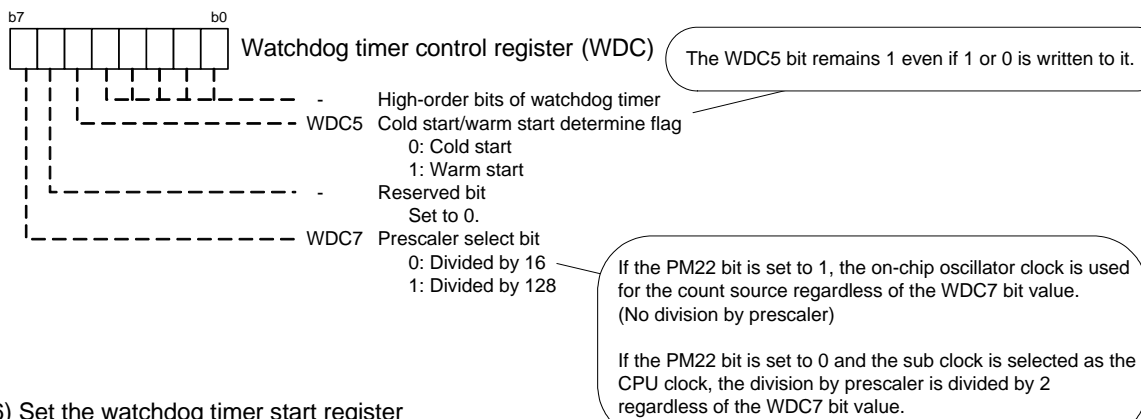
(3) Set system clock control register 0



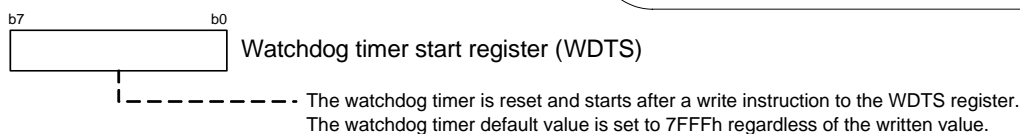
(4) Set the protect register



(5) Set the watchdog timer control register



(6) Set the watchdog timer start register



4. Sample Programming Code

4.1 To Use Watchdog Timer Interrupt

Increment the P10 port indication by writing to the WDTS register. When the P10 port output is set to 40h, finish writing to the WDTS register to stop updating the P10 port indication.

If a watchdog timer underflow occurs, increment the P10 port indication in the watchdog timer interrupt handler by writing to the WDTS register. When the P10 port output is set to 00h, stop updating the P10 port indication.

```

/*****
 *
 * FILE NAME : interrupt_src.c
 * CPU      : M32C/84 Group
 * Function  : Operation of Watchdog Timer
 *
 * Version   : 1.00 (2006-05-18) Initial
 *
 * Copyright (C)2006, Renesas Technology Corp.
 *
 *****/
/*****
 * include file
 *****/
#include "sfr32c84.h"

unsigned int i;
/*****
 * main
 *****/
void main(void) {

    p10 = 0x00;
    pd10 = 0xff;

    ta0mr = 0x40;          /* Select timer mode
                           Gate function select bit (00: Gate function not available)
                           Count source (01:f8)
                           */

    ta0 = 4000-1;         /* Set counter value (1 msec @ 32 MHz, f8)
                           */

    ta0ic = 0x00;        /* Set interrupt priority levels in timer A0
                           */

    ta0s = 1;           /* TimerA0 count start
                           */

    wdc = 0x00;         /* Prescaler Select Bit (0: Divided by 16)
                           (WDT cycle approx. 16.384 ms Xin = @32 MHz)
                           */

    i = 0;
    prcr = 0x03;
    pm2 = 0x00;         /* WDT Count Source Protect Bit (0: Selects CPU clock as count source of the
                           watchdog timer)
                           */

    cm0 = 0x08;        /* Watchdog Timer Function Select Bit (0: Watchdog timer interrupt)
                           */

    prcr = 0x00;

    wdts = 0xFF;       /* The watchdog timer is initialized and starts counting
                           with a write instruction to this register.
                           The watchdog timer value is always initialized to "7FFFh"
                           regardless of the value written.
                           */

    while (1) {
        while(ir_ta0ic == 0){};
        ta0ic = 0x00;
        i++;
        if(i == 500){
            i = 0;
            p10++;
        }
        if(p10 >= 64){
            p10 = 64;
        }
    }
}

```

```

        }else{
            wdts = 0xFF;          /* Set watchdog timer start register
                                */
        }
    }
}

#pragma interrupt _watchdog_int
void watchdog_int(){
    wdts = 1;
    while(1){
        while(ir_ta0ic == 0){};
        ta0ic = 0x00;
        i++;

        wdts = 0xFF;          /* Set watchdog timer start register
                                */

        if(i == 500){
            i = 0;
            if(p10 != 0){
                p10--;
            }
        }
    }
}

```

4.2 To Reset on Watchdog Timer Underflow

Increment the P10 port indication by writing to the WDTS register. When the P10 port output is set to 40h, finish writing to the WDTS register to stop updating the P10 port indication. If a watchdog timer underflow occurs, the MCU is reset.

```

/*****
 *
 * FILE NAME : reset_src.c
 * CPU       : M32C/84 Group
 * Function  : Operation of Watchdog Timer
 *
 * Version   : 1.00 (2006-05-18) Initial
 *
 * Copyright (C)2006, Renesas Technology Corp.
 *
 *****/
/*****
 * include file
 *****/
#include "sfr32c84.h"

unsigned int i;
/*****
 * main
 *****/
void main(void) {

    p10 = 0x00;
    pd10 = 0xff;

    ta0mr = 0x40;          /* Select timer mode
                           Gate function select bit (00: Gate function not available)
                           Count source (01:f8)
                           */

    ta0 = 4000-1;         /* Set counter value (1 ms @ 32 MHz, f8)
                           */

    ta0ic = 0x00;         /* Set interrupt priority levels in timer A0
                           */

    ta0s = 1;             /* TimerA0 count start
                           */

    wdc = 0xFF;           /* Prescaler Select Bit (0: Divided by 16)
                           (WDT cycle approx. 16.384ms Xin = @ 32 MHz)
                           */

    i = 0;
    prcr = 0x03;
    pm2 = 0x00;          /* WDT Count Source Protect Bit (0: Selects CPU clock as count source of the
                           watchdog timer)
    
```

```

        */
cm0 = 0x48;          /* Watchdog Timer Function Select Bit (1: Reset)
                    */
prcr = 0x00;

wdts = 0x00;        /* The watchdog timer is initialized and starts counting
                    with a write instruction to this register.
                    The watchdog timer value is always initialized to "7FFFh"
                    regardless of the value written.
                    */

while (1) {
    while(ir_ta0ic == 0){};
    ta0ic = 0x00;
    i++;
    if(i == 500){
        i = 0;
        p10++;
    }
    if(p10 >= 64){
        p10 = 64;
    }else{
        wdts = 0xFF;          /* Set watchdog timer start register
                              */
    }
}

}

#pragma interrupt _watchdog_int
void watchdog_int(){
    wdts = 1;
    while(1){
        while(ir_ta0ic == 0){};
        ta0ic = 0x00;
        i++;

        wdts = 0xFF;        /* Set watchdog timer start register
                              */

        if(i == 500){
            i = 0;
            if(p10 != 0){
                p10--;
            }
        }
    }
}
}

```

5. Reference Documents

Hardware Manuals

M32C/84 Group Hardware Manual

M32C/85 Group Hardware Manual

M32C/86 Group Hardware Manual

M32C/87 Group Hardware Manual

M32C/88 Group Hardware Manual

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REVISION HISTORY	M32C/84, 85, 86, 87, 88 Group Watchdog Timer
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