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H8SX Family

Watchdog Timer

Introduction

Watchdog operation is performed using the watchdog timer function.

Target Device

H8SX/1582F

Contents

1. Specifications

- Watchdog operation is performed using the watchdog timer function.
- The overflow cycle of the timer counter TCNT is set at 24 µs, and the TCNT is initialized within 24 µs. When a low trigger is input to the $\overline{\text{IRQ0}}$ pin, the TCNT overflows without being initialized and a power-on reset occurs.
- Figure 1 shows an example of connecting a switch to the $\overline{\text{IRQ0}}$ pin.

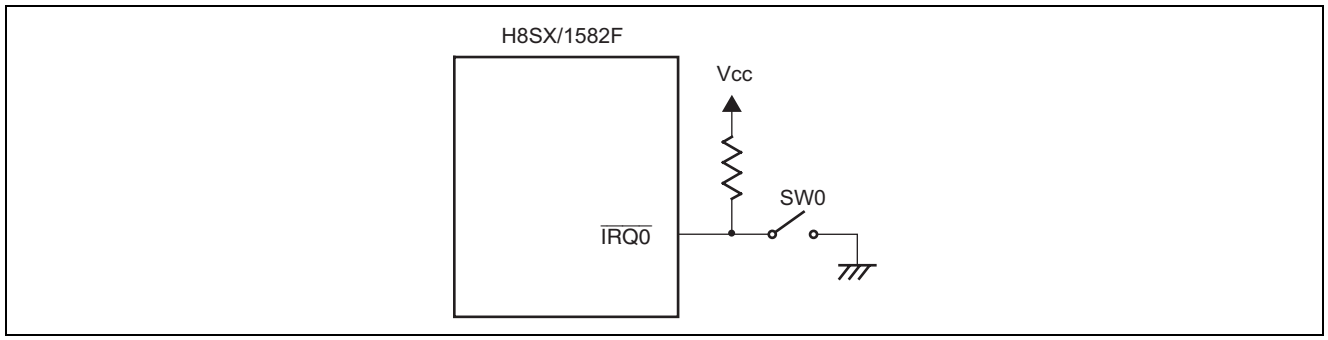


Figure 1 Block Diagram of Connecting a Switch

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents	
Operating frequency	Input clock:	5 MHz
	System clock (Iϕ):	40 MHz
	Peripheral module clock (Pϕ):	20 MHz
	External bus clock (Bϕ):	20 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
On-board programming mode	User boot mode	
Development tool	High-performance Embedded Workshop Version 4.00.02	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Version 6.01.00 (from Renesas Technology Corp.)	
Compile option	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3, -speed = (register, shift, struct, expression)	

Table 2 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF9000	B	Uninitialized data area (RAM area)

3. Description of Modules Used

Figure 2 shows a block diagram of the watchdog timer (WDT). The block diagram of the WDT is described below.

- Timer counter (TCNT)
  TCNT is an 8-bit readable/writable up-counter. When the TME bit in the timer control/status register (TCSR) is 0, TCNT is initialized to H'00.
- Timer control/status register (TCSR)
  TCSR selects the clock to be input to TCNT and the mode.
- Reset control/status register (RSTCSR)
  RSTCSR controls generation of an internal reset signal caused by a TCNT overflow and selects the internal reset signal type. RSTCSR is initialized to H'1F by a reset signal from the $\overline{\text{RES}}$ pin. RSTCSR is not initialized by an internal reset signal caused by an overflow of the WDT.

To use the watchdog timer in watchdog timer mode, set both the WT/$\overline{\text{IT}}$ bit and TME bit in TCSR to 1. The value of TCNT is rewritten before TCNT overflows, and it is made not to overflow. The sample program rewrites the value of TCNT with H'10. This prevents TCNT from overflowing while the system is operating normally.

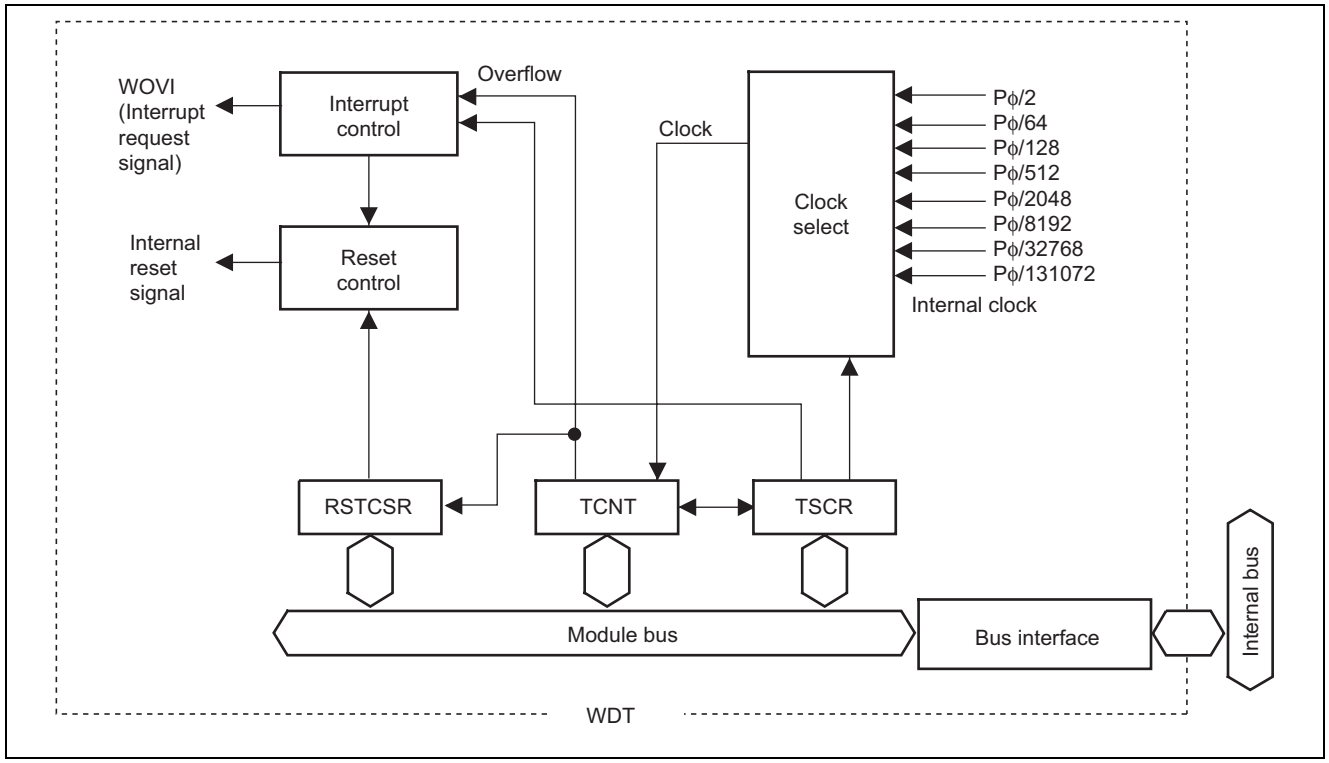


Figure 2 Block Diagram of Watchdog Timer

4. Description of Operation

Figure 3 illustrates watchdog operation by means of the watchdog timer function. The hardware processing and software processing are shown in table 3 for describing figure 3.

(1) The clock input to TCNT is Pϕ/2 (Pϕ: 20 MHz).
(2) The TCNT overflow cycle is 24 µs. The formula for calculating the overflow cycle is shown below.

$$\text{Overflow period} = \frac{1}{P\phi/2} \times (256 - 16) = \frac{1}{20\ \text{MHz}/2} \times (256\ -16) = 24\ \mu\text{s}$$

(3) TCNT is not cleared because of an IRQ0 interrupt, and an internal reset occurs after 24 µs.

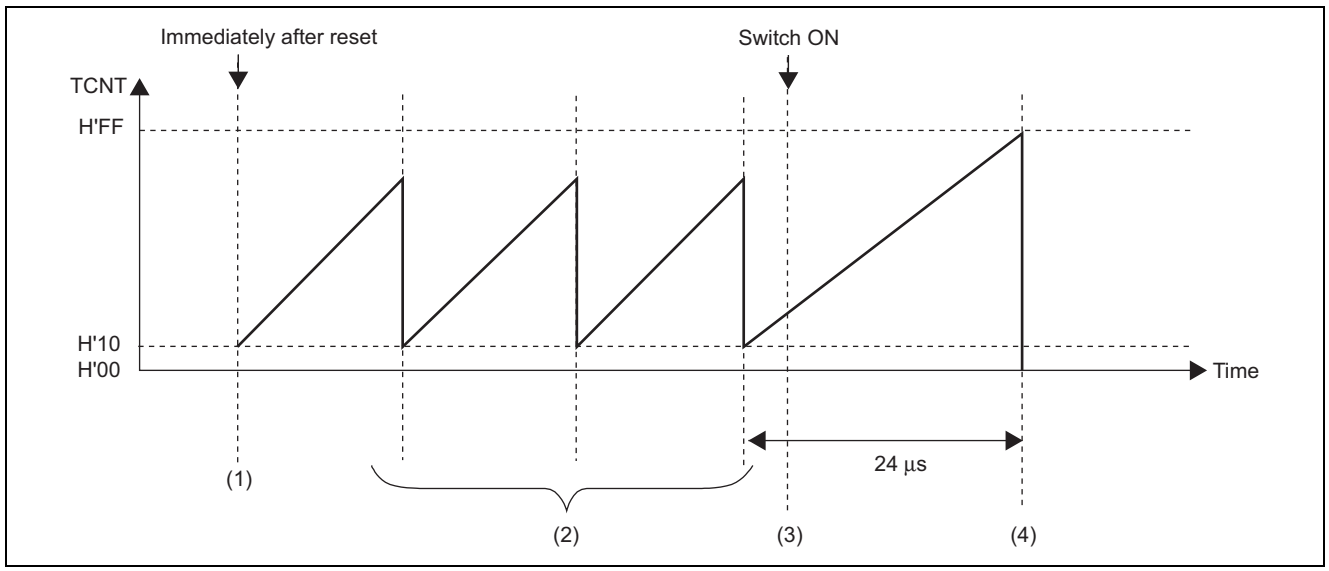


Figure 3 Watchdog Operation by Watchdog Timer Function

Table 3 Hardware and Software Processing

	Hardware Processing	Software Processing
(1)	None	Initial settings • Set up the watchdog timer. • Enable the IRQ0 interrupt.
(2)	(a) Increment TCNT.	(a) Set TCNT to H'10.
(3)	(a) Input a low level to the $\overline{\text{IRQ0}}$ pin.	(a) Start IRQ0 interrupt processing.
(4)	(a) TCNT overflows. (b) Generate an internal reset signal.	None

5. Description of Software

5.1 List of Functions

The functions of this sample task are listed in table 4.

Table 4 List of Functions

Function Name	Functions
init	Initialization routine Cancels module stop mode, sets the clock, and calls the main function.
main	Main routine Sets the watchdog timer function, enables interrupts, and checks whether an IRQ0 interrupt has occurred.
irq0_int	IRQ0 interrupt processing routine Sets sw_buf to 1.

5.2 RAM Usage

RAM usage in this sample task is shown in table 5.

Table 5 RAM Usage

Label Name	Description	Memory Size	Used In
sw_buf	IRQ0 interrupt occurrence flag 0: IRQ0 interrupt has not occurred 1: IRQ0 interrupt has occurred	1 byte	Main irq0_int

5.3 Description of Functions

5.3.1 init Function

(1) Functional overview

Initialization routine which cancels module stop mode, makes clock settings, and calls the main function.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- System clock control register (SCKCR) Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Function
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the system clock frequency. The CPU, DMAC,
8	ICK0	0	R/W	and DTC modules are driven by the system clock.
				000: Input clock × 8
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 4
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	1	R/W	001: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC are the registers that control module stop mode. Setting the bits in these registers places the corresponding modules in module stop mode, and clearing the bits cancels module stop mode.

- Module stop control register A (MSTPCRA) Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Function
15	ACSE	0	R/W	All-module-clock-stop mode enable Enables or disables transition to all-module-clock-stop mode. If this bit is set to 1, all-module-clock-stop mode is entered when the SLEEP instruction is executed by the CPU while all the modules under control of the MSTPCR registers are placed in module stop mode. In all-module-clock-stop mode, even the bus controller and I/O ports are stopped to reduce the supply current. 0: Disables transition to all-module-clock-stop mode. 1: Enables transition to all-module-clock-stop mode.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
4	MSTPA4	1	R/W	A/D converter (unit 1)
3	MSTPA3	1	R/W	A/D converter (unit 0)
1	MSTPA1	1	R/W	16-bit timer pulse unit (TPU channels 11 to 6)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

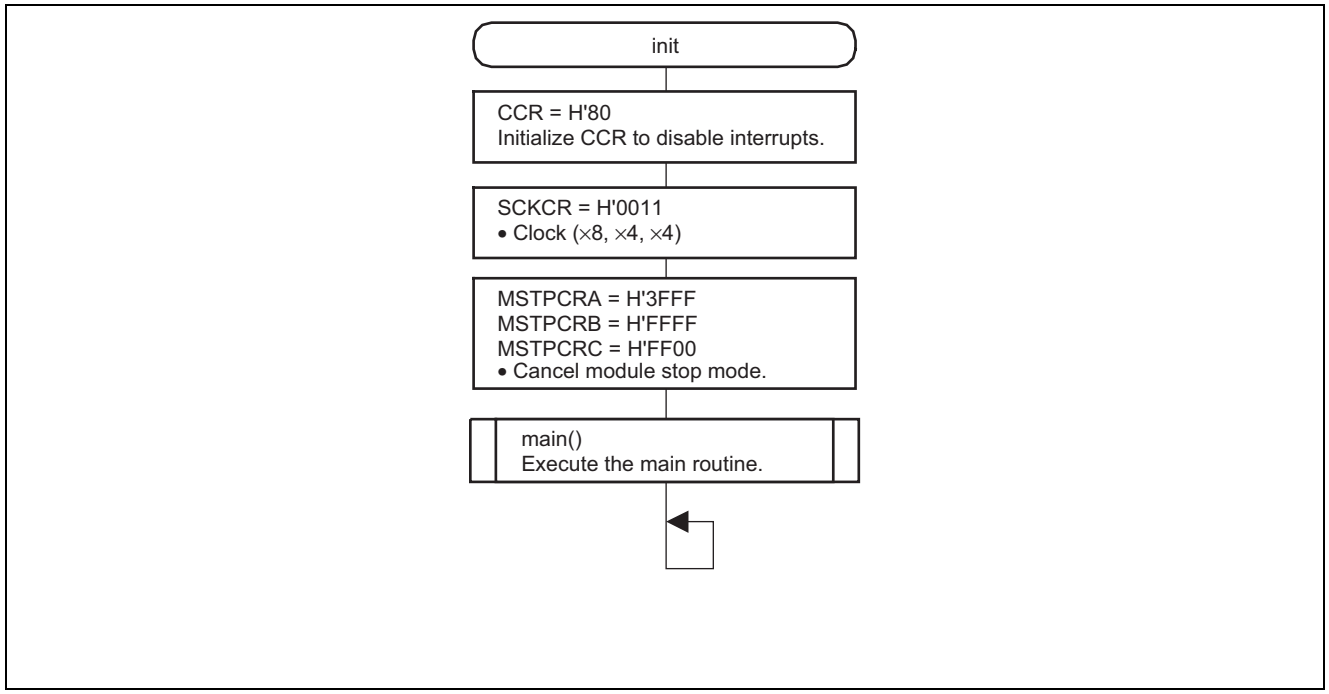
- Module stop control register B (MSTPCRB) Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Function
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communication interface_4 (SCI_4)
11	MSTPB11	1	R/W	Serial communication interface_3 (SCI_3)

- Module stop control register C (MSTPCRC) Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Function
10	MSTPC10	1	R/W	Synchronous serial communication unit 2 (SSU_2)
9	MSTPC9	1	R/W	Synchronous serial communication unit 1 (SSU_1)
8	MSTPC8	1	R/W	Synchronous serial communication unit 0 (SSU_0)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF9000 to H'FFBFFF)
0	MSTPC0	0	R/W	Always write the same value to the MSTPC1 and MSTPC0 bits.

(5) Flowchart



5.3.2 main Function

(1) Functional overview

Main routine which sets the watchdog timer function, enables an IRQ0 interrupt, and checks whether the switch connected to the $\overline{\text{IRQ0}}$ pin is ON.

(2) Argument

None

(3) Return value

None

(4) Description of internal registers

The internal registers used in this sample task are described below. The setting values shown in these tables are the values used in this sample task and differ from their initial values.

- Port 1 input buffer control register (P1ICR) Address: H'FFFB90

Bit	Bit Name	Setting	R/W	Function
0	P10ICR	1	R/W	0: Input buffer of pin P10 is disabled 1: Input buffer of pin P10 is enabled

- IRQ sense control register L (ISCRL) Address: H'FFFD6A

Bit	Bit Name	Setting	R/W	Function
1	IRQ0SR	0	R/W	IRQ0 Sense Control Rise
0	IRQ0SF	1	R/W	IRQ0 Sense Control Fall 01: Interrupt request is generated on the falling edge of the $\overline{\text{IRQ0}}$ input

- IRQ enable register (IER) Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	1	R/W	IRQ0 Enable 0: IRQ0 interrupt request is disabled 1: IRQ0 interrupt request is enabled

- Timer control/status register (TCSR) Address: H'FFFFA4 (when read)

Bit	Bit Name	Setting	R/W	Function
6	WT/$\overline{\text{IT}}$	1	R/W	Timer Mode Select 0: Used in interval timer mode 1: Used in watchdog timer mode
5	TME	1	R/W	Timer Enable 0: TCNT stops counting and is initialized to H'00 1: TCNT starts counting
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	These bits select the clock to be input to TCNT.
0	CKS0	0	R/W	000: Clock of Pϕ/2 When Pϕ = 20 MHz, overflow cycle is 25.6 μs

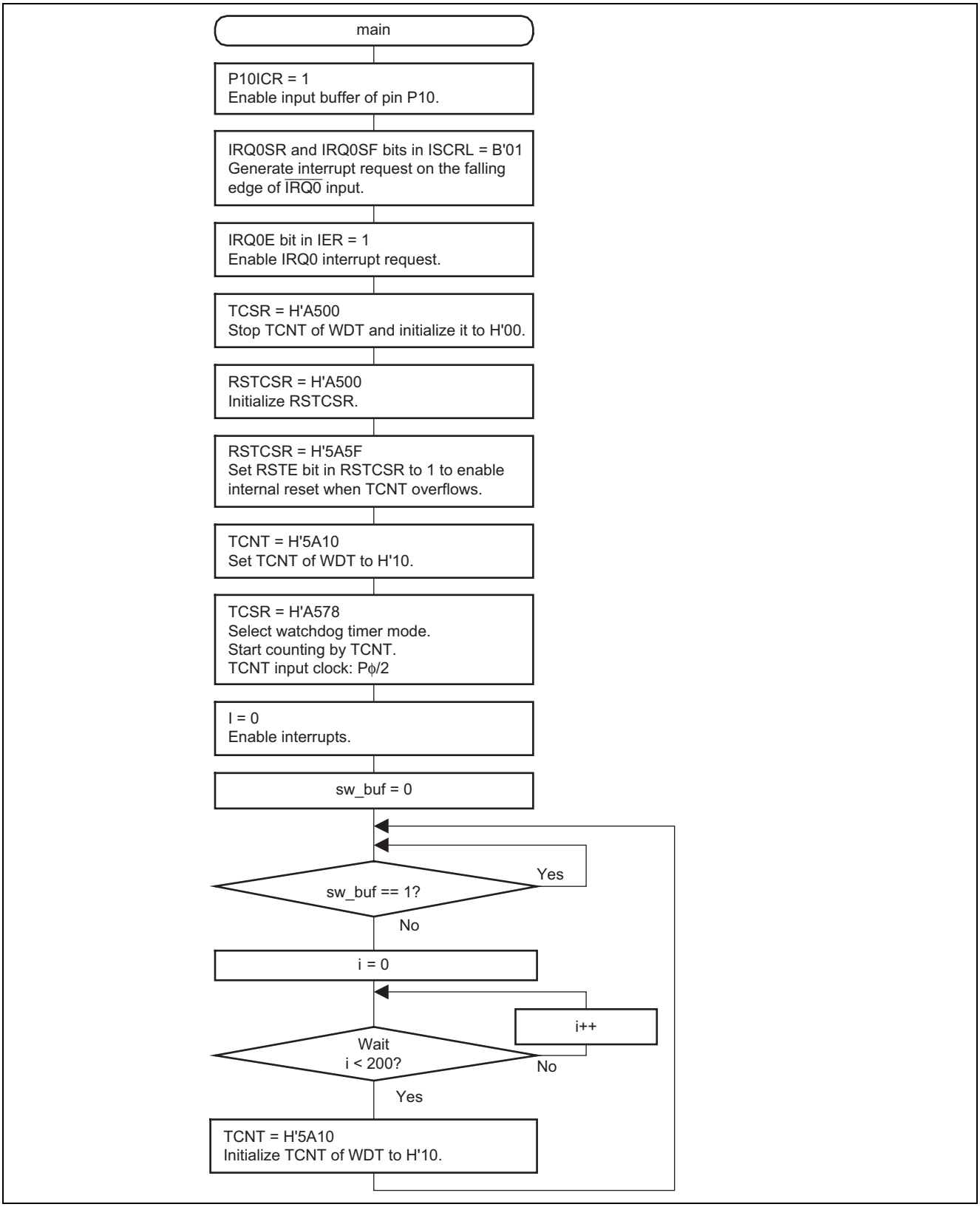
- Reset control/status register (RSTCSR) Address: H'FFFFA7 (when read)

Bit	Bit Name	Setting	R/W	Function
7	WOVF	0	R/(W)*	Watchdog Timer Overflow Flag This flag is set when TCNT overflows in watchdog timer mode. [Setting condition] When TCNT overflows (H'FF → H'00) in watchdog timer mode [Clearing condition] When 0 is written to WOVF after WOVF = 1 is read
6	RSTE	0	R/W	Reset Enable Selects whether to internally reset the LSI when TCNT overflows in watchdog timer mode. 0: Internal reset does not occur even though TCNT overflows 1: Internal reset occurs when TCNT overflows

Note: * Only 0 can be written to clear the flag.

- Timer counter (TCNT) Address: H'FFFFA5 (when read)
  8-bit readable/writable up-counter
  Setting: H'10

(5) Flowchart


main
P10ICR = 1
Enable input buffer of pin P10.
IRQ0SR and IRQ0SF bits in ISCRL = B'01
Generate interrupt request on the falling edge of IRQ0 input.
IRQ0E bit in IER = 1
Enable IRQ0 interrupt request.
TCSR = H'A500
Stop TCNT of WDT and initialize it to H'00.
RSTCSR = H'A500
Initialize RSTCSR.
RSTCSR = H'5A5F
Set RSTE bit in RSTCSR to 1 to enable internal reset when TCNT overflows.
TCNT = H'5A10
Set TCNT of WDT to H'10.
TCSR = H'A578
Select watchdog timer mode.
Start counting by TCNT.
TCNT input clock: Pϕ/2
I = 0
Enable interrupts.
sw_buf = 0
sw_buf == 1?
Yes
No
i = 0
i++
Wait
i < 200?
No
Yes
TCNT = H'5A10
Initialize TCNT of WDT to H'10.

5.3.3 irq0_int Function

(1) Functional overview

IRQ0 interrupt processing routine which sets SWONF to 1.

(2) Argument

None

(3) Return value

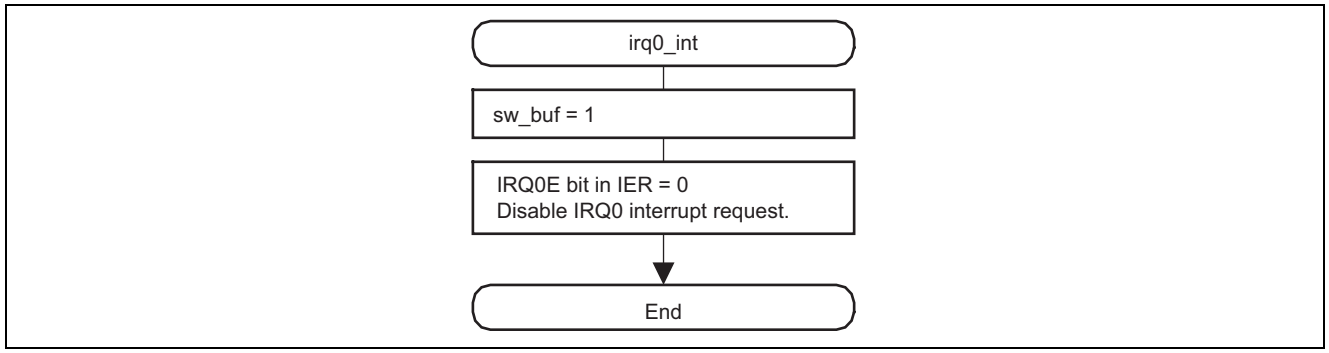
None

(4) Description of internal register

- IRQ enable register (IER) Address: H'FFFF34

Bit	Bit Name	Setting	R/W	Function
0	IRQ0E	0	R/W	IRQ0 Enable 0: IRQ0 interrupt request is disabled 1: IRQ0 interrupt request is enabled

(5) Flowchart



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		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Mar.10.06	—	First edition issued

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