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M32C/84 Group

Wait Mode Set-Up

1. Abstract

Settings and operation for entering wait mode are described here. Figure 1 shows the set-up procedure.
In the reference program,wait mode is entered when using the CPU clock with 32MHz(PLL clock multiply-by-8, divided-by-2) while the CM02 bit in the CM0 register is set to “0”(peripheral function clock dose not stop in wait mode) and exited when using the INT0 interrupt for a return factor from wait mode.

2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user’s manual. When using the functions shown in this application note, evaluate them carefully for an operation

3. Set-up

- Initial Setting

(1) Set each interrupt priority level after setting the exit priority level, required to exit wait mode,controlled by the RLVL2 to RLVL0 bits in the RLVL register, to ”7”

- Before Entering Wait Mode

(2) Set the I flag to “0”
(3) Set the interrupt priority level of the interrupt being used to exit wait mode
(4) Set the interrupt priority levels of the interrupts, not being used to exit wait mode, to “0”
(5) Set IPL in the FLG register. Then set the exit priority level to the same level as IPL
Interrupt priority level of the interrupt used to exit wait mode > IPL = the exit priority level
(6) Set the PRC0 bit in the PRCR register to “1”
(7) If the CPU clock source is the PLL clock, set the CM17 bit in the CM1 register to “0” (main clock) and PLC07 bit in the PLC0 register to “0” (PLL off)(Note1)
(8) Set the I flag to “1”
(9) Execute the WAIT instruction

- After Exiting Wait Mode

(10) Set the exit priority level to “7” as soon as exiting wait mode

Note1: When entering wait mode while the CM02 bit in the CM0 register is set to “1” (peripheral function stops in wait mode), set the MCD4 to MCD0 bits in the MCD register to maintain 10MHz CPU clock freguency or less after main clock is divided.

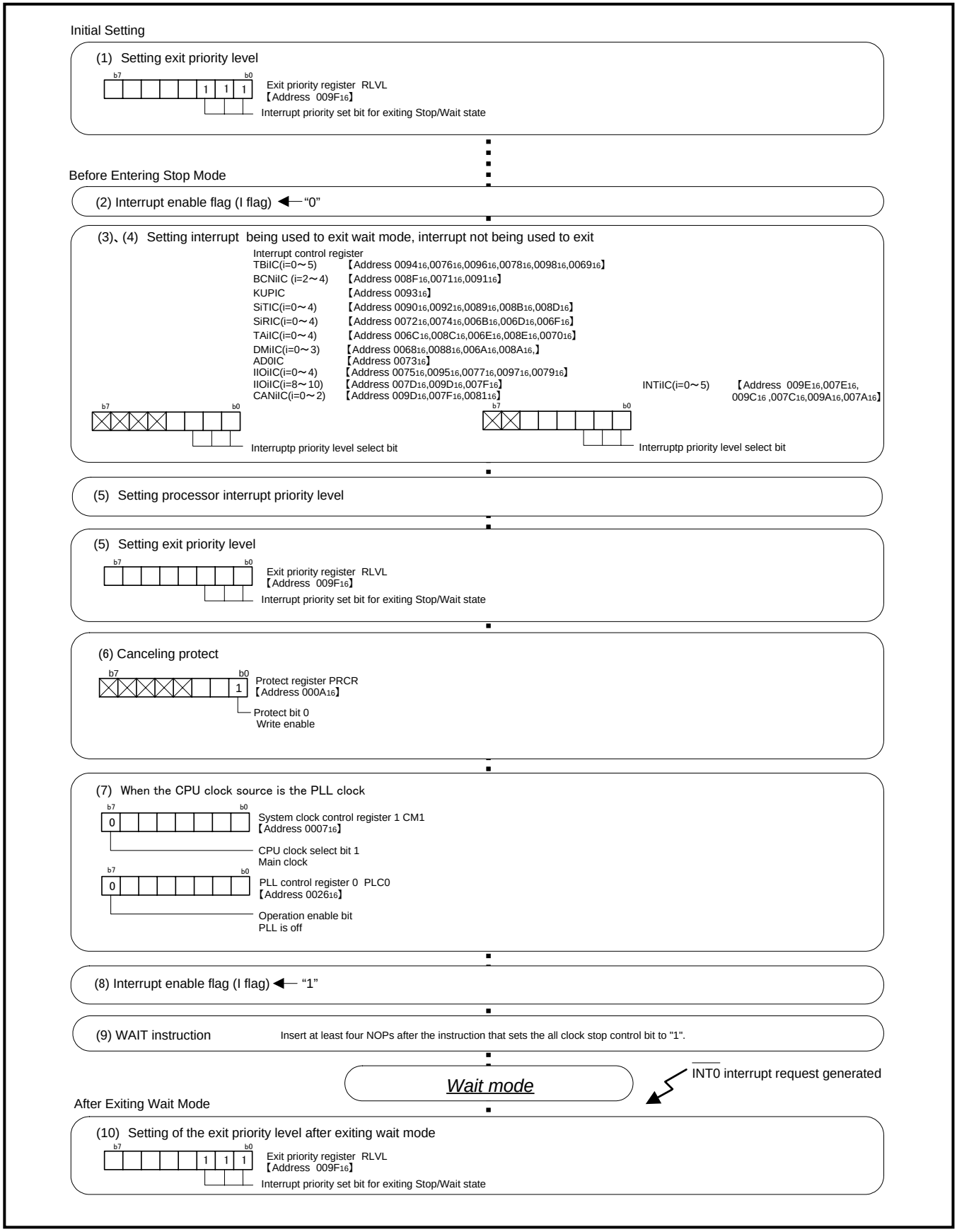

Figure 1. Example of wait mode set-up

4. The example of reference program

```
;***************************************************************************
;
;    M32C/84 Program Collection
;
;    FILE NAME : rjj05b0764_src.a30
;    CPU       : M32C/84 Group
;    FUNCTION  : Wait Mode Set-up
;    HISTORY   : 2005.4.7   Ver 1.00
;
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;
;***************************************************************************
;***************************************************************************
;         Include
;***************************************************************************
;
        .LIST       off                 ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr32c84.inc        ;Reads the file that defined SFR
        .LIST       on                  ;Starts outputting lines to the assembler list file
;
;***************************************************************************
;         Symbol definition
;***************************************************************************
;
RAM_TOP             .equ    000400h     ;Start address of RAM
RAM_END             .equ    002affh     ;End address of RAM
ROM_TOP             .equ    0fe0000h    ;Start address of ROM
VECT_TOP            .equ    0fffe00h    ;Start address of vect_top
FIXED_VECT_TOP      .equ    0ffffdch    ;Start address of fixed_vect_top
;
;***************************************************************************
;         Program area
;***************************************************************************
;=========================================================================
;         Start up
;=========================================================================
        .SECTION    PROGRAM, CODE       ;Declares section name and section type
        .ORG        ROM_TOP             ;Declares start address
START:
        ldc         #RAM_END+1,isp      ;Sets interrupt stack pointer
        mov.b       #03h, prcr          ;Removes protect
        mov.w       #0254h,plc0         ;Multiply-by-8
        bset        plc07               ;PLL is on
```

```
        mov.w       #1000,r0            ;Wait 5ms
CNT:
        dec.w       r0                  ;
        cmp.w       #0,r0               ;
        jnz         CNT                 ;
        mov.b       #00000000b, pm0     ;Single-chip mode
        mov.b       #00000000b, pm1     ;
        mov.b       #00001000b, cm0     ;Xcin-Xcout High
        mov.b       #10100000b, cm1     ;PLL clock
        mov.b       #00010010b, mcd     ;No division mode
        mov.b       #00h, prcr          ;Protects all registers
        ldc         #VECT_TOP,intb      ;Sets interrupt table register
;
;=========================================================================
;         Main program
;=========================================================================
MAIN:
;
        mov.b       #00000111b,rlvl     ;Exit priority register
;                           +++---------;Interrupt priority set bit for exiting stop/wait state
                                        ;(111:Level 7, interrupt disabled)
WAIT_MODE:
        fclr        i                   ;Clear interrupt enable flag
        mov.b       #00000101b,int0ic   ;Interrupt control register
;                           |+++---------;Interrupt priority level select bit
;                           |           ;(101:Level 5, interrupt disabled)
;                           +-----------;Interrupt request bit (0:Interrupt not requested)
        ldipl       #3                  ;Intterrupt permission level: 3
        mov.b       #00000011b,rlvl     ;Exit priority register
;                            +++---------;Interrupt priority set bit for exiting stop/wait state
                                        ;(011:Level 3, interrupt disabled)

        mov.b       #00000001b,prcr     ;Removes protect
        mov.b       #00100000b, cm1     ;Main clock
        bclr        plc07               ;PLL is off
        mov.b       #00000000b,prcr     ;Protect all registers
        fset        i                   ;Set interrupt enable flag
;
        wait                            ;Wait mode
;
        nop
        nop
        nop
        nop
;
MAIN_B:
;
```

```
        jmp             MAIN_B
;
;=============================================================================
;           Interrupt program
;=============================================================================
INT0_INT:
;
        mov.b           #00000111b,rlvl         ;Exit priority register
;                               +++-------------------;Interrupt priority set bit for exiting stop/wait state
                                                ;(111:Level 7, interrupt disabled)
;
                        reit
;
;=============================================================================
;           Dummy interrupt processing program
;=============================================================================
DUMMY:
                        reit
;
;*****************************************************************************
;           Setting of variable vector table
;*****************************************************************************
;
        .SECTION        VECT,ROMDATA
        .ORG            VECT_TOP + (8*4)
;
        .lword                  DUMMY           ;DMA0 interrupt vector
        .lword                  DUMMY           ;DMA1 interrupt vector
        .lword                  DUMMY           ;DMA2 interrupt vector
        .lword                  DUMMY           ;DMA3 interrupt vector
        .lword                  DUMMY           ;TA0 interrupt vector
        .lword                  DUMMY           ;TA1 interrupt vector
        .lword                  DUMMY           ;TA2 interrupt vector
        .lword                  DUMMY           ;TA3 interrupt vector
        .lword                  DUMMY           ;TA4 interrupt vector
        .lword                  DUMMY           ;UART0 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART0 receive/ACK interrupt vector
        .lword                  DUMMY           ;UART1 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART1 receive/ACK interrupt vector
        .lword                  DUMMY           ;TB0 interrupt vector
        .lword                  DUMMY           ;TB1 interrupt vector
        .lword                  DUMMY           ;TB2 interrupt vector
        .lword                  DUMMY           ;TB3 interrupt vector
        .lword                  DUMMY           ;TB4 interrupt vector
        .lword                  DUMMY           ;INT5 interrupt vector
        .lword                  DUMMY           ;INT4 interrupt vector
        .lword                  DUMMY           ;INT3 interrupt vector
```

```
        .lword          DUMMY       ;INT2 interrupt vector
        .lword          DUMMY       ;INT1 interrupt vector
        .lword          INT0_INT    ;INT0 interrupt vector
        .lword          DUMMY       ;TB5 interrupt vector
        .lword          DUMMY       ;UART2 transmit/NACK interrupt vector
        .lword          DUMMY       ;UART2 receive/ACK interrupt vector
        .lword          DUMMY       ;UART3 transmit/NACK interrupt vector
        .lword          DUMMY       ;UART3 receive/ACK interrupt vector
        .lword          DUMMY       ;UART4 transmit/NACK interrupt vector
        .lword          DUMMY       ;UART4 receive/ACK interrupt vector
        .lword          DUMMY       ;Bus collision detection,start/stop
                                    ;condition detection (UART2) interrupt vector
        .lword          DUMMY       ;Bus collision detection,start/stop
                                    ;condition detection (UART3) interrupt vector
        .lword          DUMMY       ;Bus collision detection,start/stop
                                    ;condition detection (UART4) interrupt vector
        .lword          DUMMY       ;A-D interrupt vector
        .lword          DUMMY       ;KEY interrupt vector
        .lword          DUMMY       ;IntelligentI/O interrupt vector0
        .lword          DUMMY       ;IntelligentI/O interrupt vector1
        .lword          DUMMY       ;IntelligentI/O interrupt vector2
        .lword          DUMMY       ;IntelligentI/O interrupt vector3
        .lword          DUMMY       ;IntelligentI/O interrupt vector4
        .lword          DUMMY       ;IntelligentI/O interrupt vector8
        .lword          DUMMY       ;IntelligentI/O interrupt vector9,CAN0
        .lword          DUMMY       ;IntelligentI/O interrupt vector10,CAN1
        .lword          DUMMY       ;CAN2
;
;*******************************************************************************
;           Setting of fixed vector
;*******************************************************************************
;
        .SECTION        F_VECT,ROMDATA
        .ORG            FIXED_VECT_TOP
;
        .lword          DUMMY       ;Undefined instruction interrupt vector
        .lword          DUMMY       ;Overflow (INTO instruction) interrupt vector
        .lword          DUMMY       ;BRK instruction interrupt vector
        .lword          DUMMY       ;Address match interrupt vector
        .lword          DUMMY       ;
        .lword          DUMMY       ;Watchdog timer interrupt vector
        .lword          DUMMY       ;
        .lword          DUMMY       ;NMI interrupt vector
        .lword          START       ;Sets start vector
;
        .end
```

5. Referense

Hardware manual

M32C/84 group Hardware Manual

(Use the latest version on the web-site: http://www.renesas.com)

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http://www.renesas.com/

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Revision

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		Page	Point
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