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M16C/62P Group

Wait Mode Set-Up

1. Abstract

Settings and operation for entering wait mode are described here. Figure 2 shows the set-up procedure. A reference program is an example when using the INT0 interrupt for a return factor from wait mode.

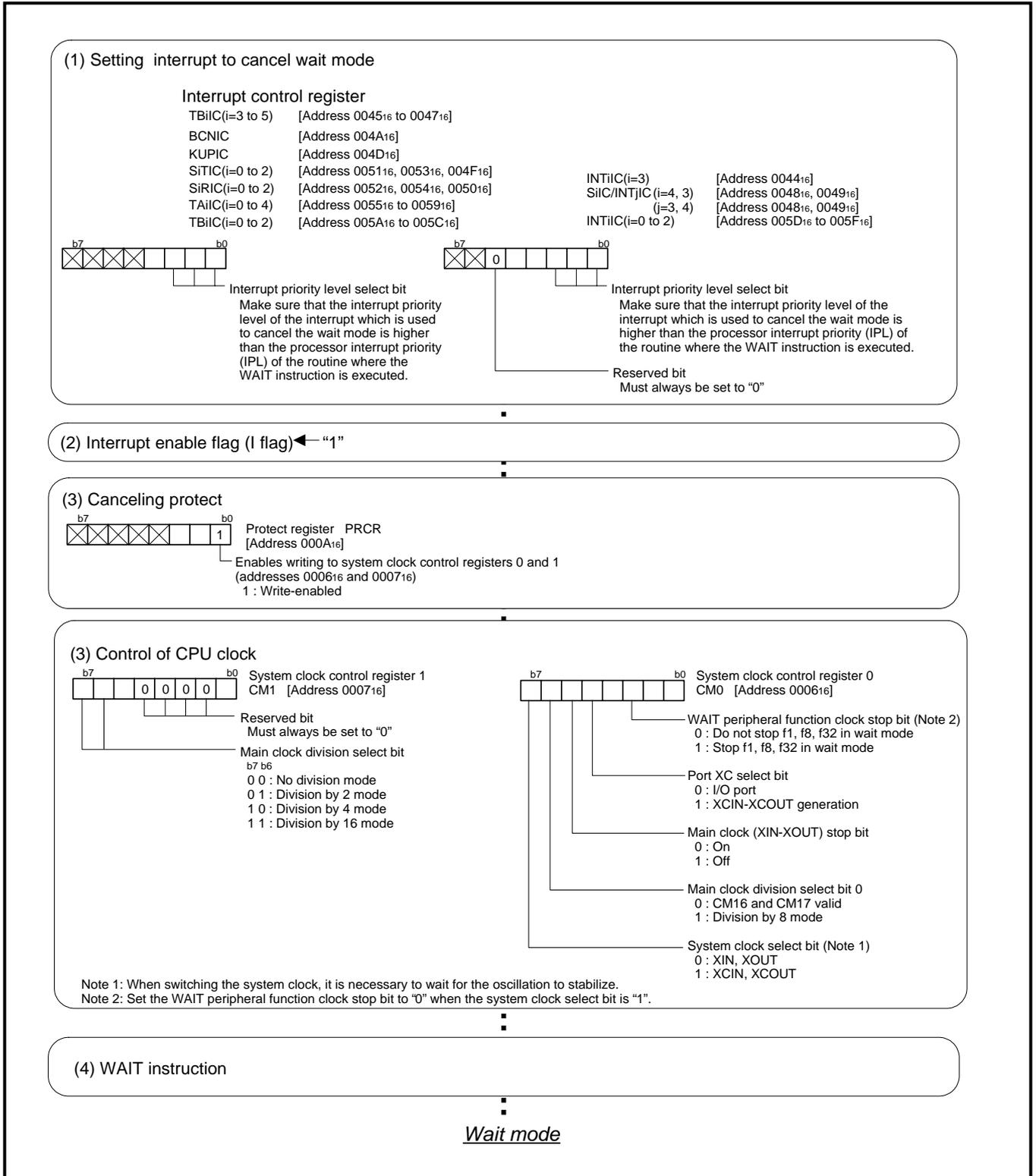
2. Introduction

This application note is applied to the M16C/62P group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M16C/62P Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation

3. Set-up

- (1) Enables the interrupt used for returning from wait mode.
- (2) Sets the interrupt enable flag (I flag) to "1".
- (3) Clears the protection and changes the content of the system clock control register.
- (4) Executes the WAIT instruction.



4. The example of reference program

```

*****
;
;
; M16C/62P Program Collection
;
; FILE NAME : rjj05b0697_src.a30
; CPU       : M16C/62P Group
; FUNCTION  : Wait Mode Set-up
; HISTORY   : 2004.12.24  Ver 1.00
;
; Copyright(C)2004, Renesas Technology Corp.
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;
*****
;
*****
; Include
*****
;
; .LIST      off           ;Stops outputting lines to the assembler list file
; .INCLUDE   sfr62p.inc    ;Reads the file that defined SFR
; .LIST      on           ;Starts outputting lines to the assembler list file
;
;
*****
; Symbol definition
*****
;
;
RAM_TOP      .equ    00400h    ;Start address of RAM
RAM_END      .equ    013ffh    ;End address of RAM
ROM_TOP      .equ    0f4000h   ;Start address of ROM
VECT_TOP     .equ    0ffe00h   ;Start address of vect_top
FIXED_VECT_TOP .equ    0fffdch  ;Start address of fixed_vect_top
SB_BASE      .equ    00380h    ;Base address of sb
;
;
*****
; Program area
*****
;
=====
; Start up
=====
;
;
; .section   program,code     ;Declares section name and section type
; .org      ROM_TOP          ;Declares start address
; .sb       SB_BASE          ;
;
;
START:

```

```

ldc          #RAM_END+1,isp ;Sets interrupt stack pointer
ldc          #SB_BASE,sb   ;Sets sb register
;
mov.b        #03h,prcr     ;Removes protect
;Set processor mode registers 0 and 1
mov.w        #0800h,pm0    ;Single-chip mode
;No expansion, No wait
mov.w        #2008h,cm0    ;Xcin-Xcout High
;Xin-Xout High, Main clock is No divison
mov.b        #0,prcr       ;Protects all registers
;
ldintb       #VECT_TOP     ;Sets interrupt table register
;
mov.w        #0,r0         ;Clears WORKRAM area
mov.w        #((RAM_END+1)-RAM_TOP)/2,r3
mov.w        #RAM_TOP,a1
sstr.w
;
;=====
; Main program
;=====
MAIN:
;
fclr         i             ;Clear interrupt enable flag
;M16C-85-0202(Japanese) countermeasure
;M16C-85-0204(English) countermeasure
;
mov.b        #00000011b,int0ic ;Interrupt control register
;          |+++-----;Interrupt priority level select bit
;          |           ;(011:Level 3, interrupt disabled)
;          +-----;Interrupt request bit (0:interrupt not requested)
mov.w        #00400h,r0     ;Dummy read
fset         i             ;Set interrupt enable flag
mov.b        #00000001b,prcr ;Removes protect
mov.b        #00001000b,cm0 ;Xcin-Xcout(High)
mov.b        #00100000b,cm1 ;Xin-Xout(High)
mov.b        #00000000b,prcr ;Protects all register

MAIN_A:
;
jmp.b        MAIN_B        ;TN-16C-128A/JA(Japanese) countermeasure
;TN-16C-128A/EA(English) countermeasure
MAIN_B:
wait         ;Wait mode
;
nop
nop
nop

```

```

        nop
;
MAIN_C:
        jmp          MAIN_C
;
;=====
;      Interrupt program
;=====
INT0_INT:
;
;          ;/ INT0 interrupt routine /
;
        reit
;
;=====
;      Dummy interrupt processing program
;=====
DUMMY:
        reit
;
;*****
;      Setting of variable vector table
;*****
;
        .section vect,romdata
        .org          VECT_TOP + (4 * 4)
;
        .lword        DUMMY          ;INT3 interrupt vector
        .lword        DUMMY          ;TB5 interrupt vector
        .lword        DUMMY          ;TB4 interrupt vector
;
        .lword        DUMMY          ;UART1 bus collision detection interrupt vector
        .lword        DUMMY          ;TB3 interrupt vector
;
        .lword        DUMMY          ;UART0 bus collision detection interrupt vector
        .lword        DUMMY          ;SI/04/INT5 interrupt vector
        .lword        DUMMY          ;SI/03/INT4 interrupt vector
        .lword        DUMMY          ;UART2 bus collision detection interrupt vector
        .lword        DUMMY          ;DMA0 interrupt vector
        .lword        DUMMY          ;DMA1 interrupt vector
        .lword        DUMMY          ;KEY interrupt vector
        .lword        DUMMY          ;A-D interrupt vector
        .lword        DUMMY          ;UART2 transmit/NACK interrupt vector
        .lword        DUMMY          ;UART2 receive/ACK interrupt vector
        .lword        DUMMY          ;UART0 transmit/NACK interrupt vector
        .lword        DUMMY          ;UART0 receive/ACK interrupt vector
        .lword        DUMMY          ;UART1 transmit/NACK interrupt vector
        .lword        DUMMY          ;UART1 receive/ACK interrupt vector
        .lword        DUMMY          ;TA0 interrupt vector

```

```

.word          DUMMY          ;TA1 interrupt vector
.word          DUMMY          ;TA2 interrupt vector
.word          DUMMY          ;TA3 interrupt vector
.word          DUMMY          ;TA4 interrupt vector
.word          DUMMY          ;TB0 interrupt vector
.word          DUMMY          ;TB1 interrupt vector
.word          DUMMY          ;TB2 interrupt vector
.word          INTO_INT       ;INT0 interrupt vector
.word          DUMMY          ;INT1 interrupt vector
.word          DUMMY          ;INT2 interrupt vector
;
;*****
;
;   Setting of fixed vector
;*****
;
;
;   .section f_vect,romdata
;   .org          FIXED_VECT_TOP
;
;   .word          DUMMY          ;Undefined instruction interrupt vector
;   .word          DUMMY          ;Overflow (INTO instruction) interrupt vector
;   .word          DUMMY          ;BRK instruction interrupt vector
;   .word          DUMMY          ;Address match interrupt vector
;   .word          DUMMY          ;Single-step interrupt vector
;   .word          DUMMY          ;Watchdog timer interrupt vector
;   .word          DUMMY          ;Oscillation stop and Re-oscillation detection interrupt
;   .word          DUMMY          ;vector
;   .word          DUMMY          ;Voltage down detection interrupt vector
;   .word          DUMMY          ;DBC interrupt vector
;   .word          DUMMY          ;NMI interrupt vector
;   .word          START         ;Sets start vector
;
;   .end

```

5. Referense

Hardware manual

M16C/62P group (M16C/62P,M16C/62PT) Hardware Manual Rev.2.30

(Use the latest version on the web-site: <http://www.renesas.com>)

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Revision

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		Page	Point
1.00	2004.12	-	First edition issued

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