VersaClock 7 Reference Schematics and Power Filtering Recommendations

VersaClock®7 reference schematics are provided to help customers optimize their schematics designs when using VersaClock 7 (VC7) devices. It will highlight some of the new features in the devices that require different handling of circuitry to match with them.

This document provides different termination schemes when driving different standard receivers like HCSL, LVPECL, LVDS, CML and STSL. It also provides recommendations for power supply filtering for the device, especially when some of power filtering can be combined or shared among multiple power supply rails to save board space as often required by some customer designs. Lastly, the app note provides simulation results using recommended power filtering topologies.

The contents in this document apply to the entire product family devices including RC21005/RC31005 (5-output), RC21008/RC31008 (8-output) and RC21012/RC31012 (12-output). RC2100xAQ/BQ (x = 5, 8) and RCx1012AQ/BQ (x = 2, 3) devices have internal crystal thus the crystal and crystal overdrive is not applicable.

For reference schematics, see section 2**.**

Contents

1. Reference Schematics Considerations

This section will summarize each circuit block of a VC7 device design.

1.1 Crystal Interface and Crystal Overdrive

Crystal interface in VC7 devices support 3 different signal sources or types. They are:

1. Crystal oscillator.

   XIN and XOUT pins are connected to a crystal's X1 and X2 terminals as shown below. This is the most common PLL reference source. Please note VC7 has built in sufficient and flexible internal crystal load capacitance (0–26pF). It is recommended that no external load capacitors used for the crystal to save components and board space. Specify C_L of selected crystal and configure the value internally.

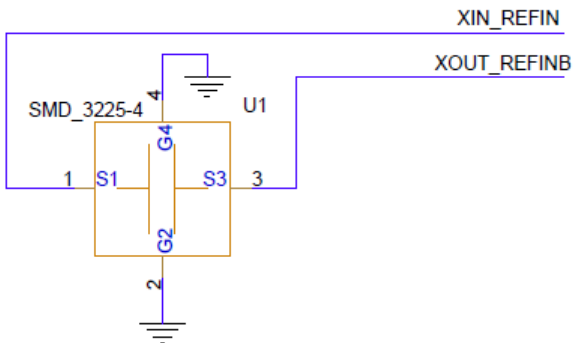


Figure 1. Crystal Connection to DUT

   When configured for a crystal reference, a single-ended LVCMOS signal can be used to overdrive XIN pin of the crystal interface. XOUT pin can be left floating in this case.

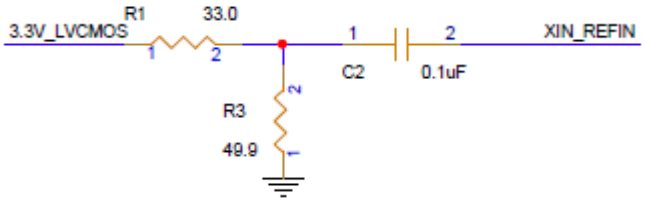


Figure 2. When Crystal Mode is Configured, XIN can be Overdriven by a 3.3V LCMOS Clock

2. LVCMOS overdrive input.

   XIN pin can be configured to take a direct 3.3V LVCMOS signal as APLL reference without amplitude attenuation. An LVCMOS signal with a source termination (usually a series resistor equal in value to 50Ω minus Ro which is the driver's internal impedance) can directly feed into XIN pin. XOUT pin is left floating.

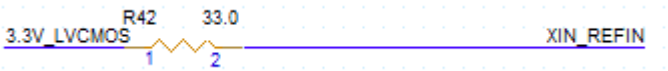


Figure 3. 3.3V LVCMOS Clock Feeding XIN Directly when Configured in "Single-ended" Mode

3. Differential signal input.

   What's new in VC7 is that its crystal interface (XIN and XOUT pins) can take in a differential pair signal directly as a APLL reference when XIN/XOUT is configured in "Differential" mode. This is a redundant function as this differential pair can also drive CLKIN0/CLKIN0B or CLKIN1/CLKIN1B, APLL reference mux can select it as the source for APLL reference.

1.2 GPI – General-Purpose Input

VC7 devices have four pins with dual definitions (RC21005AQ only has two of such pins): as two differential or four single-ended input clocks – CLKIN0/CLKIN0B, CLKIN1/CLKIN1B, or as four general-purpose inputs – GPI[3:0]. See details below.

1.2.1 As Input Clocks

When used as input clocks, pin names are CLKIN0, CLIN0B, CLKIN1 and CLKIN1B. For taking in differential input clock, CLKIN0/CLKIN0B are an input differential pair; so is CLKIN1/CLKIN1. Each pin is also be used as a single-ended LVCMOS input clock, each pin. The usage of input clock types need to be configured accordingly in RICBox GUI.

Either differential or single-ended, the clock can be properly terminated externally and DC-coupled to the inputs. External clocks can also ac-coupled to the inputs for which input has internal DC-offset to support ac-coupling.

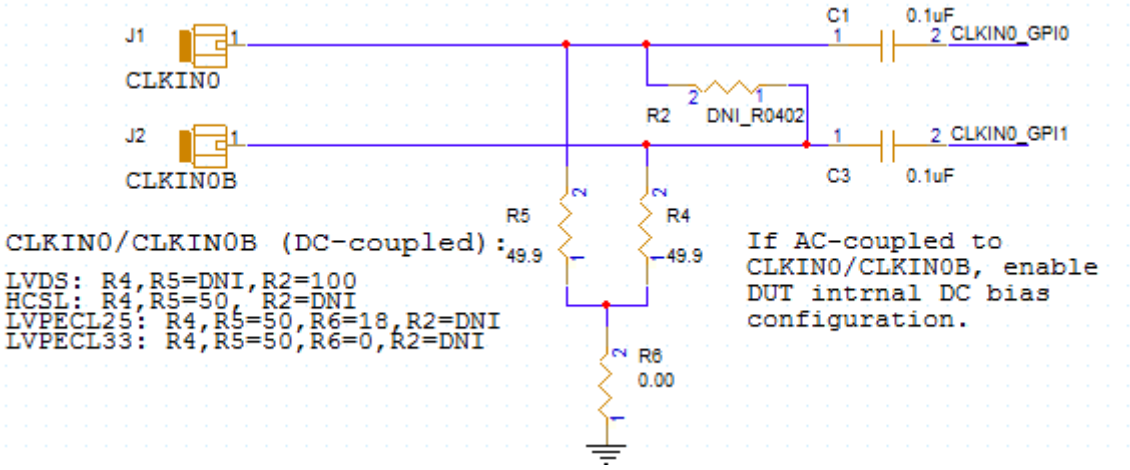


Figure 4. Input Clock Interface with Various Differential Types

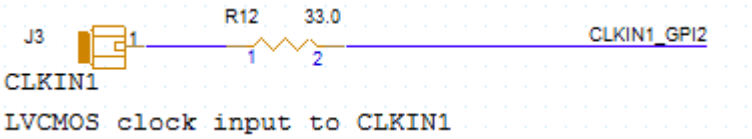


Figure 5. Input Clock Interface with LVCMOS Type

1.2.2 As General Purpose Input

If not used as input clocks, these 4 pins can be used as general-purpose inputs. They can be configured with a function. For example, it can be configured as an output enable control (OE function), with active edge configurable as well. When SPI port is configured, one of the GPI pins can be configured as SDI signal.

1.3 GPIO Pins

GPIO[2:0] pins are used for selecting up to 27 configurations (each GPIO pin with 3 states – low, middle and high). In a single configuration design, no GPIO pin is needed for configuration select. Middle level is only supported in configuration select.

When used as a GPIO pin, each of 5 GPIO pin supports a variety of functions (for more information, see the *VersaClock 7 Schematic Checklist*). As for the schematics, they are LVCMOS-compatible inputs or outputs.

Each of GPIO pin has internal pull-up or pull-down, which can be each enabled or disabled, or both disabled. Both pull-up and pull-down enabled is supported but no use case for it as no middle level is supported as a general-purpose IO.

1.4 Serial Port (I^2C and SPI)

1.4.1 I^2C

I^2C is the default serial port in the device. SCL and SDA have dedicated pins. The only point to note for I^2C pins is that both SCA and SDA require a pull-up resistor. For a single I^2C slave, a 4.7KΩ pull-up resistor can be used; for an I^2C bus with multiple I^2C slave devices, 1kΩ pull-up resistor is recommended.

1.4.2 SPI

VC7 devices support SPI when configured so. In SPI setting, SCL (pin 9) is SCLK, nCS (pin 10) is chip select, one of GPIO pins can be configured as SDI and another GPIO as SDO. When configured 3-wire SPI, only one of GPIO pins is need and configured as SDIO. Each SPI signals are treated as LVCMOS signals.

1.5 Outputs

When differential type is configured, VC7 outputs support LVDS or LP-HCSL. LP-HCSL is source terminated. When driving LVPECL or CML receivers, LP-HCSL type is configured and AC-couple to the receiver with external termination/DC-bias circuit. See the reference schematic circuit examples in section 2. In the schematics, the following examples are illustrated:

- LP-HCSL driving an HCSL receiver with DC-coupling (OUT1/OUT1B)
- LP-HCSL driving an LVPECL receiver with AC-coupling (OUT2/OUT2B)
- LP-HCSL driving an LVDS receiver with AC-coupling (OUT3/OUT3B)
- LP-HCSL driving an LVDS receiver with internal termination with AC-coupling (OUT6/OUT6B)
- LP-HCSL driving a CML receiver with AC-coupling (OUT7/OUT7B)
- LP-HCSL driving an SSTL receiver with AC-coupling (OUT8/OUT8B)
- LVDS driving an LVDS driver with DC-coupling (OUT10/OUT10B, OUT11/OUT11B)

When LVCMOS output is configured, each output pair (for differential output) can support 2 LVCMOS outputs. The 2 LVCMOS outputs can be individually enabled or disabled. When both LVCMOS are enabled, the phase relationship between the two can be set in-phase, or 180-degrees out-of-phase.

1.6 Power Supply Pins

1.6.1 Power Supply Overview

VC7 power supply is divided into 2 groups: core voltages and output driver supply voltages. Core voltages include:

- VDDR – power supply for input clocks
- VDDX – power supply for crystal oscillator circuits
- VDDD – power supply for digital core circuits
- VDDA – power supply for analog core circuits

VC7 has 3 variants of devices in terms of number of outputs: 5-output, 8-output and 12-output. The number of outputs with respect to number of output banks with each power supply are listed in Table 1.

Table 1. Output Bank and its Power Supply

Number of Outputs	Number of Output Banks	Bank Power Supply	Part Numbers
5-Output	5 (Bank1–5)	VDDO1–5, respectively	RC21005AQ, RC31005AQ
8-Output	6 (Bank1–6)	VDDO1–6, respectively	RC21008, RC21008AQ RC31008 RC31008AQ
12-Output	7 (Bank0–6)	VDDO0–6, respectively	RC21012 RC31012

Each power rail supports 1.8V, 2.5V or 3.3V. For best possible performance, it is desired that a separate power filtering is used for each individual power domain in schematics designs. However, under certain conditions two or more power supply filtering can be combined so that not as many separate power filtering are necessary. This is especially needed when a PCB board space constraint condition is present.

1.6.2 Power Supply Filtering

A power filtering topology for each of the power supply domain is demonstrated in Figure 6. When there is no board space constraint, it is recommended to use the following filter for each and every power rail to avoid noise coupling and interferences from one another.

On top of each power rail filtering, it is also recommended that there is a 0.1µF decoupling capacitor for each power pin. Place this decoupling capacitor on the same board layer as DUT and as close to each power pin as possible. Use the ground via to ground each decoupling capacitor. Do not share ground vias between these decoupling capacitors.

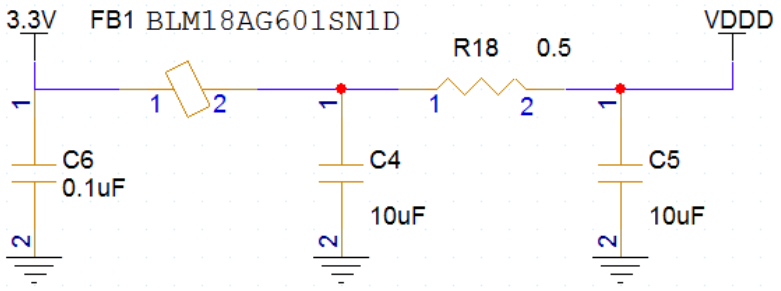


Figure 6. Power Filtering for Each Power Domain

As noted, there is a 0.5Ω series resistor in the filter for further noise attenuation. However, this series resistor can cause DC voltage drop of the power rail when current is big. Among VC7 power rails, VDDA draws a current of ~141–150mA. Other rails draw a current less than 35mA. Some rails draw less than 10mA. Therefore, VDDA is the only power rail that could risk a voltage drop below some design specifications. In order to minimize DC voltage drop for VDDA rail, there are the following workarounds:

- Select a ferrite bead with minimum DCR
- Remove 0.5Ω series resistor in the filter path

1.6.3 Power Filtering Reduction

As stated above, it is recommended that each power rail has its own separate filtering. In cases where PCB board space is a constraint, power filtering can be combined or shared by multiple power rails with the following conditions:

- When input clock is not used, VDDR can share a filter with VDDX or VDDD
- When outputs have a same frequency, they can share VDDO rail filtering
- When the output(s) of a bank is not used, VDDO supply for that bank can be floating thus no power filtering needed (with float_vddox enabled in the setting)

1.6.4 Power Filtering Simulations

Simulations have been conducted based on the above filter model to verify the effectiveness of the filter. Pspice models used in the simulations are from each respective vendor. Four scenarios have been simulated with results listed under each scenario. A summary of simulation results are given at the end of this section.

1.6.4.1 Scenario 1:

- 0.1µF capacitor, Murata P/N: GRM033C81E104KE14
- Ferrite bead: Murata P/N: BLM18AG601SN1
- 10µF capacitor: Murata P/N: GRM188R61E106KA73
- 0.5Ω series resistor
- 10µF capacitor: same as above

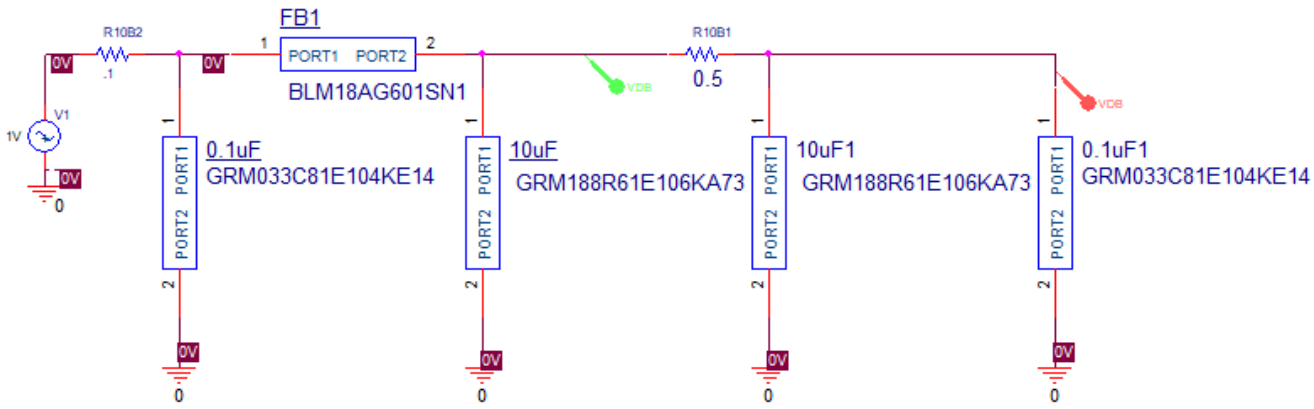


Figure 7. Schematics for Scenario 1 Simulations

Table 2. Scenario 1 Simulation Results

Frequency	1MHz	5MHz	10MHz	100MHz
Noise Suppression (dB)	-88	-115	-102	-92

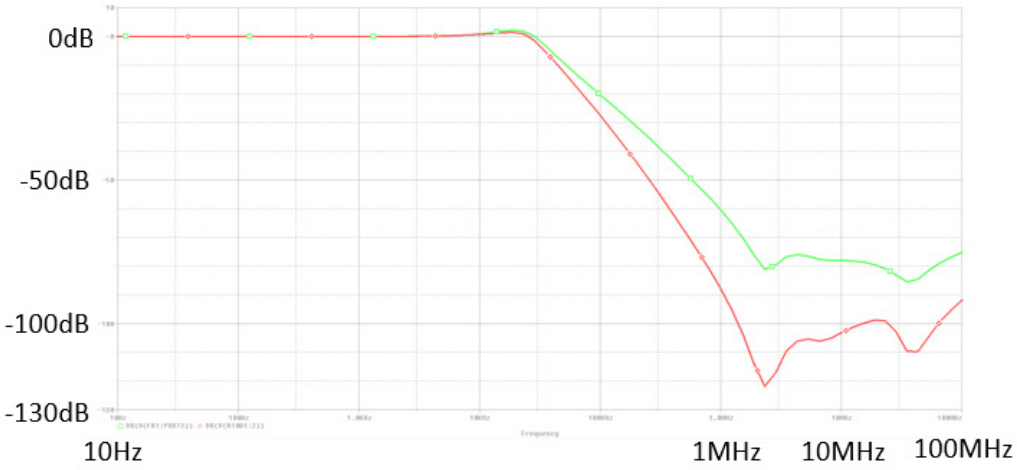


Figure 8. Noise Attenuation in Scenario 1 (see Circuit Definition above)

1.6.4.2 Scenario 2

- 0.1µF capacitor, Murata P/N: GRM033C81E104KE14
- Ferrite bead: Murata P/N: BLM18AG221SN1
- 10µF capacitor: Murata P/N: GRM188R61E106KA73
- 0.5Ω series resistor
- 10µF capacitor: same as above

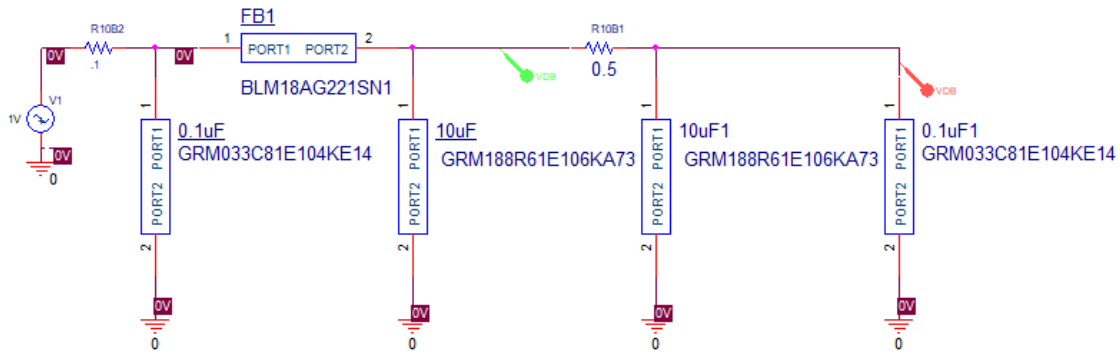


Figure 9. Schematics and Component Models for Scenario 2 Simulation

Table 3. Scenario 2 Simulation Results (1MHz–100MHz)

Frequency	1MHz	5MHz	10MHz	100MHz
Noise Suppression (dB)	-80	-105	-95	-82

Figure 10. Noise Attenuation in Scenario 2 (see Circuit Definition above)

1.6.4.3 Scenario 3

Same as Scenario 2 but remove the 2nd 10µF capacitor, as shown in Figure 11.

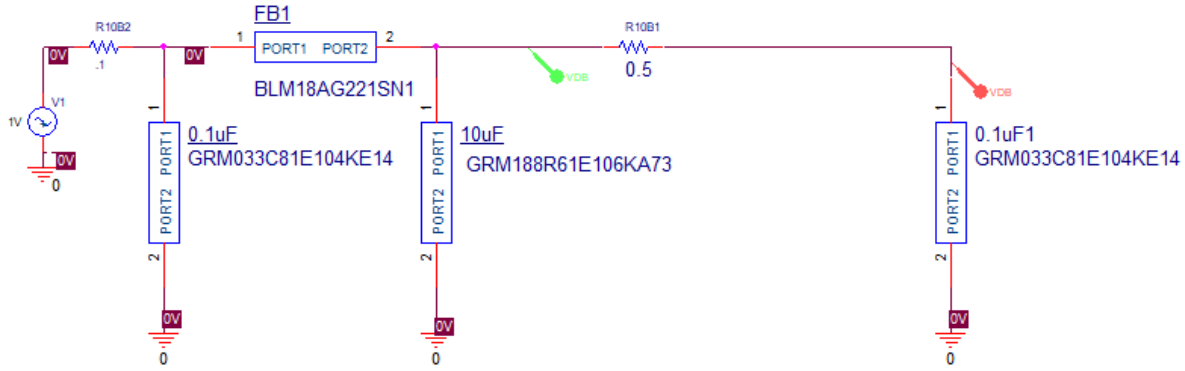


Figure 11. Schematics for Scenario 3 Simulations

Table 4. Scenario 3 Simulation Results

Frequency	1MHz	5MHz	10MHz	100MHz
Noise Suppression (dB)	-52	-72	-78	-80

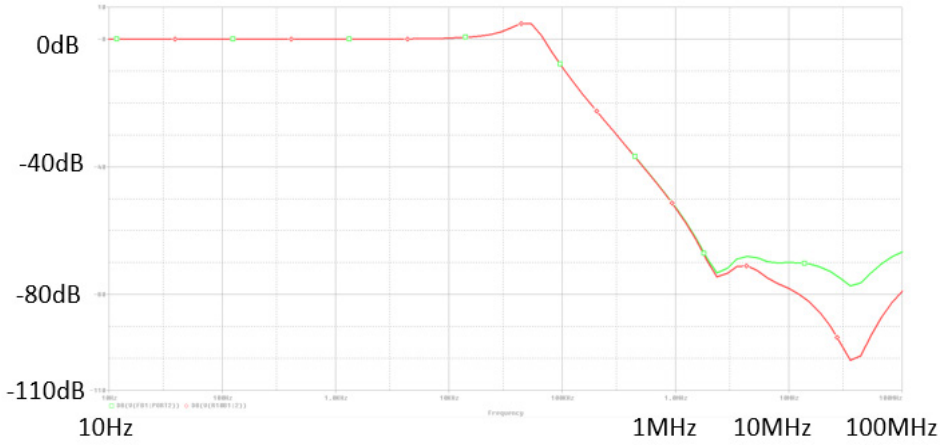


Figure 12. Noise Attenuation in Scenario 3 (see Circuit Definition above)

1.6.4.4 Scenario 4

Same as Scenario 1 but removing the series resistor (0.5Ω). To keep the same probing points, a nominal 0Ω resistor is used to keep topology the same.

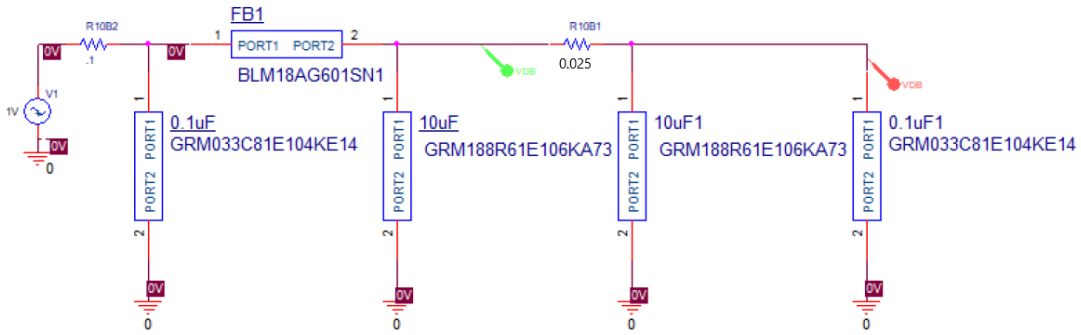


Figure 13. Filter Schematics for Simulation Scenario 4

Table 5. Scenario 4 Simulation Results

Frequency	1MHz	5MHz	10MHz	100MHz
Noise Suppression (dB)	-70	-92	-86	-85

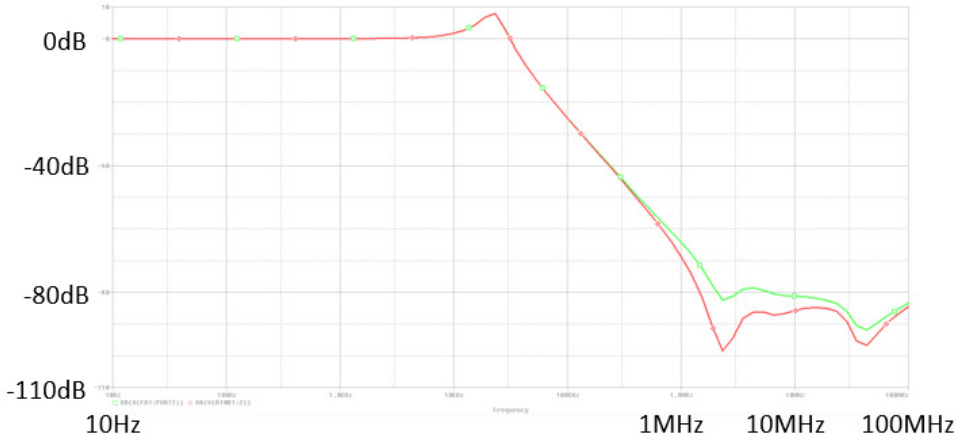


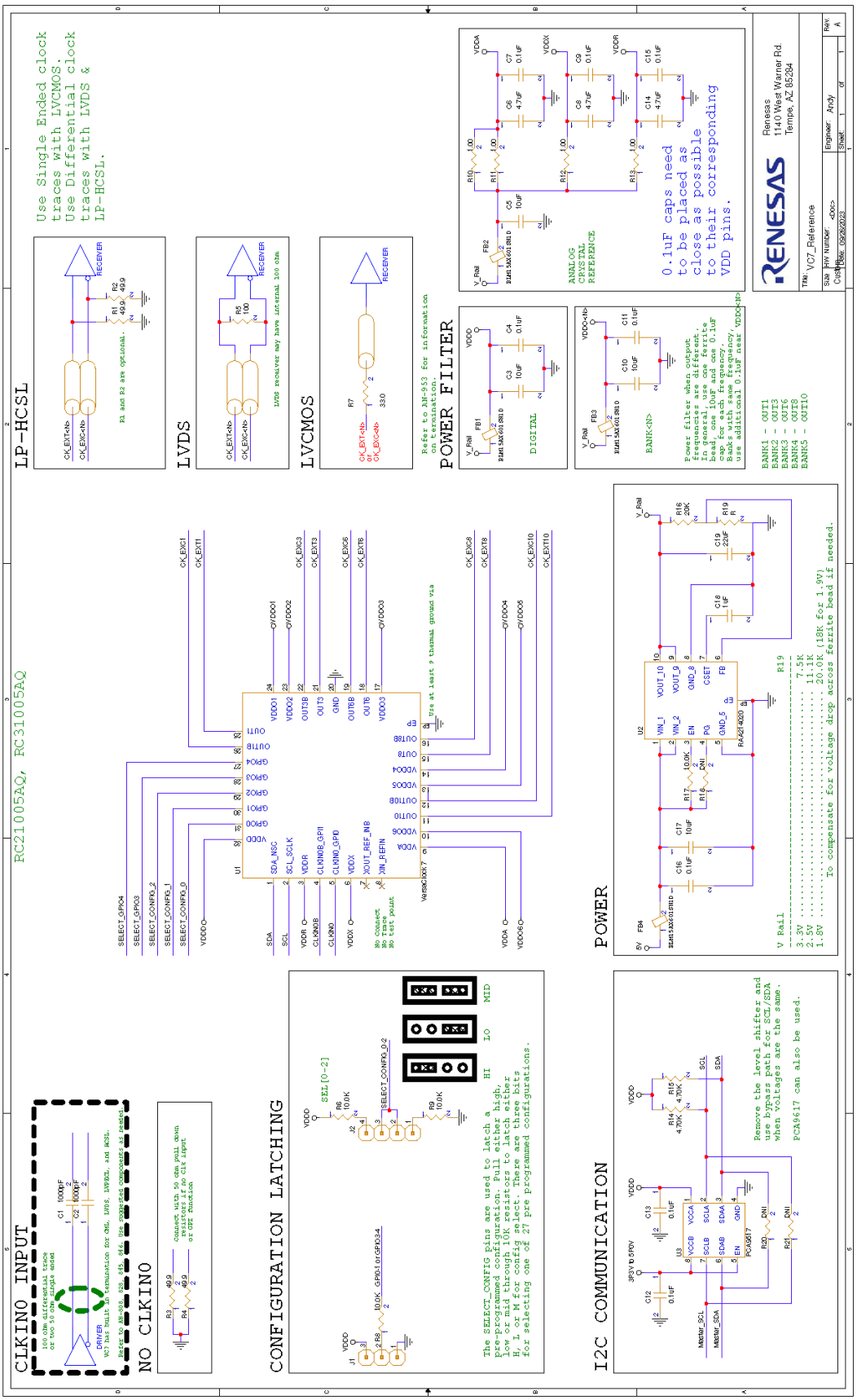
Figure 14. Noise attenuation in Scenario 4 (see Circuit Definition above)

1.6.4.5 Summary

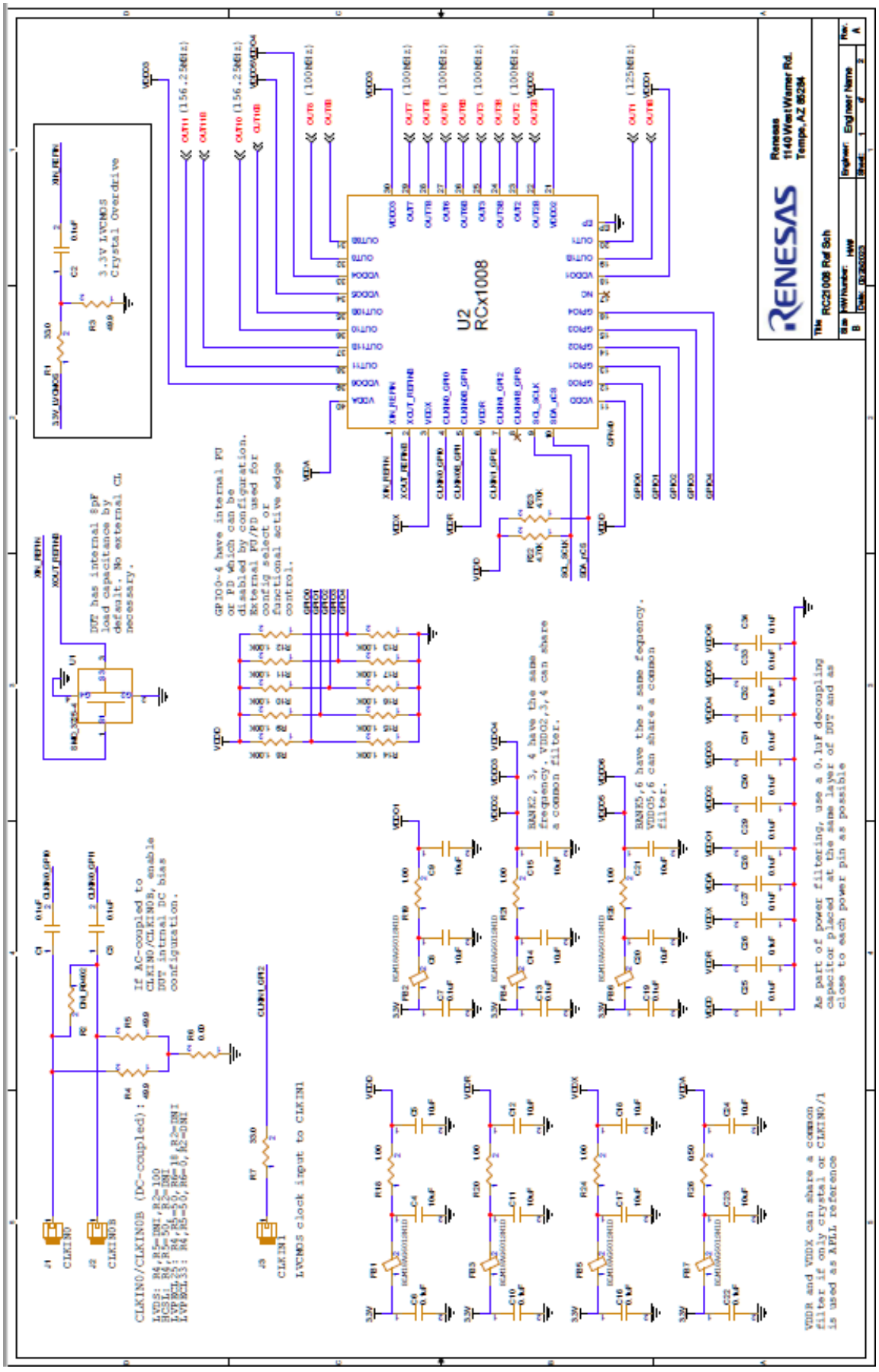
- Ferrite bead with a higher impedance (at 100MHz) attenuates noise better – compare noise attenuation data between Table 2 and Table 3.
- The 10µF bypass capacitor at the right-hand side of the series resistor is not redundant. It helps a significant noise attenuation – compare noise attenuation data between Table 2 and Table 4.
- The 0.5Ω series resistor helps attenuate noise by 7dB (at 100MHz) to 18dB (at 1MHz).

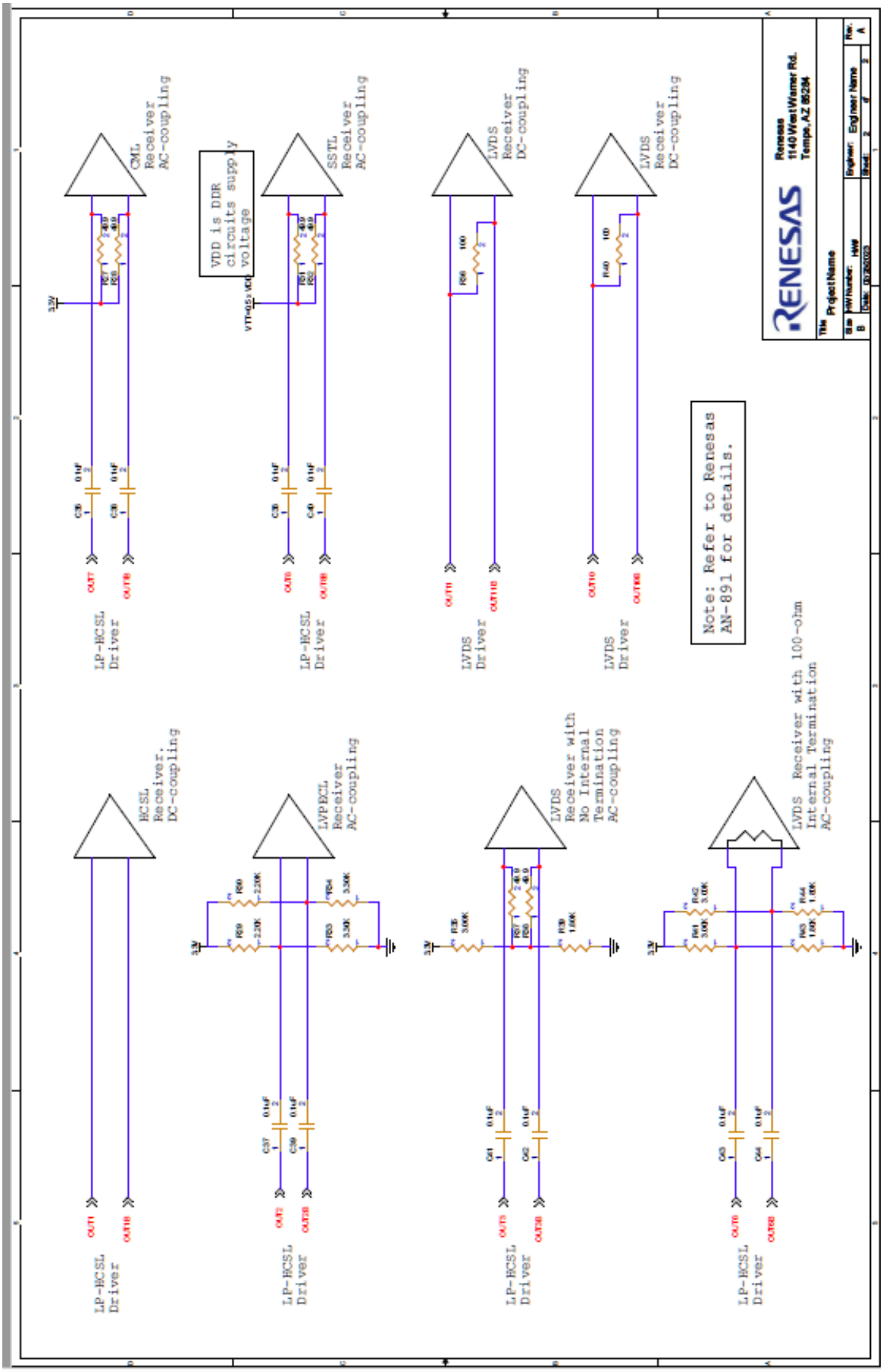
2. Reference Schematics

2.1 5-Output Reference Schematics (RC21005AQ/BQ, RC31005AQ/BQ)

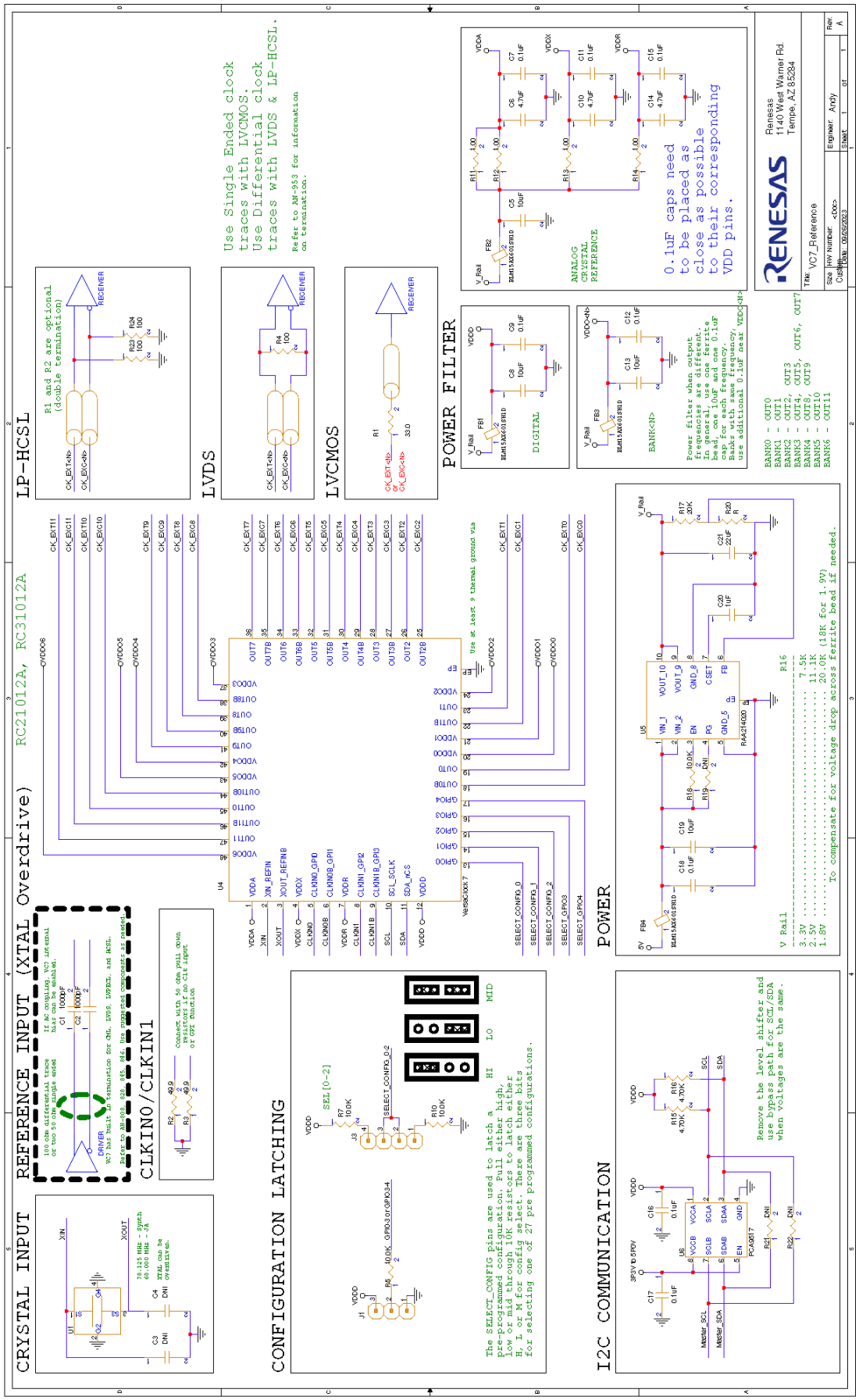


2.2 8-Output Reference Schematics (RC21008B/Q, RC31008B/Q)




CML
Receiver
AC-coupling
VDD is DDR
circuits supply
voltage
SSTL
Receiver
AC-coupling
LVDS
Receiver
DC-coupling
LVDS
Receiver
DC-coupling
LP-HCSL
Driver
LP-HCSL
Driver
LVDS
Driver
LVDS
Driver
Note: Refer to Renesas
AN-891 for details.
HCSL
Receiver,
DC-coupling
LVPECL
Receiver
AC-coupling
LVDS
Receiver with
No Internal
Termination
AC-coupling
LVDS Receiver with 100-ohm
Internal Termination
AC-coupling
LP-HCSL
Driver
LP-HCSL
Driver
LP-HCSL
Driver
LP-HCSL
Driver
RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title
ProjectName
Engineer
Engineer Name

2.3 12-Output Reference Schematics (RC21012B/Q, RC31012B/Q)



3. Revision History

Revision	Date	Description
1.03	Oct 31, 2025	▪ Corrected 2 typos in section 1.6.3.
1.02	Oct 26, 2023	▪ Updated front page text ▪ Updated Crystal Interface and Crystal Overdrive section ▪ Updated Serial Port (I^2C and SPI) section ▪ Updated Power Supply Filtering section ▪ Updated Reference Schematics section
1.01	May 26, 2023	Updated referenced part numbers by removing “A” for generics, and adding “B” to full part number(s).
1.00	May 10, 2023	Initial release.

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