### VersaClock 7 RC31 Series SYSREF

This document provides the steps needed to set up SYSREF on the VersaClock 7 (VC7) RC31 series using Renesas IC Toolbox (RICBox) software. For more information about RICBox, see the <u>Renesas IC Toolbox User</u> <u>Guide</u>.

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## 1. Installation

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox User Guide.

# 2. Creating and Loading Settings Files

RICBox settings files, or .rbs files, are used to save and distribute custom device configurations. Each settings file contains all of the register settings for a given device.

### 2.1 Creating a New Configuration

To create a new configuration:

1. Open RICBox and click on the "Create new project" link.

RENESAS	RICBox — 🗆 🗙
<u>Eile H</u> elp	
RENESAS BIG IDEAS FOR EVERY SPACE	Recent Projects
Create new project Create a new settings file.	You have no recent projects
	tinks
	Renesas Website
것님!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!	Sales Support
	Technical Support

2. Choose the RC31 device to be configured and click "OK".

RENESAS	RICBox —	
Select a Product Family	Select a Product Variant	
VersaClock7	RC21008AQ	
	RC21012A	
	RC26008A	
	RC26012A	
	RC31005AQ	
	RC31008A	
	RC31006AQ	
TED		
	Bills in reasons will be interesting with the sense of the Back OK	



3. Configure the RC31 to match the application. However, for this example, Bank0 will be configured to source from IOD0 and output 10MHz. Click the "Finish" button when done.

Renesas	RICBox	- 🗆 X
Configuring RC31012A		4 of 4 Outputs
APLL Frequency 10GHz		Outputs are arranged in output banks and some output banks share multiple outputs.
Bank 0		Each output bank gets its frequency from the selected clock source.
Power Down	Output 0 Mode LPHC V Stars	
Bank 1		
Power Down     Image: Comparison of the	Output 1 Mode LPHC × 🖆 Settings	
Bank 2		
Power Down ✓ Source FOD1 ✓ Goal Frequency None	Output 2     Output 3       Mode     LPHC `       Settings     Settings	
Cancel		Previous Finish
		Errors Warnings RC31012A Not red

## 3. Setting Up SYSREF

1. Click on the Block Diagram button to view block diagram.

RENE	SAS	RICBox			- C	l ×
Eile <u>T</u> ool	ls <u>H</u> elp					
<u> </u>	RC31012A	4.1.0	Reference			
	Settings Mode Operational Mode Input XTAL XTAL load capacitance CLKIN0 CLKIN10 CLKIN11 CLKIN15 SySClock Quad sys clock APLL Frequency Divider Loop Bandwidth Phase Margin (degrees) Third Pole Frequency DPLL Enabled Outputs OUT0 OUT1 OUT3 OUT4 OUT5 OUT6 OUT6 OUT7 OUT6 OUT7 OUT8 OUT9 OUT1 OUT1 OUT9 OUT1 OUT1 OUT1 OUT3 OUT6 OUT7 OUT6 OUT9 OUT1 OUT1 OUT1 OUT1 OUT1 OUT1 OUT3 OUT6 OUT7 OUT3 OUT1 OUT1 OUT3 OUT6 OUT7 OUT3 OUT1 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT5 OUT6 OUT7 OUT1 OUT1 OUT1 OUT1 OUT1 OUT1 OUT1 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT3 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT3 OUT1 OUT3 OUT1 OUT3 OUT3 OUT1 OUT3 OUT3 OUT3 OUT4 OUT3 OUT1 OUT3 OUT4 OUT3 OUT4 OUT3 OUT1 OUT3 OUT1 OUT3 OUT3 OUT3 OUT1 OUT3 OUT3 OUT4 OUT3 OUT3 OUT1 OUT3 OUT4 OUT3 OUT1 OUT3 OUT1 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT4 OUT3 OUT3 OUT3 OUT3 OUT4 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT3 OUT4 OUT3	SYNTH 49.152MHz 10.26 (0.0002ppt from goal of 10.26) None None None None None -227.2727MHz 10GHz (-24.4141ppt from goal of 10GHz) ~101.7253 (101+97342805/2^27) ~513.7628Hz ~69.2761 ~28.4205MHz no 10MHz [LPHCSL] powered down (Hi-Z) powered down				
	BANKO	10MHz (-24.4141ppt from goal of 10MHz)				

2. Scroll down until the SYSREFs block is visible. Click the SYSREFs block to bring up the SYSREF Configuration GUI.



 Decide how SYSREF0 will be triggered. Trigger from SYSREF\_IN requires defining a GPIO/GPI as a SYSREF\_IN. Trigger from register sysref\_trig uses the respective register field value to transition from '0' to '1'.



### 3.1 Setting Up GPIO/GPI for SYSREF\_IN Trigger

After deciding that SYSREF will be triggered from SYSREF\_IN, choose which GPIO/GPI will be the source. For this example, GPIO0 will be the source. To configure GPIO0:

1. Click the GPIO button. This opens the GPIO window.



2. In the GPIO window, click the GPIO0 button. This will open a GPIO0 options window.



3. Click on the "function" pull-down list and select SYSREF\_IN. RICBox will initially display a warning, but that will go away once SYSREF is enabled. Close the GPIO0 and GPIO windows.

RENESAS	GPIO0	—		×		
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	GPIO0 options		/			
function	GPI, input, input status	allowed r	· ·	đ		
type	RESET_IN#, input					
drive strength	SFT+, input					
enable pull up	SFT-, input					
enable pull down	SOD_EN#, input SDI, input (SPI 4-wire r	node)				
enable inversion	SYSREF_IN_Piput					
GPO output state	GPI, input, input status	s allowed	read ba	ck via SSI		
	Dynamic CSEL, input, o	dynamic c	onfigura	tion conf		
	RSTOUT# (SFTRST# AN	D HRDRS	T#), outp	out		

GPIO0 now appears in the SYSREF Configuration window for SYSREF0 channel. The reason GPIO0 is seen only in SYSREF0 channel is because the sysref\_sync\_src\_sel field for all respective SYSREF channels are set to source from SYSREF0. For more information, see the register documentation in the <u>RC31xxxA Programming</u> <u>Guide</u>.



Depending on the SYSREF application, the next step is to set the number of pulses to generate. VC7 can support generating 1 to 256 pulses. To set the pulse count, enter the desired value in the "Pulse Count" (sysref\_pulse\_cnt) field. Note that the value entered will result in value + 1 pulses.



The final step is to enable SYSREF. Select the "Enabled" check box. The SYSREF pulses will generate from IOD0 when GPIO0 transitions from '0' to '1'. Additional pulses will generate with additional GPIO0 toggles.



# 4. Revision History

Revision	Date	Description
1.00	Feb 2, 2022	Initial release.

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