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## M16C/65 Group

### Variable-period variable-duty PWM output

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#### 1. Abstract

In this process, Timer A0 and Timer A1 are used to generate variable-period, variable-duty PWM output. Use the following peripheral function:

- Timer mode of timer A
- One-shot timer mode of timer A

#### 2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

### 3. Specification

- (1) Set timer A0 in timer mode, and set timer A1 in one-shot timer mode with pulse-output function.
- (2) Set 1 ms, the PWM period, to timer A0. Set 500  $\mu$ s, the width of PWM “H” pulse, to timer A1. Both timer A0 and timer A1 use fTIMAB for the count source.
- (3) Connect a 20MHz oscillator to XIN.
- (4) Using POFSi bit in TAPOFS register to select the output polarity of the TAiOUT pin.

### 4. Operation

- (1) Setting the count start flag to “1” causes the counter of timer A0 to begin counting. The counter of timer A0 performs a down count on count source fTIMAB.
- (2) If the counter of timer A0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A0 interrupt request bit goes to “1”.
- (3) An underflow in timer A0 triggers the counter of timer A1 and causes it to begin counting. When the counter of timer A1 begins counting, the output level of the TA1OUT pin goes to “H”.
- (4) As soon as the count of the counter of timer A1 becomes “0000h”, the output level of TA1OUT pin goes to “L”, and the counter reloads the content of the reload register and stops counting. At the same time, the timer A1 interrupt request bit goes to “1”.

Figure 1 shows the operation timing.

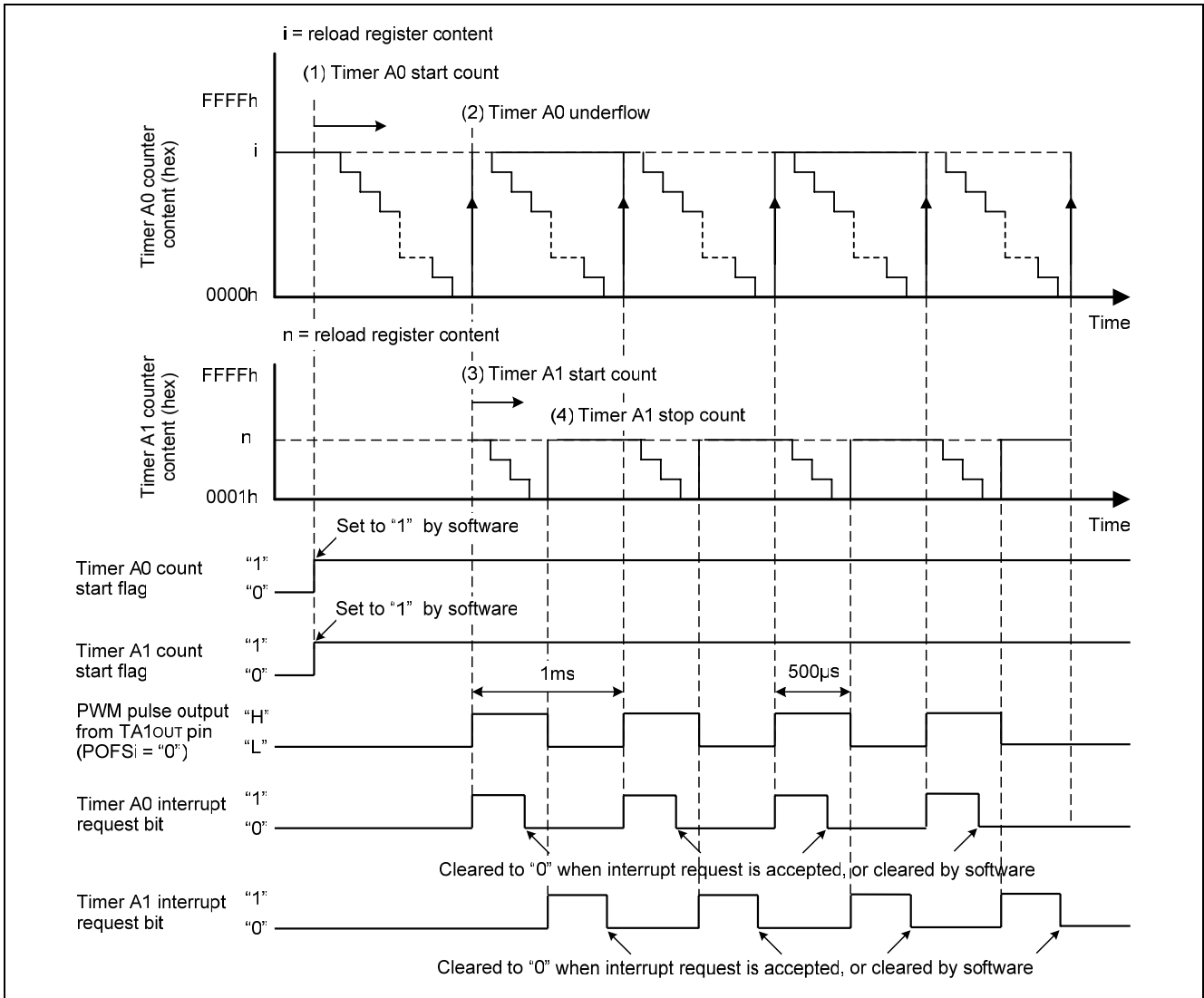


Figure 1. Operation timing of variable-period variable-duty PWM output

Figure 2 shows the connection diagram.

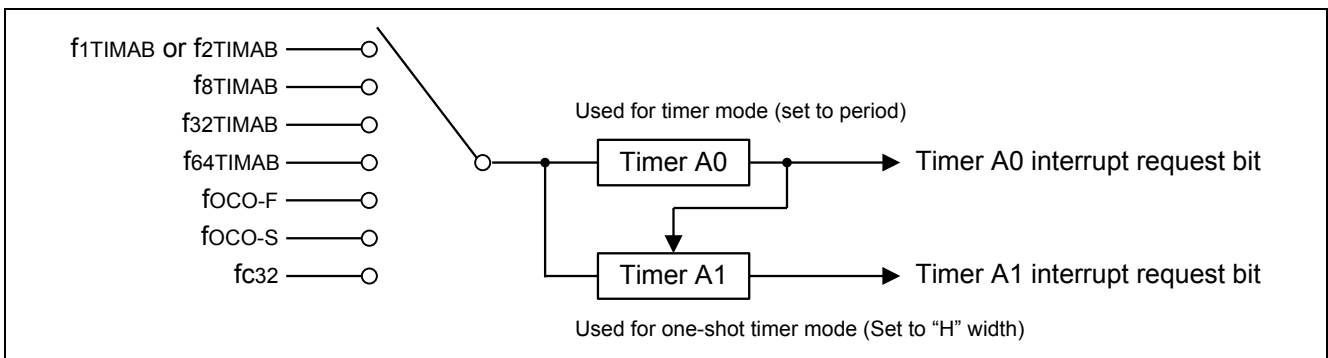


Figure 2. Connection diagram of variable-period variable-duty PWM output

## 5. Set-up procedure

Table 1 shows Timer A count source, Figure 3 shows block diagram of Timer A count source in timer mode.

**Table 1. Count Source Selection of Timer A**

TCKDIV00 register (Note 1)	TACSj register (Note 2)				TAiMR register		Count source	Count source period
	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		
								f(X <sub>IN</sub> ):20MHz f(X <sub>CIN</sub> ):32.768kHz f(oco-F):about 20MHz f(oco-s):about 125kHz
0	0	-	-	-	0	0	f <sub>1</sub> TIMAB/ f <sub>2</sub> TIMAB (Note 3)	50ns/100ns
0	0	-	-	-	0	1	f <sub>8</sub> TIMAB	400ns
0	0	-	-	-	1	0	f <sub>32</sub> TIMAB	1600ns
0	0	-	-	-	1	1	fc <sub>32</sub>	976.56μs
0	1	0	0	0	-	-	f <sub>1</sub> TIMAB/ f <sub>2</sub> TIMAB (Note 3)	50ns/100ns
0	1	0	0	1	-	-	f <sub>8</sub> TIMAB	400ns
0	1	0	1	0	-	-	f <sub>32</sub> TIMAB	1600ns
0	1	0	1	1	-	-	f <sub>64</sub> TIMAB	3200ns
0	1	1	0	0	-	-	foco-F	about 50ns
0	1	1	0	1	-	-	foco-s	about 8μs
0	1	1	1	0	-	-	fc <sub>32</sub>	976.56μs
1	1	0	0	0	-	-	f <sub>1</sub> TIMAB/ f <sub>2</sub> TIMAB (Note 3)	about 50ns/100ns
1	1	0	0	1	-	-	f <sub>8</sub> TIMAB	about 400ns
1	1	0	1	0	-	-	f <sub>32</sub> TIMAB	about 1600ns
1	1	0	1	1	-	-	f <sub>64</sub> TIMAB	about 3200ns

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.

Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f<sub>1</sub>TIMAB. When the PCLK0 bit is "0", the selected clock source is f<sub>2</sub>TIMAB.

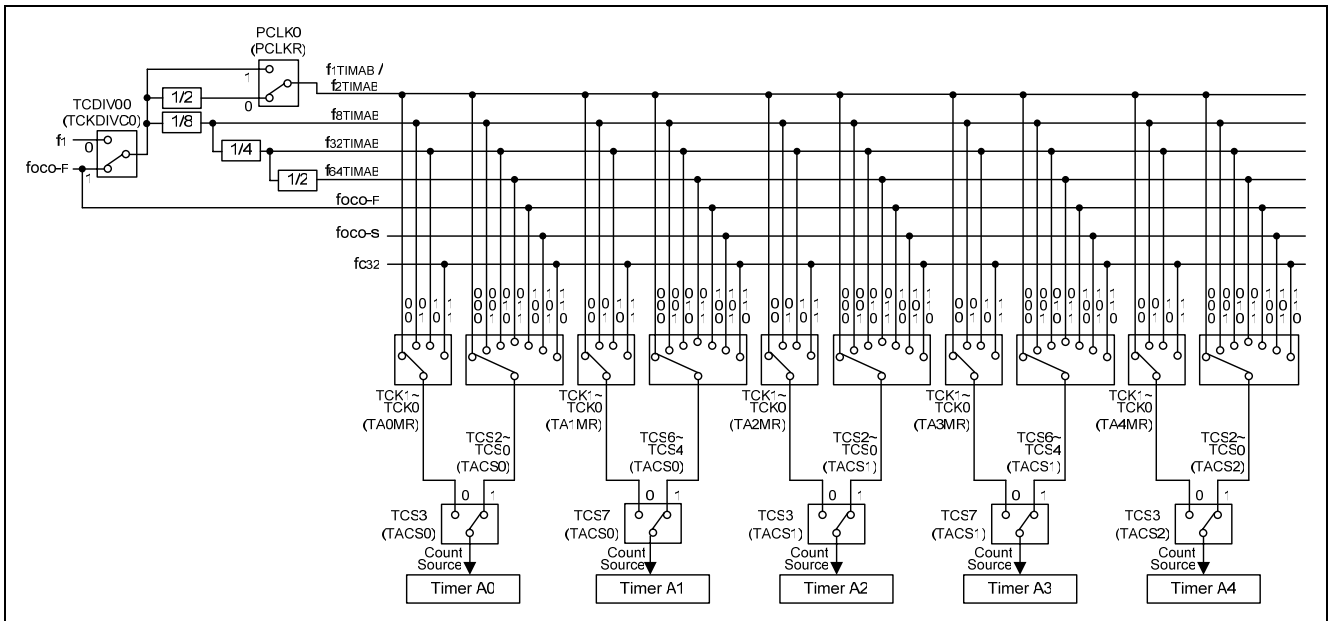
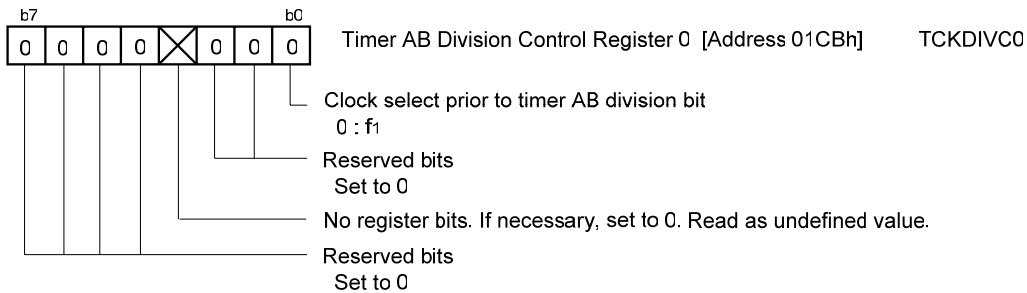


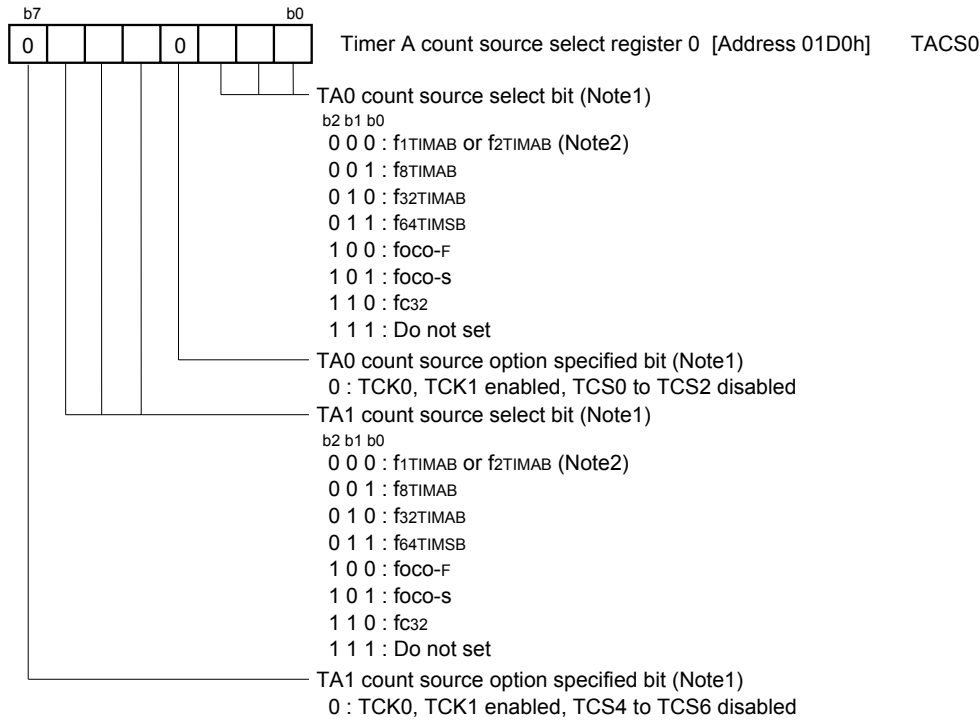
Figure 3. Count source of Timer A

Selecting a clock used prior to timer AB frequency dividing

(Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.)



Selecting timer count source

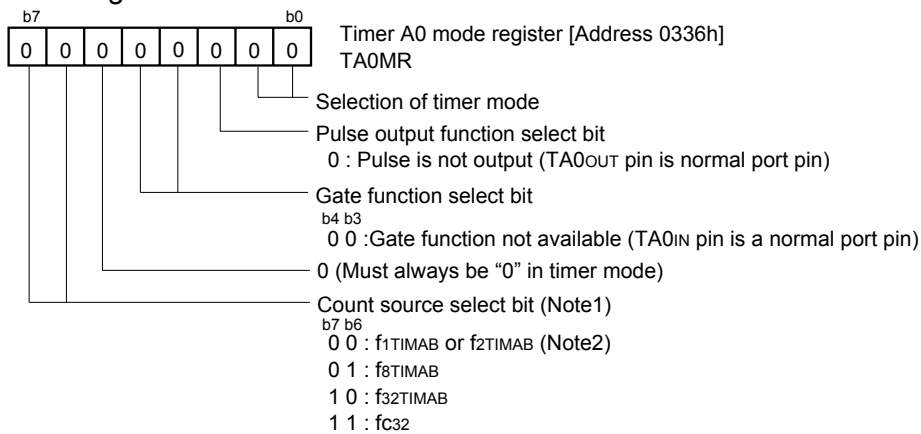


Note 1: About the count source period, please refer to Table 1.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Setting timer A0

Selecting timer mode and functions

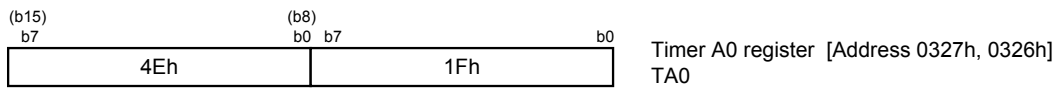


Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 1.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

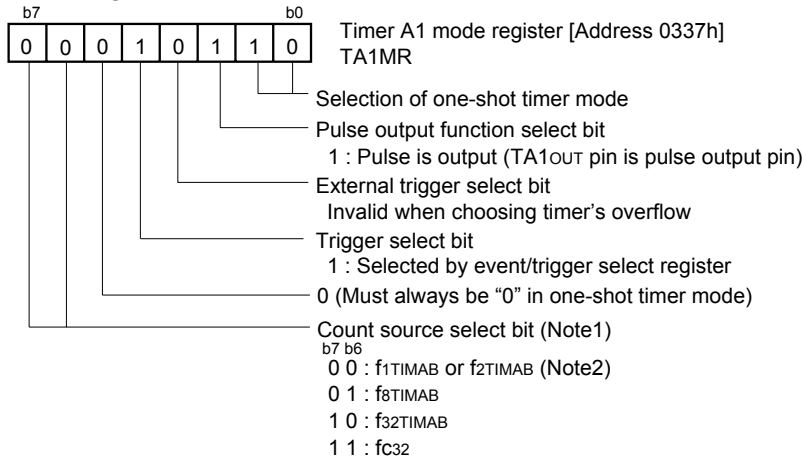


Setting counter value



Setting timer A1

Selecting one-shot timer mode and functions

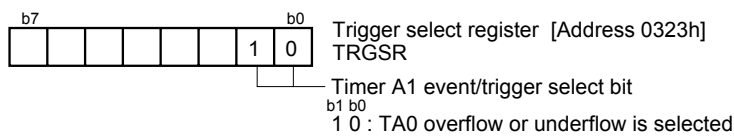


Note 1: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 1.

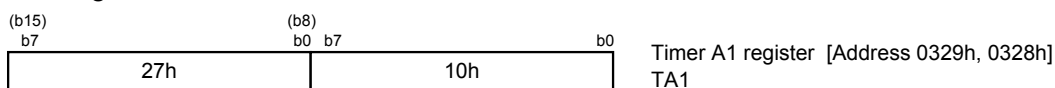
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Setting event/trigger select bit

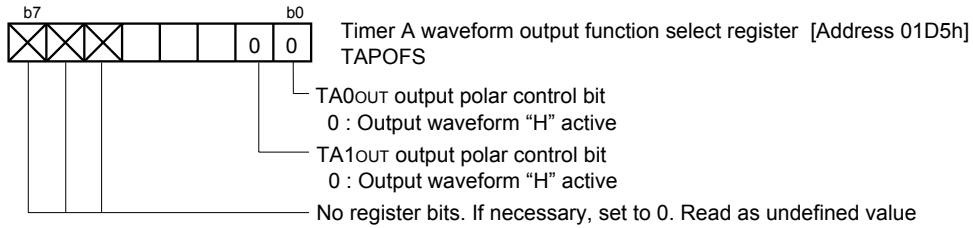
(Set timer A0 to trigger timer A1)



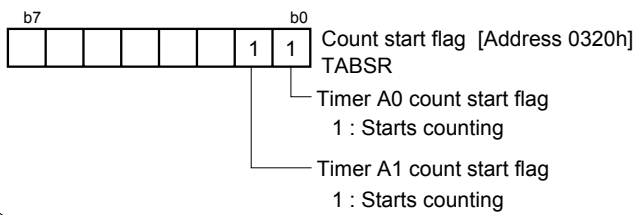
Setting one-shot timer's time



Selecting waveform output function



Setting count start flag



*Start counting*

## 6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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**Revision**

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